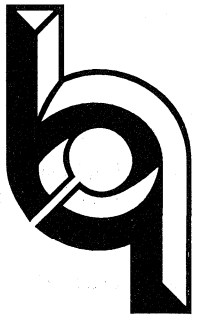
1995 DATA BOOK

BENCHMARQ



BENCHMARQ

1995
Data Book

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BENCHMARQ 1995 Data Book

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Our Products

At Benchmarq, we provide integrated circuit and module solutions for power-sensitive and portable electronics systems.

Power-sensitive AC-powered systems in the office and industry must gracefully deal with the loss of power, maintaining the integrity of important data and self-sufficiently continuing critical operation. Portable systems share the design requirements of their powercord-bound counterparts, but add entirely new challenges—including power supervision, energy management, data security, and size minimization.

The product families described in this data book directly address these requirements, taking full advantage of advanced analog and digital VLSI technologies and state-of-the-art battery and packaging expertise. Power supervision, energy management, size reduction, nonvolatility, data security, and retrofit capability are integral to Benchmarq's product line.

Our Commitment

When you choose to integrate Benchmarq products within your own, be assured that Benchmarq is committed to providing the specific solutions you need today and to developing creative solutions to the growing challenges of tomorrow—supported by the best customer service and the highest overall quality.

The drive for excellence in all dimensions of quality is a cornerstone of our company.

Data Book Organization

This data book is organized into general information sections and product family sections.

You can locate information in this book in several ways.

To locate information by:	See pages:
Table of Contents	v – vi
Alphanumeric Product Index	vii – viii
Family Summary and Selection Guides	1-1 – 1-6
Product Cross-Reference Tables	1-7 – 1-8
Ordering Information	1-9

Chapters 2 through 5 contain detailed product information. Chapter 6 includes packaging information, and Chapter 7 describes Benchmarq's commitment to quality and the processes we use to ensure reliability in our products. Chapter 8 lists sales offices and distributors.

For More Information ...

If you haven't found it here . . . Ask!

Benchmarq maintains an updated product listing on the World Wide Web at the URL listed below. Browse the Benchmarq Home Page for the latest Benchmarq product information and sales office locations at:

http://synapse.onramp.net/benchmarq/

To send us e-mail to be added to our mailing list or to get further information, contact Benchmarq at:

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Additional Benchmarq information is available from your Benchmarq distributor or sales office (listed in the back of this Data Book), or by contacting Benchmarq Customer Service at (800) 966-0011 or (214) 407-0011.

Alphanumeric Product Index

Data Sheet Types

Product information data sheets progress in detail as the product goes from design to full production.

The three types of data sheets are defined below.

- Advance Information: Benchmarq Advance Information data sheets provide information for early product planning. These data sheets describe a product in the design or development stage. Specifications may change in any manner.
- Preliminary: Benchmarq Preliminary data sheets provide preliminary specifications for product design. They describe a product through its early production stage. Supplementary data may be published at a later date.
- Final: Benchmarq data sheets not labeled Advance Information or Preliminary are considered Final. They describe a product in full production and provide specifications for product design.

Benchmarq reserves the right to make changes to any products without notice.

Engineering Prototype

Prior to full production, Benchmarq may provide limited quantities of Engineering Prototypes. Engineering Prototypes are suitably tested for evaluation and restricted use. Any necessary errata data accompanies engineering prototype parts. They are marked with the part number and are identified as Engineering Prototypes.

Electrostatic Discharge (ESD) and Integrated Circuit (IC) Handling

Benchmarq ICs, as all ICs, are sensitive to electrostatic discharge (ESD). Although Benchmarq ICs are designed to withstand high ESD voltages, improper handling may cause damage. Standard ESD-prevention handling procedures should be followed. ESD-prevention considerations include proper grounding of operators, work surfaces and chip-handling equipment; appropriately high relative humidity levels; and use of antistatic handling and packaging materials. The ICs should be stored and shipped in antistatic tubes. The antistatic tubes containing the ICs must be brought to the same potential as the work area/operator before the individual ICs are handled.

bq2001 Energy Management Unit™ (EMU™) Summary and Selection Guide

The bq2001 EMU battery-management IC provides a "gas gauge" capacity monitor, fast charge control, and sophisticated battery conditioning for battery-operated electronic systems.

- Gas gauge capability for direct measurement of battery discharge consumption and capacity
- Fast charging and conditioning control for nominal 4.8V–12V nickel cadmium or lead acid batteries
  - Programmed constant charge, pulsed charge, or "burp" charge
  - Full charge detection by negative delta voltage, maximum temperature, maximum voltage, and maximum charge time
- Programmable for adaptive operation
- EEPROM default settings for application-specific configuration
- Programmable open-drain outputs for status indication or control
- Provides battery-backup supply from main battery, switching to backup cell
- Operates directly from 5.5V–18V charging supply or 4.5V–5.5V V_{CC}
- Direct microprocessor bus interface for capacity monitoring

bq2001 EMU Selection Guide

Configuration	Battery Voltage	Operating Supply	Backup Supply Output Voltage	Pins / Package	Part Number	Page Number
Microprocessor peripheral	up to 18V	5.5–18V charging supply or 4.5V–5.5V V_{CC}	2–6V	24 / .300" NDIP, SOIC	bq2001	2-1

Fast Charge IC Summary and Selection Guide

The Fast Charge IC family provides fast charge control, switch-mode current regulation, and battery conditioning for rechargeable batteries.

- Fast charging and conditioning of nickel cadmium, nickel metal hydride, lead acid, lithium ion, or rechargeable alkaline batteries
- Flexible current regulation:
  - Frequency-modulated switching current regulator for low-heating design
  - Gating control for use with external regulator
- Easily integrated into systems or as a stand-alone charger
- Pre-charge checks for temperature and voltage faults
- Direct LED outputs display battery and charge status
- Fast charge termination by delta temperature/delta time, negative delta voltage, peak voltage detect, maximim voltage/minimum current, maximum temperature, voltage, and time
- Optional top-off charge
- Discharge-before-charge option
- Variable-rate charging uses excess supply current to charge batteries during system operation

Fast Charge IC Selection Guide

Battery Technology	Charge Control Output	Termination Method	Key Features	Pins / Package	Part Number	Page Number
NiMH NiCd	Single	-ΔV, peak voltage, time, and temp. and voltage qual.	Low power and small size	8/.300" DIP, 8/.150" SOIC	bq2002	2-31
NiMH NiCd	Single	ΔT/Δt, max. temp., time, and temp. and voltage qual.	Low power and small size	8/.300" DIP, 8/.150" SOIC	bq2002T	2-41
NiMH NiCd Lead Acid	Single	-ΔV, ΔT/Δt, max. temp., voltage, and time	Includes PWM	16/.300" DIP, 16/.300" SOIC	bq2003	2-53
NiMH NiCd	Single	-ΔV, peak voltage, ΔT/Δt, max. temp., voltage, and time	PWM and low power mode	16/.300" DIP, 16/.150" SOIC	bq2004	2-109
NiMH NiCd	Single	-ΔV, peak voltage, ΔT/Δt, max. temp., voltage, and time	PWM, pulsed precharge conditioning	16/.300" DIP, 16/.150" SOIC	bq2004E	2-121
NiMH NiCd	Dual	-ΔV, ΔT/Δt, max. temp., voltage, and time	Sequential charger	20/.300" DIP, 20/.300" SOIC	bq2005	2-139
NiMH NiCd	Single	-ΔV, peak voltage, max. temp, voltage, time	LCD/LED display	24/.300" DIP, 24/.300" SOIC	bq2007	2-173
Lead Acid	Single	max. voltage/min. current, $-\Delta^2V$, temp., and time	Temp. compensated thresholds	16/.300" DIP, 16/.150" SOIC	bq2031	2-305
Lithium Ion	2–4 cells	max. charge and discharge voltage safety cut-off	Very low power	8/.300" DIP, 8/.150" SOIC	bq2053	2-345
Lithium Ion	Single	max. voltage/min current, temp and voltage qual.	Temp. compensated thresholds	16/.300" DIP, 16/.150" SOIC	bq2054	2-346
Rechargeable Alkaline	2 cells	maximum voltage	Individual cell charging	8/.300" DIP, 8/.150" SOIC	bq2900	2-347
Rechargeable Alkaline	3 or 4 cells	maximum voltage	Individual cell charging	14/.300" DIP, 14/.150" SOIC	bq2901	2-355

The Gas Gauge IC family measures the available charge, calculates self-discharge, and optionally provides the available charge over a serial port or by directly driving an LED display.

- Conservative and repeatable measurement of available charge for nickel cadmium, nickel metal-hydride, and lithium ion rechargeable batteries
- Designed for battery pack integration
  - 150µA typical operating current
- Integrate within a system or as a stand-alone device
  - Serial port or direct LED display
- Self-discharge calculation compensated using internal temperature sensor
- Measurement compensated for current rate and temperature
- Accurate measures across a wide range of currents
- bq2012/bq2014 charge-control output controlled by measured state-of-charge, temperature, and voltage
- System Management Bus and Smart Battery Data support (bq2040)

Gas Gauge Selection Guide

Configuration	Application	Key Features	Pins / Package	Part Number	Page Number
Battery pack or system integration	General	Low cost, min. components	16/.300" DIP, 16/.150" SOIC	bq2010	2-209
Battery pack or system integration	Very high discharge rates (i.e., power tools)	Low cost, min. components	16/.300" DIP, 16/.150" SOIC	bq2011	2-241
Battery pack or system integration	General	Charge control output	16/.300" DIP, 16/.150" SOIC	bq2012	2-263
Battery pack or system integration	General	External charge control support	16/.300" DIP, 16/.150" SOIC	bq2014	2-285
Battery pack or system integration	SMBus interface	External E^2 support	16/.300" DIP, 16/.150" SOIC	bq2040	2-319
Battery pack or system integration	Li-Ion packs	Capacity in mAh and mWh	16/.300" DIP, 16/.150" SOIC	bq2050	2-343

Nonvolatile SRAM Summary and Selection Guide

Benchmarq's NVSRAMs integrate—in a single-DIP package—extremely low standby power SRAM, nonvolatile control circuitry, and a long-life lithium cell. The NVSRAMs combine secure nonvolatility (more than 10 years in the absence of power) with standard SRAM pinouts and fast unlimited read/write operation.

- ➤ Data retention in the absence of power
- ➤ Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10 or 5 years minimum data retention in the absence of power
- ➤ Battery internally isolated until power is first supplied
- ➤ Industrial temperature range available

Nonvolatile SRAM Selection Guide

Density	Configuration	Technology	Access Time (ns)	Minimum Data-Retention Time	Pins / Package	Part Number[1]	Page Number
64 Kb	8 Kb x 8	NVSRAM	70, 85[2], 150[2], 200	10 years	28 / DIP	bq4010/ bq4010Y	5-1
256 Kb	32 Kb x 8	NVSRAM	70[2], 85, 150[2], 200	10 years	28 / DIP	bq4011/ bq4011Y	5-11
1 Mb	128 Kb x 8	NVSRAM	70[2], 85[2], 120	10 years	32 / DIP	bq4013/ bq4013Y	5-21
2 Mb	256 Kb x 8	NVSRAM	85, 120	10 years	32 / DIP	bq4014/ bq4014Y	5-31
	128 Kb x 16	NVSRAM	85, 120	10 years	40 / DIP	bq4024/ bq4024Y	5-41
4 Mb	512 Kb x 8	NVSRAM	85, 120	5 or 10 years	32 / DIP	bq4015/ bq4015Y	5-51
	256 Kb x 16	NVSRAM	85, 120	5 years	40 / DIP	bq4025/ bq4025Y	5-61
4 Mb	512 Kb x 8	NVPSRAM	150[3]	10 years[3]	40 / DIP	bq4115Y	5-71

Notes:
1. "Y" version denotes 10% V_{CC} tolerance.
2. "Y" version available in -40°C to +85°C industrial temperature range.
3. See data sheet for details.

Benchmarq's nonvolatile controllers provide power monitoring, write-protection, and supply switching to convert standard SRAM or PSRAM and a backup battery into a reliable, predictable nonvolatile memory. The nonvolatile controller modules are complete battery-backup solutions including an encapsulated 130mAh lithium cell that is isolated until power is applied.

- Power monitoring and switching for 3V battery-backup applications
- Automatic write-protection during power-up/power-down cycles
- Automatic switching from V_{CC} to first backup battery and from first backup battery to second backup battery
- Reset output option for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation
- Control up to four banks of SRAM
- Module/DIP or SOIC packages

Nonvolatile Controller Selection Guide

SRAM Banks Controlled	Battery Monitor Outputs	Reset Output	I_{OUT} (Typ.)	Pins / Package	Part Number	Page Number
1			160 mA	8 / NDIP, NSOIC	bq2201	3-1
2		✓	160 mA	16 / NDIP, NSOIC	bq2202	3-9
2	✓	✓	160 mA	16 / NDIP, NSOIC	bq2203A	3-17
4			160 mA	16 / NDIP, NSOIC	bq2204A	3-25
2		✓	80 mA	16 / NDIP, NSOIC	bq2212	3-33
2		✓	160 mA	12 / DIP module	bq2502	3-45

Real-Time Clock Summary and Selection Guide

Benchmarq's IBM® PC AT-compatible real-time clocks (RTCs) provide highly integrated clock/calendar solutions for microcomputer-based designs. Each *module* is a completely self-contained unit, including IC, crystal, and a battery ensuring operation for 10 years in the absence of power. The very compact, low-power *ICs* need only a battery and a crystal for operation. NVSRAM controller versions allow users to make inexpensive SRAM nonvolatile for EISA/MCA bus, Plug and Play, portable, and other applications.

- ➤ Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- ➤ Completely self-contained modules operate for more than 10 years in the absence of power
- ➤ IC versions require only a crystal and battery
- ➤ 114/242 bytes of user nonvolatile storage RAM
- ➤ 32kHz output for power management (E/ L)
- ➤ 2.7–3.6V operation (L versions)
- ➤ Calendar in day, date, month, and year with automatic leap-year adjustment
- ➤ Time of day in seconds, minutes, and hours
- ➤ One minute per month clock accuracy in modules
- ➤ Nonvolatile control for an external SRAM

Benchmarq's high-density modules combine 32Kbytes or 128Kbytes of memory with the RTC, battery, and crystal to provide a self-contained battery-backed-up real-time clock/NVSRAM solution. The modules have standard SRAM pin-outs and interfaces. The bq4832Y and bq4842Y provide a built-in CPU supervisor with a microprocessor reset and watchdog timer. The bq4845/Y and bq4847/Y RTCs With CPU Supervisor allow flexible memory configurations with their built-in NVSRAM controller.

Real-Time Clock Selection Guide

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	32kHz Output	CPU Super-visor	Pins / Package	Part Number	Page Number
114		Muxed	5V			24 / DIP, SOIC 28 / PLCC	bq3285	4-1
242		Muxed	5V	✓		24 / DIP, SOIC, SSOP 28 / PLCC	bq3285E	4-19
242		Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq3285L	
114		Muxed	5V			24 / DIP module	bq3287/ bq3287A	4-43
242		Muxed	5V	✓		24 / DIP module	bq3287E/ bq3287EA	4-61
114	✓	Muxed	5V			24 / DIP, SOIC 28 / PLCC	bq4285	4-79
114	✓	Muxed	5V	3		24 / DIP, SOIC, SSOP, 28 / PLCC	bq4285E	4-99
114	✓	Muxed	3V	3		24 / DIP, SOIC,SSOP, 28 / PLCC	bq4285L	4-99
114	✓	Muxed	5V			24 / DIP module	bq4287	4-125
32K		SRAM	5V			28 / DIP module	bq4830Y	4-145
32K		SRAM	5V		✓	32 / DIP module	bq4832Y	4-159
128K		SRAM	5V		✓	32 / DIP module	bq4842Y	4-173
0	✓	SRAM	5V		3	28 / DIP, SOIC	bq4845/Y	4-187
0	✓	SRAM	5V		3	28 / DIP module	bq4847/Y	4-205

NVSRAM Cross-Reference

Density	Dallas Semiconductor	SGS-Thomson	Benchmarq
64Kb	DS1225AB DS1225AD/Y	MK48Z08 MK48Z18	bq4010 bq4010Y
256Kb	DS1230AB DS1230Y DS1630AB DS1630Y	M48Z30 M48Z30Y - -	bq4011 bq4011Y Contact factory Contact factory
1Mb	DS1245AB DS1245Y DS1645AB DS1645Y DS1645EE	M48Z128 M48Z128Y - - -	bq4013 bq4013Y Contact factory Contact factory Contact factory
2Mb	- - DS1658AB DS1658Y	M48Z256 M48Z256Y M46Z128 M46Z128Y	bq4014 bq4014Y bq4024 bq4024Y
4Mb	DS1650 DS1650Y - -	M48Z512 M48Z512Y M46Z256 M46Z256Y	bq4015 bq4015Y bq4025 bq4025Y

Real-Time Clock Cross-Reference

Dallas Semiconductor	SGS-Thomson	Motorola*	Benchmarq
DS1285/885	-	MC146818AP MC146818BP	bq3285P
DS1285Q/885Q	-	MC146818FN	bq3285Q
DS1285S/885S	-	MC146818SP	bq3285S
DS1287/887	MK48T87B24	MC146818BM	bq3287MT
DS1287A/887A	-	MC146818B1M	bq3287AMT

* Last-time buy in progress—obsolete device.

Nonvolatile Controllers Cross-Reference

Dallas Semiconductor	Benchmarq
DS1210	bq2201PN [4]
DS1210S	bq2201SN [1, 4]
DS1221	bq2204APN [3, 4]
DS1221S	bq2204ASN [2, 3, 4]

Notes:

1. Benchmarq's bq2201SN is a small 8-pin, 150-mil SOIC, compared to the DS1210S, which is a 16-pin, 300-mil SOIC.
2. Benchmarq's bq2204ASN is a small 16-pin, 150-mil SOIC, compared to the DS1221S, which is a 16-pin, 300-mil SOIC.
3. Optional "security feature" DS1221 pins are no-connect on the bq2204A.
4. Benchmarq's bq2201 and bq2204A do not incorporate a "check battery status" function.

Benchmarq's standard products are available in several packages and operating ranges. A valid order number is a sequence of:

- Device
- Package Options
- Speed Options
- Temperature Range

Valid options for a specific device are defined in the ordering information section at the end of its data sheet. Contact your Benchmarq sales office about non-standard requirements or to place an order. Sales offices are listed at the end of this data book.

bq40xx MA - __ __

Temperature Range:

blank	= Commercial (0 to +70°C)
N	= Industrial (-40 to +85°C)

Speed Options:

70, 85, ... , 200, or blank

Package Options:

P	= Plastic DIP
PN	= Narrow Plastic DIP
S	= SOIC
SN	= Narrow SOIC
Q	= Quad PLCC
Mx	= x-type module

Device:

bq2003
bq2201
bq4011Y
bq4287
etc.

Examples:

bq2003S
bq2201SN-N
bq2204PN-N
bq4010YMA-150N
bq4011MA-100
bq4287MT

Notes

BENCHMARQ

bq2001

Energy Management Unit (EMU)

Features

- Microprocessor peripheral for battery management and related functions
- Direct measurement of battery charge consumption and capacity
- Fast charging and conditioning control for nominal 4.8V to 12V nickel cadmium, lead acid, or nickel hydride batteries
- Full-charge detection by negative delta voltage method, maximum temperature, maximum voltage, and maximum time
- Programmable for adaptive operation
- EEPROM default settings for application-specific configuration
- Open-drain outputs for status indication or control
- Provides and controls 3V battery-backup supply
- Operates from 5.5–18V DC or 4.5–5.5V V_{CC} supplies

General Description

The BiCMOS bq2001 Energy Management Unit (EMU) is a low-power microprocessor peripheral providing battery-management services for systems using rechargeable (secondary) batteries. The bq2001 works directly from the DC charging supply, operating as programmed, or from 5V V_{CC}, operating as a microprocessor peripheral. bq2001-based systems can easily incorporate sophisticated capacity monitoring, battery management, backup supply services, and power-conservation capabilities.

The "gas gauge" register provides the actual charge consumption from the secondary battery and measures the actual battery capacity. The charge time register allows calculation of the energy stored following partial or complete recharge. The programmed end-of-discharge voltage (EDV) threshold determines full discharge.

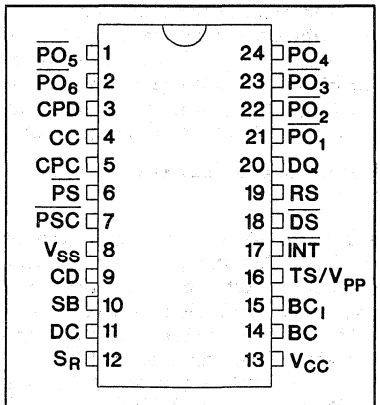
Battery management includes charge control at standard to fast charge rates, with full charge determined using the preferred negative delta voltage (-ΔV) method, a maximum temperature threshold, a maximum voltage threshold, and a maximum time limit. The EMU may also be configured to inhibit or abort charging when the battery temperature is below an acceptable temperature range. Trickle charge can occur before and after charging. Non-operational discharge before charge may be selected for cell conditioning or capacity measurement. Charge patterns may be programmed to be constant, pulsed, or "burp" (alternating charge/discharge).

For the power-off condition, the bq2001 regulates the secondary battery input to maintain its programmed state while it simultaneously sources a backup cell output to maintain a real-time clock or other low-current battery-backed ICs. A backup cell provides system data retention current when the secondary battery is depleted or removed.

System design is simplified by six open-drain outputs controlled by the EMU or the host processor. These may be allocated for subsystem control, LED activation, EMU status indication, and system power switch control.

2

Pin Connections



24-Pin SDIP or SOIC

PN-30

Pin Names

$\overline{DS}$	Data strobe input
RS	Register select input
DQ	Data input/output
$\overline{INT}$	Interrupt request output
V_{CC}	+5V system supply input
DC	Charging supply input
BC	Backup cell output
BC_I	Backup cell input
SB	Secondary battery input
S_R	Sense resistor input
CC	Charge control output
CPC	Charge pump capacitor output
CPD	Charge pump diode output
CD	Discharge control output
TS/V_{PP}	Temperature sensor input or programming voltage input
$\overline{PS}$	Power switch input
$\overline{PSC}$	Power switch control output
$\overline{PO_1}$	Charging indicator or programmable output 1
$\overline{PO_2}$	End-of-discharge voltage indicator or programmable output 2
$\overline{PO_3}$	Temp not OK indicator or programmable output 3
$\overline{PO_4}$	DC valid indicator or programmable output 4
$\overline{PO_5}$	Gas gauge threshold indicator or programmable output 5
$\overline{PO_6}$	Secondary battery fault or programmable output 6
V_{SS}	System ground

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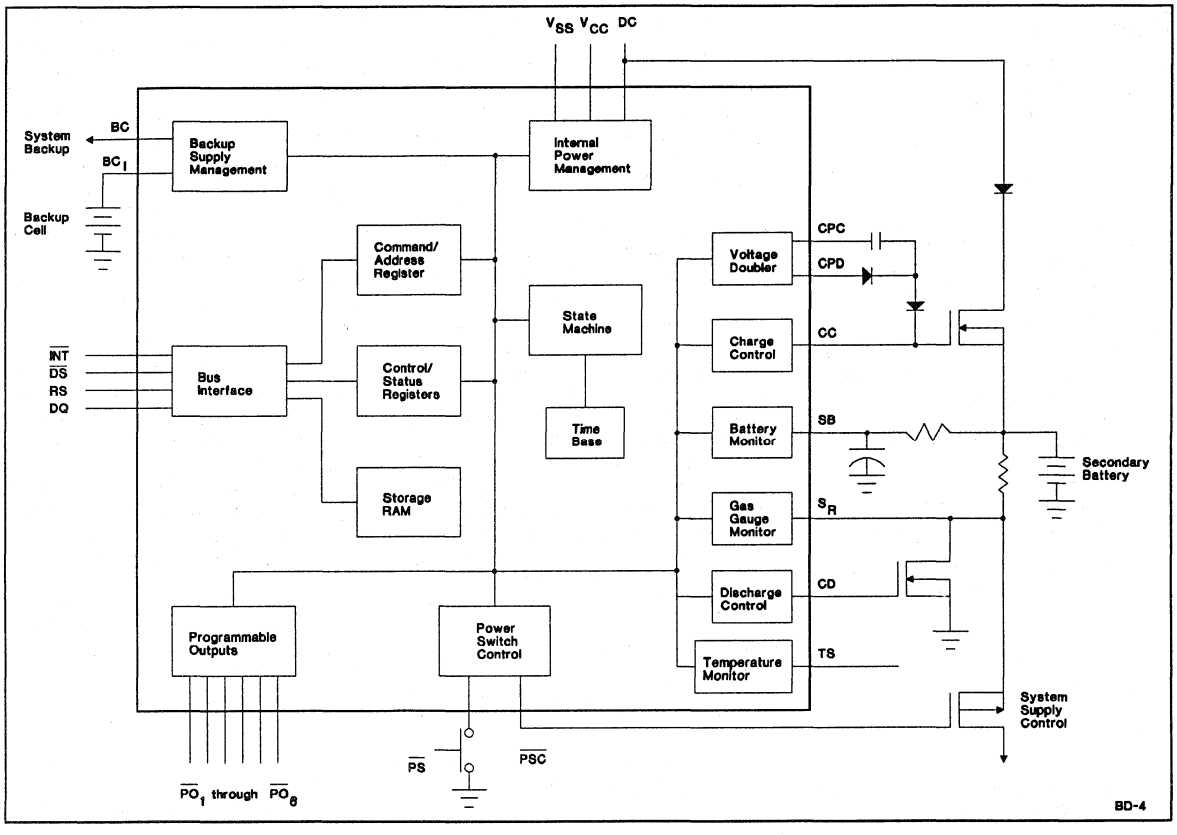
Block Diagram



Pin Descriptions

$\overline{DS}$ **Data strobe TTL-level input**

$\overline{DS}$ is used to identify the time when read data is used to drive DQ or for latching write data present on DQ. During read cycles, valid data is output on DQ after time t_{ACS} following $\overline{DS}$ asserted low. During write cycles, the rising edge on $\overline{DS}$ latches the input data on DQ into the bq2001.

RS **Register select TTL-level input**

RS is used during an access cycle to identify the data byte type. RS low identifies the data bit as part of a command byte to be written to the command register, CMR. RS high identifies the data bit as part of a read or write data byte for the control and status register or storage RAM as addressed in the preceding CMR read or write command. An incomplete data byte being transferred to or from the bq2001 is terminated if a low is present on RS when $\overline{DS}$ becomes active. This allows synchronization of a data-byte transfer (return to CMR to restart the sequence).

DQ **Data bit bidirectional TTL-level input/ output**

DQ is used to transfer one bit of data from or to the bq2001. During a read cycle, the bq2001 outputs one bit of data on the DQ pin at time t_{ACS} after the falling edge of $\overline{DS}$ and returns the output driver to the high impedance state t_{DHZ} time after $\overline{DS}$ rises. Valid write data must be presented for time t_{DW} before the rising edge of the $\overline{DS}$ pulse.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$, an open-drain output, goes low to indicate an interrupt request. The interrupt request is activated by reaching end-of-discharge voltage (EDV), the gas gauge threshold, a low transition on the $\overline{PS}$ pin, or the application of V_{CC}. $\overline{INT}$ may be tied to the NMI of the host processor so that the system can not overlook this request. $\overline{INT}$ goes to high impedance in the absence of V_{CC}.

V_{CC} **V_{CC} supply input**

V_{CC}, 5V system supply, must be valid during system operation to operate the microprocessor interface and—in the absence of DC—the gas gauge.

DC **DC supply input**

DC is the secondary battery charging supply input. DC must be provided a valid voltage during charge actions. The DC input powers the bq2001 during charge actions in the absence of V_{CC}.

BC **Backup cell output**

BC is the backup cell supply output pin. A voltage regulated from S_R to the voltage value on BC_I is output on BC as a backup source for a real-time clock, data retention, and other battery-backed requirements (see Figure 1). For proper regulation, the BC pin must be provided a minimum capacitance of 0.1µF and a maximum of 1.0µF.

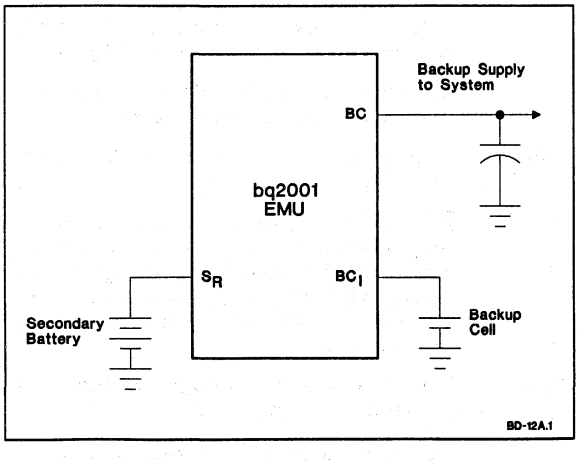


Figure 1. Backup Supply and Sources

BC_I **Backup cell input**

BC_I is the supply input for a backup cell. BC_I also provides the reference voltage to which the secondary battery is regulated for internal data retention and output on BC. No protective circuits are required between the backup cell and BC_I (see Figure 1).

When the BC output voltage regulated from S_R falls below the backup cell voltage, the backup cell input is switched directly through the bq2001 to the BC output.

BC_I is monitored for the backup cell low-voltage threshold.

SB **Secondary battery supply input**

SB is the secondary battery input pin. SB is monitored for negative delta voltage (-ΔV), maximum battery voltage, end-of-discharge voltage (EDV), secondary battery inoperable, and secondary battery replaced.

An R-C filter is recommended in front of SB for noise reduction and to generate the recommended V_{OFF} (negative offset voltage between SB and S_R). The R may be calculated from:

$$R = V_{OFF} * R_{SB} / V_{SB}, \text{ or}$$
$$R = 2.8mV * 1.1M\Omega / V_{SB}$$

Based on this R, C should be selected to provide a time constant of 1–3ms.

S_R **Sense resistor input**

S_R, part of the gas gauge subsystem, is used along with SB to measure the voltage across the sense resistor. The sense resistor should be chosen by fitting it to the profile of the secondary battery discharge rate, allowing the highest gas gauge accuracy. Typical applications achieve high accuracy when the voltage drop across the sense resistor from SB to S_R is in the range of 30 to 170mV during the discharge periods that dominate battery drain. (See Capacity Monitoring for details.) S_R also powers the BC output and bq2001 data retention.

***Caution*: To avoid damaging the device, the voltage at S_R must never be held at more than 400mV above SB.**

CC **Charge control output**

CC is an open-drain output that is high impedance during the charging period of a charge action interval. CC provides charge

control if used to switch an external channel power FET. The voltage at CC may be two times the voltage at DC to allow full turn-on of the external charge control FET. CC is high impedance in the absence of voltage on DC.

CPC **Charge pump capacitor output**

CPC is part of the voltage-doubler circuit. The voltage-doubler output is only available for use with pin CC. This pin should be connected to one end of a capacitor. The capacitor value must be as large as the input capacitance of the n-FET being controlled and may be a maximum of 1µF. (See Figure 2.)

If the voltage doubler is not used, CPC must be left open.

CPD **Charge pump diode output**

CPD is part of the voltage-doubler circuitry. The CPD pin supplies the charge pump for the voltage doubler. This output is inactive when CC is low.

If the voltage doubler is not used, CPD must be left open.

CD **Discharge control output**

CD is an open-drain output used to control an n-channel power FET during a bq2001 controlled discharge. CD is high impedance during the discharge phase of a charge action or during the discharge period of a charge interval. (See Charge Action.)

TS/V_{PP} **Temperature sensor input/V_{PP} input**

The TS input voltage is used to sense the battery temperature. Input voltages below or above the min/max thresholds may prevent or terminate charging. The TS input voltage alternatively provides the programming voltage for the internal EEPROM.

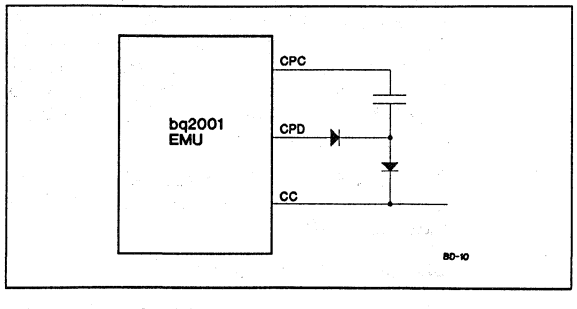


Figure 2. Voltage Doubler and Charge Control

$\overline{PS}$ **Power switch input**

$\overline{PS}$ selects system on/off status for the bq2001. In conjunction with $\overline{PSC}$ output, $\overline{PS}$ may be used to control the gate of a FET switch. When the power switch status bit = 1 ($\overline{PSC}$ active), $\overline{PS}$ incorporates 30ms (minimum) debounce.

$\overline{PS}$ low causes the following actions:

1. Activates $\overline{PSC}$ if $\overline{PSC}$ is inactive.
2. Discontinues any existing charging action prior to $\overline{PSC}$ being activated.
3. Sets the power switch state bit, status register bit 7, to 1.
4. Sets the power switch interrupt bit, status register bit 0, to 1.
5. Generates an $\overline{INT}$ output.

$\overline{PSC}$ **Power switch control output**

$\overline{PSC}$ is an open-drain output that may be used for turning system power on or off. $\overline{PSC}$ is activated (low impedance to V_{SS}) following $\overline{PS}$ low and deactivated by writing the system-off command to the command register (CMR). The polarity is meant to drive a p-channel FET.

When $\overline{PSC}$ is active, a charge action may only be initiated through the command register, CMR.

When $\overline{PSC}$ is inactive, a charge action may be initiated by the appearance of the later of either valid charging supply or battery voltage.

The status of $\overline{PSC}$ is reflected in the status register (SR) power switch state bit.

$\overline{PO_1}$ **Charging indicator or programmable output 1**

$\overline{PO_1}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 1, charging (mask register bit 1 = 1). When mask register bit 1 = 0, $\overline{PO_1}$ is controlled by output control register (OCR) bit 1.

$\overline{PO_2}$ **End-of-discharge voltage indicator or programmable output 2**

$\overline{PO_2}$ is an open-drain output that may be programmed to indicate when the secondary battery voltage is at or below the end-of-discharge voltage threshold defined by the end-

of-discharge cell voltage register and the number of cells field. When mask register bit 2 = 0, $\overline{PO_2}$ is controlled by output control register (OCR) bit 2.

$\overline{PO_3}$ Temp not OK indicator or programmable output 3

$\overline{PO_3}$ is an open-drain output that may be programmed to indicate when the TS input voltage is below or above the min/max thresholds. When mask register bit 3 = 0, $\overline{PO_3}$ is controlled by output control register (OCR) bit 3.

$\overline{PO_4}$ DC valid indicator or programmable output 4

$\overline{PO_4}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 4, DC valid (mask register bit 4 = 1). When mask register bit 4 = 0, $\overline{PO_4}$ is controlled by output control register (OCR) bit 4.

$\overline{PO_5}$ Gas gauge threshold or programmable output 5

$\overline{PO_5}$ is an open-drain output that may be programmed to indicate when the gas gauge value increments to or beyond the gas gauge threshold (mask register bit 5 = 1). This output will go active or inactive on or before a one-half count gas gauge increment following a gas gauge value transition below-to-equal/above or equal/above-to-below the gas gauge threshold. This is true whether this transition is caused by a change to the gas gauge count or a change to the gas gauge threshold. When mask register bit 5 = 0, $\overline{PO_5}$ is controlled by output control register (OCR) bit 5.

$\overline{PO_6}$ Secondary battery fault indicator or programmable output 6

$\overline{PO_6}$ is an open-drain output that may be programmed to indicate the condition of status register (SR) bit 6, secondary battery fault (mask register bit 6 = 1). When mask register bit 6 = 0, $\overline{PO_6}$ is controlled by output control register (OCR) bit 6.

V_{SS} Ground

V_{SS} is the system ground pin. All bq2001 supplies are defined relative to this pin.

2

Functional Description

Microprocessor Interface

The bq2001 provides a simple and space-efficient three-pin serial data interface to Intel, Motorola, and other parallel or serial bus architectures. This interface is active only when V_{CC} is valid. Table 1 shows the microprocessor interface truth table.

The interface uses command bytes (written to the command register, CMR) that direct access to 18 data bytes used for control and status, and to 32 data bytes provided for nonvolatile storage of programmer-defined information. CMR is used to directly write any of three direct action commands or to manage subsequent data-byte access.

Data-byte access through CMR involves writing one of the four access commands. Two of the commands direct access to the control and status registers, and two direct access to the storage RAM. Each of the four data-byte access commands includes the internal data-byte address.

Table 1. Microprocessor Interface Truth Table

Mode	RS	$\overline{DS}$	Immediately Prior Command Byte		I/O Operation
			Command Field	Address Field	
Output disable	X	H	XXX	XXXXX	High Z
Command	L	L	XXX	XXXXX	D_{IN}
Control and Status Register:					
Read	H	L	011	AAAAA	D_{OUT}
Write	H	L	101	AAAAA	D_{IN}
Storage RAM:					
Read	H	L	010	AAAAA	D_{OUT}
Write	H	L	100	AAAAA	D_{IN}

The physical interface uses bidirectional DQ (data I/O pin) to read or write data one bit at a time. The logic level on RS (register select input pin) identifies the byte currently being accessed as CMR (command register) or a data byte.

$\overline{DS}$ (data strobe input pin) is used during write cycles to latch the data at DQ into memory, and during read cycles to clock the EMU data out on DQ. $\overline{DS}$ should be gated with the chip select generated for the bq2001. Input data is accepted as valid only after the last bit of a complete byte is written.

A fourth microprocessor interface pin, $\overline{INT}$ (interrupt request output), allows the EMU to generate interrupt requests to the host processor. When any of the interrupt bits in the status register (SR) is set to 1, then $\overline{INT}$ goes active, powered by V_{CC}. Any of three events sets an interrupt bit:

- $\overline{PS}$ (power switch input) is brought low, indicating a power-on or power-off request. The power switch interrupt bit (PSI) is set to 1.
- The secondary battery has discharged to the programmed gas gauge threshold. The gas gauge interrupt bit (GGI) is set to 1.
- The secondary battery has discharged to the programmed end-of-discharge voltage threshold. The end-of-discharge voltage interrupt bit (EDVI) is set to 1.

$\overline{INT}$ also becomes active on application of V_{CC}. $\overline{INT}$ becomes inactive when SR is read. This action also clears PSI, GGI, and EDVI.

Capacity Monitoring

The bq2001 incorporates a "gas gauge" discharge counter that provides a real measurement of the charge drawn from the secondary battery. When DC or V_{CC} is valid, the gas gauge meters current from the secondary battery, incrementing the value in the gas gauge register pair, GG. The host system subtracts the gas gauge reading from the previous actual or the nominal capacity for that battery. The gas gauge is reset by a full recharge, by an abort command, or by battery removal.

The charge time register (CTR) allows the processor to estimate the amount of charge put into the battery. CTR counts the time, in 4.25-minute intervals, that a charge phase is enabled. CTR is reset to zero each time the gas gauge is reset.

The secondary battery discharge rate is monitored for the gas gauge by measuring the voltage across a sense resistor using S_R, sense resistor input, and SB, secondary battery input. The sense resistor should be chosen by fitting it to the system battery discharge rate profile to achieve acceptable average gas gauge accuracy. Figure 3 indicates the gas gauge error with respect to a range of voltage drops across the sense resistor.

The sense resistor should be selected to minimize total error, especially for systems that include significant battery discharge across a wide range of currents. Typically, no more than a small portion of the total discharge should occur with high error (that is, with very small voltage drop).

The gas gauge samples at a 512Hz rate. The gas gauge count rate is proportional to the voltage drop across the sense resistor, except for the error shown in Figure 3. A time-averaged 70mV signal causes the gas gauge counter

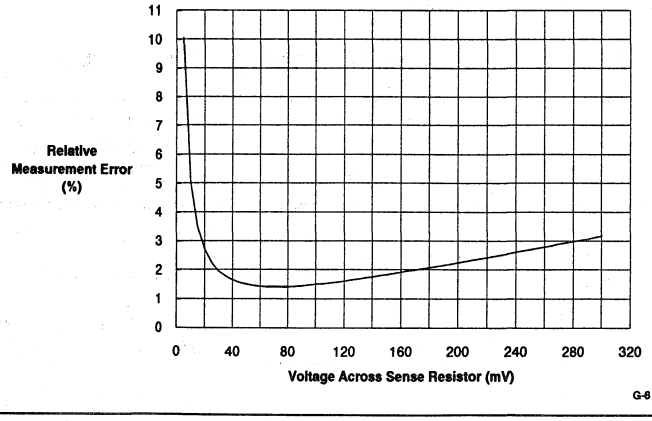


Figure 3. Gas Gauge Measurement Error

to wrap around after 20 hours. A time-averaged 140mV signal wraps around after 10 hours.

Removed charge is determined as follows:

$$\text{Removed charge (mAh)} = \frac{\text{gas gauge value}}{47 \times S_R\,(\Omega)}$$

A gas gauge measurement to full battery discharge (end-of-discharge voltage, EDV) is a measure of the actual secondary battery capacity. When the battery discharges to EDV, the gas gauge value is automatically loaded into the last capacity register pair, an interrupt is generated on $\overline{INT}$ (V_{CC} valid), and the status register (SR) end-of-discharge voltage interrupt bit is set to 1. Mask register bit 2 may be programmed so that passing EDV also activates $\overline{PO_2}$. The EDV threshold is selected by programming a configuration of 2 to 10 cells and an EDCV threshold of 0.6 to 2.42V per cell.

When the gas gauge becomes equal to the gas gauge threshold programmed in the gas gauge threshold register pair, an interrupt request is generated on $\overline{INT}$ (V_{CC} valid), and the status register (SR) gas gauge interrupt bit is set to 1. Mask register bit 5 may be programmed so that reaching the gas gauge threshold activates $\overline{PO_5}$.

The gas gauge register (and CTR register) is reset to 0 by:

- Charge action termination due to -ΔV, maximum temperature, maximum charge time, or maximum voltage determination, any of which indicates full charge.
- An abort charge action command written to CMR (command register).
- Battery removal.

The CTR register is a volatile register. If V_{CC} or DC power is not available, then data in CTR will be lost. (See the application note, "bq2001 Gas Gauge Monitoring.")

The gas gauge register may be interpreted in conjunction with charge setup register 2 (CSR2) bit 0, gas gauge not valid (GGNV), and CSR2 bit 1, battery removed (BR).

GGNV = 1 indicates to the host that the gas gauge register value does not reflect discharge from bq2001-determined full charge, and may not be valid.

GGNV is set to 1 by:

- The start of a charge phase.
- Battery removal.

GGNV is reset to 0 by:

- Charge action termination due to -ΔV, maximum temperature, maximum charge time, or maximum voltage determination, any of which indicates full charge.
- Writing it to 0 (if a charge action is not active and the battery is present).

BR = 1 indicates to the host that the battery has been removed. BR must be written to zero to clear it.

GGNV and BR values are interpreted as follows:

Values		Interpretation
GGNV	BR	
0	0	Full charge completed; last capacity reference is valid.
0	1	Battery has been replaced; subsequent full charge completed
1	0	Incomplete charge.
1	1	Battery removed; unknown charge state.

When GGNV = 1 because of incomplete charge, the charge time register (CTR) enables the host processor to estimate the amount of charge put into the battery. In the event that a full charge is not achieved, the host processor can use the CTR value, the charge current, and a charge efficiency factor to estimate the amount of partial recharge. Any value in CTR applies to the present battery.

Charge Action

The bq2001 initiates a charge action as programmed. See Table 2, Charge Action Initiation Truth Table.

A charge action may consist of two phases. The first phase may be a CD output-controlled discharge, draining the secondary battery for conditioning or capacity determination purposes. The second phase is the charge phase. The status register (SR) charging bit is 1 during both phases. The mask register (MR) may be written such that $\overline{PO_1}$ is active throughout the charge action.

If $\overline{PSC}$ is active (power switch state bit = 1), a programmed charge action initiates only when a start charge action command is written to the command register, CMR, after all other conditions for charge initiation are valid ("command-initiated" charge).

If $\overline{PSC}$ is inactive (power switch state bit = 0), a programmed charge action is initiated without command. In this "DC-initiated" charge mode, with all charge action conditions valid, charging initiates on either (1) each application of DC (independent of V_{CC}) or (2) each replacement of the battery.

DC-initiated charge action may be qualified to occur only if the CSR2 GGNV status bit is 1 by setting CSR1 bit 7 (GGNV qualified charge) to 1. This qualification allows the system to prevent DC-initiated charge actions with the current battery. Removing and replacing the battery sets GGNV, allowing DC-initiated charge.

Table 2. Charge Action Initiation Truth Table

Charge Action, as Programmed		SR Bit 4	SR Bit 6	CSR1 Bits 5,4	CSR1 Bit 7	CSR2 Bit 0	SR Bit 7	CSR2 Bit 5	CSR2 Bit 4
Discharge Phase	Charge Phase	DC Valid	Secondary Battery Fault	Charge Action Selection	GGNV Qualified Charge	Gas Gauge Not Valid	Power Switch State	Temper-ature Enable	Temper-ature OK
Disabled		0	X	XX	X	X	X	X	X
Disabled		X	1	XX	X	X	X	X	X
Disabled		X	X	11	X	X	X	X	X
Enabled	Note 1	1	0	00, 01, or 10	X	X	X	1	0
Ignored	DC Initiated	1	0	00, 01, or 10	X	1	0	1	1
Ignored	DC Initiated	1	0	00, 01, or 10	X	1	0	0	X
DC-Initiated Disabled		1	0	00, 01, or 10	1	0	0	X	X
DC Initiated		1	0	00, 01, or 10	0	0	0	1	1
DC Initiated		1	0	00, 01, or 10	0	0	0	0	X
Command Initiated		1	0	00, 01, or 10	X	X	1	1	1
Command Initiated		1	0	00, 01, or 10	X	X	1	0	X

Note: 1. Terminates as fault ($V_{TS} \leq V_{TSL}$) or terminates as full ($V_{TS} \geq V_{TSH}$).

When $\overline{PS}$ is toggled low to activate $\overline{PSC}$, any charge action is discontinued before $\overline{PSC}$ goes active. Charge action may be reinitiated after $\overline{PSC}$ is active, through CMR.

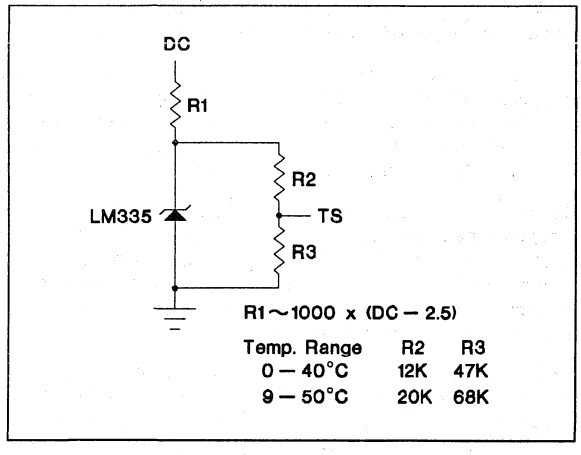


Figure 4. Example: Temperature Control Using an LM335

Temperature control of the charge phase of a charge action is accomplished using the TS input. When temperature enable (CSR2 bit 5) is written to 1, the charge phase is terminated as full whenever the TS input voltage is above 2.5V and prevented from occurring whenever this voltage is below 2.18V. The TS input voltage may be supplied using an LM335 powered by the DC supply. See Figure 4. Charge setup register 2 (CSR2) bit 4, TOK, is 1 whenever the TS input voltage is above 2.18V and below 2.50V (temperature OK). The mask register (MR) may be written such that $\overline{PO_3}$ is active whenever the TS input voltage is below 2.18V or above 2.50V (temperature not OK).

Charge action is prevented from starting when any of the following conditions occurs:

- CSR1 bits 5 and 4 (charge action selection) are both set to 1.
- SR bit 7 (power switch state) is 0, CSR1 bit 7 (GGNV qualified charge) is 1, and the CSR2 GGNV status bit is 0.
- Status register (SR) bit 4 (DC valid) is 0.
- Status register (SR) bit 6 (secondary battery fault) is 1.
- No discharge phase; CSR2 bit 5 (temperature enable) is 1 and CSR2 bit 4 (temperature OK) is 0 due to low temperature.

Any charge action is stopped when any of the following occurs (see Table 3, Charge Action Termination Truth Table):

- $\overline{PS}$ is toggled low to activate $\overline{PSC}$ (only stops DC-initiated charging).
- Abort charge actions command is written to CMR (only if power switch state = 1).
- Status register (SR) bit 4 (DC valid) is 0.
- Status register (SR) bit 6 (secondary battery fault) is 1.
- Full charge is determined.
- CSR2 bit 5 (temperature enable) is 1 and CSR2 bit 4 (temperature OK) is 0 (during charge phase only).
- CSR1 bits 4 and 5 are both written to 1.

Table 4 summarizes events that start a charge phase after charge action termination due to a fault.

Discharge Phase

The discharge phase of a charge action consists of the bq2001 activating the CD output, turning on a discharge path for the secondary battery. The gas gauge is operational during the discharge phase. The discharge phase continues until the programmed gas gauge threshold is reached or EDV is reached or charge action is terminated.

The bq2001 is programmed for discharge in CSR1 to:

- Not discharge prior to charge,
- Discharge to the value in the gas gauge threshold register (to full discharge if it occurs first), or
- Discharge fully if the gas gauge is already beyond the gas gauge threshold register value.

Typically, the second option may be used for periodic cell conditioning to avoid any voltage-depression effect. The last option may be used to force full discharge for conditioning or to measure capacity. It may also be used to allow full discharge only when the battery is near empty.

Table 4. Recovery From Charge-Action-Terminating Faults

Terminating Fault	SR bit 7 Power Switch State	Recovery Event
DC not valid (DCV = 0)	1	DCV = 1 and charge command
	0	DCV = 1
Secondary battery fault (SBF = 1)	1	SBF = 0 and charge command
	0	SBF = 0
Temp. enabled (CSR2 bit 5 = 1) and below min. temp. (charge phase only)	1	TOK = 1 and charge command
	0	TOK = 1

Table 3. Charge Action Termination Truth Table

Cause of Termination	Gas Gauge Reset	CSR2 Bit 0 (GGNV)	Trickle Charge (if enabled)
$\overline{PS}$ low to activate $\overline{PSC}$ (SR bit 7 from 0 to 1)	No	1	Yes
DC not valid (SR bit 4 = 0)	No	1	No
Secondary battery fault (SR bit 6 = 1)	No	1	Yes
Temp. enabled (CSR2 bit 5 = 1) and below min. temp. during charge phase	No	1	Yes
CSR1 bits 4 and 5 written to 1,1	No	1	Yes
Abort charge action command	Yes	1	Yes
-ΔV detected (-ΔV enabled)	Yes	0	Yes
Maximum temperature (Temp. enabled)	Yes	0	Yes
Maximum charge time	Yes	0	Yes
Maximum charge voltage	Yes	0	Yes

The full discharge threshold is the end-of-discharge voltage (EDV) determined from the number of cells programmed in charge setup register 1 and the end-of-discharge cell voltage register value. At EDV, the gas gauge value is transferred to the last capacity register.

At completion of the programmed discharge phase, the charge action enters the charge phase.

In a DC-initiated charge action (power switch state bit = 0), when the gas gauge not valid (GGNV) bit = 1, any programmed discharge phase is ignored, and the charge action begins with the charge phase.

In all cases, when the battery removed (BR) bit = 1, any programmed discharge phase is ignored, and the charge action begins with the charge phase.

Charge Phase

The charge phase of a charge action consists of the bq2001 modulating the CC output and optionally the CD output. The charge phase may be continuous, pulsed, or "burp" (alternating charge/discharge pulses, with or without an idle state). See Figure 5.

The charge phase consists of eight-second charge intervals, which repeat until charge termination. The bq2001 is programmed for periods of charge, discharge, and no action during each eight-second interval.

The CC output controls charging by switching an n-channel power FET. The desired average charging current from the DC supply is determined by the programmed duty cycles. To minimize heat generation in high-charging-current applications, two pins are available to build a charge pump that doubles the DC voltage, allowing full turn-on of an n-channel FET.

The charging period is programmed into the charging period register, with time specified in units of 1/32 seconds. The charging period register can be programmed for continuous charging (charging period = 256 units) or for pulsed charging (charging period < 256 units), as shown in Figure 5.

For burp charging, the discharge period register can be programmed with a discharge-after-charge period (see Figure 5). In operation, the charging period takes precedence over the discharge period. The discharge period may be no longer than the remainder of the eight-second interval following completion of the charge period.

Full charge is determined following detection of -ΔV, maximum temperature, maximum charge time, or maximum charge voltage—whichever occurs first.

Full charge may be determined by the negative delta voltage (-ΔV) slope detection if enabled in charge setup register 2 (-ΔV enable). The delta voltage sensitivity is selected using charge setup register 1 bit 6. The sampling period for the -ΔV determination is defined in charge setup register 2. The selectable sensitivity and sampling period allows charge control across a wide range of cells and charge rates.

Full charge may be determined by maximum temperature detection if enabled in charge setup register 2 (temperature enable). Full charge is determined whenever the TS input voltage exceeds 2.50V.

Full charge is also determined if the charge phase exceeds the maximum charge time register value or the cell voltage exceeds the maximum charge voltage per cell.

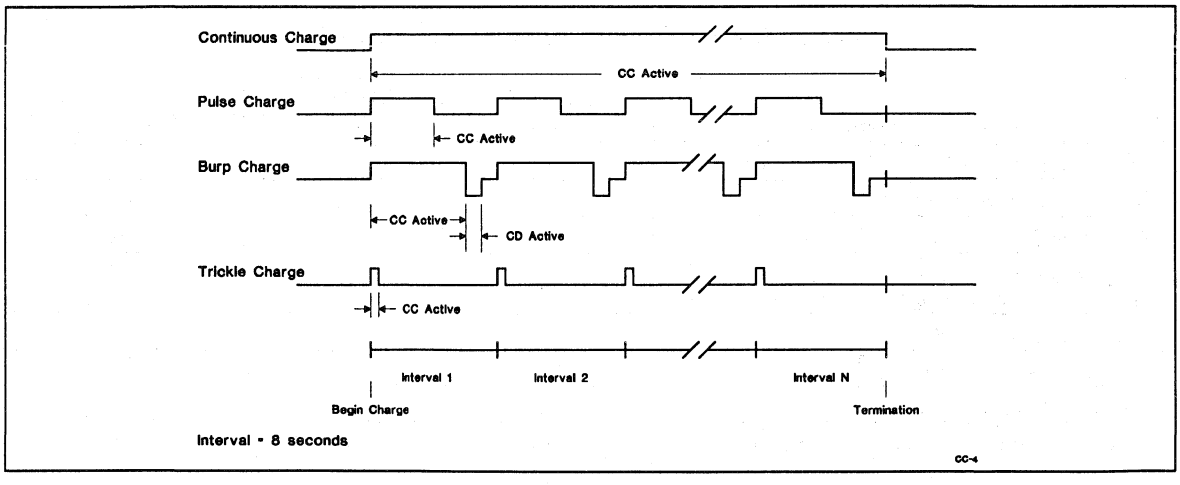


Figure 5. Charge Phase and Trickle Charge Modulation

Note: For -ΔV determination, the charging voltage per cell (with the number of cells as programmed in the CSR1 register) must be above the end-of-discharge cell voltage (EDCV) and less than EDCV plus 1.0V. For example, if a five-cell battery has an end-of-discharge voltage of 1.0V per cell, -ΔV detection requires a charging voltage between 5V and 10V.

Trickle Charge

When the trickle enable bit in charge setup register 2 (CSR2) is set, the EMU initiates the charge-sustaining trickle charge defined by the period in the trickle period register if DCV = 1 and the secondary battery is not being charged. See Figure 5.

Gas gauge discharge counting is disabled during trickle charge. Trickle charge is terminated by:

- Disabling trickle charge (CSR2 bit 2 = 0).
- No DC supply (DCV = 0).
- Normal charge initiation.

Backup Power Management

The bq2001 sources the external low-current battery-backed integrated circuits through BC, backup cell output. The bq2001 regulates power from the secondary battery to the voltage present on BC_I (backup cell input) for internal data retention and for output at BC. The BC output can be used in the absence of system power as a battery-backup source for static CMOS devices such as a real-time clock or static RAM.

When the secondary battery is removed or becomes depleted, an external power source connected to BC_I must support the bq2001 and external data retention. This backup automatically switches in as the data retention power source for the bq2001 and for the circuits sustained by BC. (See Figure 1.)

Annunciation or Switch Control

Programmable open-drain outputs $\overline{PO_1}$ through $\overline{PO_6}$ may be used to activate annunciators such as LEDs. These six outputs are programmable to become active (low impedance to V_{SS}) based on internal EMU status or as written by the host processor.

- Writing any of mask register bits 1 to 6 to a value of 1 causes the associated output pin $\overline{PO_1}$ to $\overline{PO_6}$ to become active under EMU control.
- Writing any of mask register bits 1 to 6 to a value of 0 sets the associated output pin $\overline{PO_1}$ to $\overline{PO_6}$ to become active whenever the corresponding control bit in the output control register is written to 1.

Thus $\overline{PO_1}$ to $\overline{PO_6}$ can be selected to be activated by the host processor (with system power on) or by internal EMU status.

Microprocessor control of open-drain output pins $\overline{PO_1}$ to $\overline{PO_6}$ also allows any one of them to be used to control a switch.

Rewriting a mask register bit between power-on and power-off may allow the corresponding output pin to be active as written by the processor when power is on and active reflecting EMU status when power is off (and DC is valid).

On/Off Control

The bq2001 may be used for system on/off control by hardware and software inputs. $\overline{PS}$ and $\overline{PSC}$ may be used to control an external pFET.

$\overline{PS}$ is the power switch input. $\overline{PS}$ may be toggled to turn the system on, and may be toggled to initiate a request to turn off.

$\overline{PSC}$, power switch control output, is an open-drain output intended to drive a p-channel FET, which may control the system supply. $\overline{PSC}$ is activated by $\overline{PS}$ taken low and deactivated by a system off command written to CMR.

When $\overline{PS}$ is brought low and $\overline{PSC}$ is inactive, the bq2001 sets the status register power switch state (PS) bit and the power switch interrupt (PSI) bit to 1, terminates any charge action, and activates $\overline{PSC}$.

When $\overline{PS}$ is brought low and $\overline{PSC}$ is active, the bq2001 sets the status register (SR) power switch interrupt (PSI) bit to 1. The power switch state (PS) bit is reset to 0 and $\overline{PSC}$ is deactivated when the system off command is written to CMR. This command stays active until another command is issued or V_{CC} is removed. When a valid DC or V_{CC} supply is attached to the bq2001, the PS bit is set to 1 if $\overline{PS}$ is low or to 0 if $\overline{PS}$ is high.

Note: Because the power switch state bit determines the means of charge action initiation (see Charge Action), the power switch state bit may need to reflect system power status even if $\overline{PSC}$ is left open.

EEPROM Default Programming

The bq2001 contains 12 bytes of EEPROM that set the default values loaded into the read/write control registers during initialization. Initialization occurs on the first application of DC or V_{CC} after loss of the control and status register information. Control and status register information may be lost when DC, V_{CC}, and BC_I are all invalid.

The program in Listing 1 provides the steps to write default values to the EEPROM. Values written to EEPROM are copied into the control and status registers on initialization.

Listing 1. EEPROM Erase and Write Example Procedure

```
#define byte unsigned char
#define CONFIG_CNT 12
  int read_data(int loc) /* returns data value at location loc */
  void write_cmd(int com) /* writes com value to command register */
  void write_data(int data) /* writes data value to data register */

struct {
        byte address;
        byte value;
       } init_config [CONFIG_CNT]= {

              1,0,      /* DPR set to 0 */
              2,0x7F,   /* CPR set to 4 seconds */
              3,0x01,   /* TPR set to 2/32 second */
              6,0x00,   /* GGTL set to 0 */
              7,0x02,   /* GGTH set to 2 so gas gauge threshold is set to 512 */
              8,0x69,   /* EDCV set to 1 volt */
              11,0xBD,  /* MCV set to 1.8 volt */
              12,0x1C,  /* MCT set to 2 hours */
              13,0x06,  /* set CSR1 to 6 cells, no discharge, and charge enabled */
                        /* and -DV threshold of 2.5 to 5.0mV */
              14,0x48,  /* set CSR2 to -DV time of 64 secs, temp disabled, -DV */
                        /* enabled, and trickle disabled */
              15,0x76,  /* enable output control by CHG,EDV,DCV,GGN,SBF, & OCR bit 3 */
              16,0,     /* All PO off */
            };
write_ee_defaults(data) int data[]; {
  byte i;
  read_data(0); /* sync SIO */
  i=read_data(16);
  write_cmd(0xB0); /* select byte 16 of control and status for write */
  write_data(0x80 | i); /* set PGM to 1 */
  write_cmd(0x20); /* set up vppmux */
  apply_vpp(); /* apply 15V to TS */
  write_cmd(0xA0); /* erase eeprom block */
  write_data(0); /* completes the command */
  wait_200ms(); /* wait for 200 milliseconds */
  write_cmd(0x20); /* terminate erase cycle */
  for(i=0; i<CONFIG_CNT; i++) {
    write_cmd(init_config[i].address) /* initiate write with internal addr. hold */
    write_cmd(0x80 | init_config[i].address); /* write data */
    write_data(init_config[i].data);
    wait_200ms(); /* wait for 200 milliseconds */
    write_cmd(init_config[i].address); /* terminate write with internal addr. hold */
        }
  remove_vpp(); /* vpp must be removed from TS before program enable bit is reset */
  i = read_data (16);
  write_cmd(0xB0); /*reset program enable bit */
  write_data(0x7F & i);
  }
```

Note: During initialization, the EMU registers are not accessible.

Register Description

The bq2001 has two data groups independently addressable through the write-only command and address register, CMR: (1) storage RAM and (2) control and status registers. CMR is written with command bytes that serve as action commands or that control the access of a subsequent data byte.

The storage RAM provides 32 data bytes of general purpose nonvolatile RAM storage capability, accessed with RS high.

The control and status registers consist of 18 bytes, also accessed with RS high. See Table 5.

Command Register (CMR)

The write-only CMR register is accessed when register select, RS, is low during a write access. CMR is used to start an action such as charge a battery or abort charging. The CMR register is also used to select the address and action to be performed on any data byte. Each read or write sequence must begin with a read or write command. Commands are written with the least-significant bit first.

The address field (bits 0–4) contains the address of the data byte to be accessed. The values for this field may range from 00000 to 11111 for the storage RAM and from 00000 to 10001 for the control and status registers, with all other values reserved.

The command field (bits 5–7) of this register indicates the action to be taken. Acceptable command field values are:

Bits			Command Field Values
7	6	5	
0	0	0	No operation
0	0	1	System off command
0	1	0	Read from address AAAAA of the bq2001 storage RAM
0	1	1	Read from address AAAAA of the bq2001 control and status registers
1	0	0	Write to address AAAAA of the bq2001 storage RAM
1	0	1	Write to address AAAAA of the bq2001 control and status registers
1	1	0	Start charge action command
1	1	1	Abort charge action command

The three action commands are:

The ***system off action command*** may be used to shut the system down. When the system issues this command, the power switch control output, $\overline{PSC}$, becomes high impedance, and the status register power switch state bit is cleared to 0.

The ***start charge action command*** starts a charge action when written to replace any one of the other seven commands after all other charge-initiation conditions are already valid (see Charge Action). This command is interpreted as "no operation" when written before all other conditions are valid. This command is the only way to start a charge action if $\overline{PSC}$ is on (power switch state bit = 1).

When the power switch state bit = 1, the ***abort charge action command*** causes any charge action to be discontinued and also resets the gas gauge.

Note: All commands are automatically reset to 000 when V_{CC} is removed. Otherwise, two commands—"system off action" and "abort charge action"—remain resident and active until rewritten.

Storage RAM

One of the 32 bytes of storage RAM is written following a CMR command of 100AAAAA and read following a CMR command of 010AAAAA. AAAAA is the byte address, from 00000 to 11111. Data from the storage RAM is read or written with the least-significant bit first. This RAM is intended for storing the charge capacity reference for one or more batteries, and for recording configuration settings and other data. Data in the storage RAM is nonvolatile in the presence of a valid voltage on BC_I.

Control and Status Registers

One of the 18 bytes of control and status registers is written following a CMR command of 101AAAAA and read following a CMR command of 011AAAAA. AAAAA is the byte address, with only 00000 to 10001 allowed. Data from the control and status registers is read or written with the least-significant bit first. Data in the control and status registers is nonvolatile in the presence of a valid voltage on BC_I.

All writable register bits are initialized by a one-time programmable EEPROM block, which may be programmed to define the default state (following absence of valid DC, V_{CC}, and BC_I) for these bits. During the initialization time when the EEPROM settings are being loaded to the registers, external read/write access is blocked and all bits read as 1.

Table 5 summarizes the control and status registers.

Charge Period Register (CPR)

The charge period register (CPR) is programmed to define the charge period of a charge phase interval. The eight-second charge phase interval consists of a charge

Table 5. Control and Status Registers (X=Don't Care)

Sym-bol	Register Name	Address	Read/ Write	Control Field or Status Bit								Units
				7(MSB)	6	5	4	3	2	1	0	
CPR	Charge period register	2	R/W	-	-	-	-	-	-	-	-	$\frac{1}{32}$sec
CSR1	Charge setup register 1	13	R/W	GGNV quald	-ΔV thrshld	CA selection		number of cells				
CSR2	Charge setup register 2	14	R/W	-ΔV sample time		temp. enable	TOK	-ΔV enable	trickle enable	BR	GGNV	
CTR	Charge time	17	Read	-	-	-	-	-	-	-	-	256 sec
DPR	Discharge period register	1	R/W	-	-	-	-	-	-	-	-	$\frac{1}{32}$sec
EDCV	End-of-discharge cell voltage register	8	R/W	-	-	-	-	-	-	-	-	9.5mV
GGH	Gas gauge, high byte	5	Read	-	-	-	-	-	-	-	-	$\frac{1}{47}$mVh
GGL	Gas gauge, low byte	4	Read	-	-	-	-	-	-	-	-	$\frac{1}{47}$mVh
GGTH	Gas gauge threshold, high byte	7	R/W	-	-	-	-	-	-	-	-	$\frac{1}{47}$mVh
GGTL	Gas gauge threshold, low byte	6	R/W	-	-	-	-	-	-	-	-	$\frac{1}{47}$mVh
LCRH	Last capacity register, high byte	10	Read	-	-	-	-	-	-	-	-	$\frac{1}{47}$mVh
LCRL	Last capacity register, low byte	9	Read	-	-	-	-	-	-	-	-	$\frac{1}{47}$mVh
MCT	Maximum charge time register	12	R/W	-	-	-	-	-	-	-	-	256 sec
MCV	Maximum cell voltage register	11	R/W	-	-	-	-	-	-	-	-	9.5mV
MR	Mask register	15	R/W	X	-	-	-	-	-	-	0	
OCR	Output control register	16	R/W	PGM	-	-	-	-	-	-	re-served	
SR	Status register	0	Read	PS	SBF	GGI	DCV	BCL	EDVI	CHG	PSI	
TPR	Trickle period register	3	R/W	-	-	-	-	-	-	-	-	$\frac{1}{32}$sec

period and optional off and discharge periods. The charge period is one plus the programmed value. The programmed value may be 0 to 255. Values less than 255 are used for pulse or burp charging.

The following are examples of charge period duty cycle values:

CPR	Result
0FFH	Provides continuous current during charging.
63H	Provides for 3.13 seconds of charge current out of every 8 seconds.

Charge Setup Register 1 (CSR1)

Charge setup register 1 (CSR1) contains four configuration fields.

The ***number of cells field*** (bits 0–3) contains the number of cells used to make up the battery. This register is programmed with a scale factor, typically the number of cells, to relate the measured battery voltage back to the single-cell voltage.

CSR1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	N	N	N	N

The maximum cell number is 10 (the initial default), and the minimum is 2. The value need not be the real number of cells, but must be scaled such that this value times the values in registers EDCV and MCV are the EDV and maximum charge voltage thresholds for the battery, respectively.

Caution:

Using the EMU with improperly programmed voltage thresholds may damage the device.

The ***charge action selection field*** (bits 4–5) is used to enable the charge action and select the discharge method. Discharge-before-charge may be initiated on application of a valid DC level or when a charge action command is issued in the CMR.

The charge action selection field is programmed to enable charging and to define the discharge method as follows:

CSR1 Bits							
7	6	5	4	3	2	1	0
-	-	C	C	-	-	-	-

Where CC is:

00 Charge action enabled with no discharge.

01 Charge action enabled with a discharge phase: Discharge until the gas gauge register value is greater than or equal to the gas gauge threshold register value or EDV is reached. (This method may be used to provide battery conditioning cycles by deliberately controlling discharge depth.)

10 Charge action enabled with a discharge phase: Discharge to the EDV limit if the gas gauge value is greater than the gas gauge threshold. (This method may be used to determine the battery capacity.)

11 Charge action disabled (initial default).

The ***-ΔV threshold field*** (bit 6) is programmed to select the threshold used in the -ΔV slope detection for full-charge determination. A -ΔV full-charge determination is made when the voltage at SB decreases by at least the selected voltage threshold through two consecutive sample times: sample(N) to sample(N+1) and sample(N+1) to sample(N+2).

The -ΔV threshold field values are:

CSR1 Bits							
7	6	5	4	3	2	1	0
-	ΔVT	-	-	-	-	-	-

With the following typical threshold values:

-ΔV	Min. Drop From Sample N to N+1	Min. Drop From Sample N+1 to N+2	Min. Cum. Drop From Sample N to N+2
0	0–2.5mV	0–2.5mV	2.5–5.0mV
1	2.5–5.0mV	2.5–5.0mV	7.5–10mV

Zero is the initial default.

The ***GGNV qualified charge field*** (bit 7) is programmed to 1 to force GGNV to qualify DC initiation of charge action (power switch status bit = 0). When this bit is one and the power switch status bit is 0, charge action and/or trickle charge are initiated only if the CSR2 GGNV status bit = 1. The Q field values are:

CSR1 Bits							
7	6	5	4	3	2	1	0
Q	-	-	-	-	-	-	-

Where Q is:

0 No GGNV qualification of charge action (initial default).

1 DC-initiated charge action only if GGNV = 1.

Charge Setup Register 2 (CSR2)

Charge setup register 2 (CSR2) contains four configuration fields and three status bits.

The ***gas gauge not valid*** status bit (GGNV) is set to indicate to the host processor that the gas gauge value does not reflect discharge from bq2001-determined full charge and is potentially invalid.

GGNV values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	GGNV

Where GGNV is:

0 Gas gauge value reflects discharge from bq2001-determined full charge.

1 Charge state not known; battery replaced or charge action not completed.

GGNV is set to 1 by either the start of a charge action or by battery removal. GGNV is reset to 0 on charge action termination due to -ΔV, maximum temperature, maximum voltage, or maximum time determination. GGNV may be written when charging is not occurring.

If GGNV is 1 and the power switch state bit equals 0, any discharge phase of a charge action is skipped.

The ***battery removed*** status bit (BR) indicates to the host that the battery has been removed. The battery removed bit is set to 1 if the secondary battery is removed. When the battery is replaced, this value can be written to 0. For rapid detection of battery removal, the SB input should be pulled low externally. A resistor value of 1MΩ can be used.

The BR values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	BR	-

Where BR is:

0 Battery has not been removed since last written.

1 Battery has been removed.

If BR is 1, any discharge phase of a charge action is stopped.

The ***trickle enable field*** (bit 2) is programmed to 1 to enable trickle charge. When this bit is 1, trickle charge occurs if DCV = 1 and the secondary battery is not being charged. The gas gauge is disabled when trickle charge is active.

The trickle enable field values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	T	-	-

Where T is:

0 Trickle charge disabled (initial default).

1 Trickle charge enabled.

The ***-ΔV enable field*** (bit 3) is programmed to 1 to enable -ΔV slope detection for full charge determination. When this bit is 1, a -ΔV observation is interpreted as full charge. When this bit is 0, a -ΔV observation is ignored.

The -ΔV enable field values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	ΔVE	-	-	-

Where $\overline{\Delta VE}$ is:

0 Ignore -ΔV.

1 Interpret -ΔV as full charge (initial default).

The ***temperature OK*** status bit (TOK, read only) indicates the status of temperature sensor input. If the input is below 2.18V or above 2.50V, TOK is set to 0. If the temperature input is between 2.18V and 2.50V, TOK is set to 1. When TOK is 0 and temperature enable is set, no charge action is allowed, and any active charge action stops. If selected by MR bit 3, $\overline{PO_3}$ is active when TOK =0.

The TOK values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	-	TOK	-	-	-	-

Where TOK is:

0 Temperature sensor input is below 2.18V or above 2.50V

1 Temperature sensor input is between 2.18V and 2.50V

The ***temperature enable field*** (bit 5) is set to enable temperature-qualified charging. When this bit is written to 0, no temperature limits are used.

The temperature enable field values are:

CSR2 Bits							
7	6	5	4	3	2	1	0
-	-	TE	-	-	-	-	-

Where TE is:

0 Temperature qualification disabled.

1 Temperature qualification enabled (initial default).

The ***-ΔV sample time field*** (bits 6–7) is programmed to select the time between voltage samples used to determine -ΔV. Shorter times may be chosen when a rapid charge is required and the end of charge must be detected as soon as possible. Longer times may be chosen when slow charge rates are required.

The -ΔV sample time field values are :

CSR2 Bits							
7	6	5	4	3	2	1	0
ΔVS		-	-	-	-	-	-

Where ΔVS is:

00 32 seconds between samples (initial default)

01 64 seconds between samples

10 128 seconds between samples

11 256 seconds between samples

Charge Time Register (CTR)

The read-only charge time register (CTR) contains a value that is the sum of the charge phases since the last gas gauge reset. This value is set to 0 at the completion of each charge phase, abort charge command, or on battery removal. The time unit for CTR is 256 seconds.

The CTR register is a volatile register. The data in this register will be lost when both DC and V_{CC} are removed.

Discharge Period Register (DPR)

The discharge period register (DPR) is programmed to define the optional discharge period—used for depolarization—of each charge phase interval. DPR is non-zero for burp charging. Each period may be programmed to be 0 to 255 of the 256 time segments per eight-second interval. The number of segments in the period is the same as the programmed value. The value in CPR has precedence over DPR. This means that within any eight-second interval, the charge period is completed before the discharge period is started, such that the maximum period allowed for discharge is 255 minus the CPR value.

End-of-Discharge Cell Voltage Register (EDCV)

The end-of-discharge cell voltage register (EDCV) is programmed with the value used to determine the secondary battery end-of-discharge voltage (EDV) threshold during operational or non-operational discharge. This value need not be the real single-cell voltage, but must multiply by the number of cells value in CSR1 to equal the EDV. Discharging to the EDV threshold generates an interrupt request on $\overline{INT}$, sets the status register EDVI interrupt bit, loads the value from GG into LCR, and—if selected—activates $\overline{PO_2}$.

Example:

For a voltage of 1.0V per cell, the value placed in EDCV should be 69H.

Gas Gauge Registers (GGL and GGH)

The read-only gas gauge register pair (GGL and GGH) indicates the charge that has been removed from the battery. The GG value is interpreted by:

$$GG = S_R(\Omega) \times \text{Removed Charge (mAh)} \times 47$$

The gas gauge register pair is reset to 0 by:

- Charge action termination due to negative delta voltage, maximum temperature, maximum charge time, or maximum voltage determination, any of which indicates full charge.
- An abort charge actions command written to CMR (only if the power switch state bit = 1).
- Battery removal.

Gas Gauge Threshold Registers (GGTL and GGTH)

The gas gauge threshold register pair (GGTL and GGTH) is programmed to set the gas gauge threshold. At initiation of a charge action, this limit may determine the discharge phase activity (see CSR1, charge action selection field). Reaching this limit generates an interrupt request on $\overline{INT}$ (V_{CC} valid), sets the status register gas gauge interrupt bit and—if selected—activates $\overline{PO_5}$.

The gas gauge counter may need to count at least one-half count to or beyond this threshold for the status to change. Rewriting the threshold to transition from equal/above-to-below or below-to-equal/above will be recognized on or before the next half gas gauge count.

Last Capacity Registers (LCRL and LCRH)

The read-only last capacity register pair (LCRL and LCRH) is used to keep a copy of the most recently measured battery capacity. LCR is automatically loaded with the gas gauge value when the EDV threshold is reached.

Maximum Cell Voltage Register (MCV)

The maximum cell voltage register (MCV) is programmed to define the maximum voltage per cell limit. This is one of four determinants of full charge. If the maximum voltage is reached before the -ΔV determination, maximum temperature, or maximum charge time is obtained, then the charge action is terminated, and the gas gauge and GGNV are reset. The MCV value need not be the real single-cell voltage, but—with the number of cells value in CSR1—defines the maximum battery voltage.

Maximum Charge Time Register (MCT)

The maximum charge time register (MCT) is programmed to define the maximum time for the charge phase of a charge action. This is one of four determinants of full charge. If this time value is reached before the -ΔV determination, maximum temperature, or maximum battery voltage is obtained, then the charge action is terminated and the gas gauge and GGNV are reset. The units for this register are 256 seconds, for a maximum time of 18 hours.

Mask Register (MR)

The mask register (MR) is programmed to specify each output pin—$\overline{PO_1}$ to $\overline{PO_6}$—to be controlled by a specific bq2001 status or by a specific bit of the output control register (OCR). Each of these open drain output pins can be set up to follow internally generated status or to reflect bits set by the host processor. See Table 6.

Output Control Register (OCR)

The output control register (OCR) may be used by the host processor to activate any of the outputs $\overline{PO_1}$ to $\overline{PO_6}$. $\overline{PO_1}$ to $\overline{PO_6}$ reflect the status of OCR bits 1 to 6, respectively (1 = output active), provided that host control is enabled by writing the appropriate masking bit in the mask register, MR, to 0. See Table 6.

Table 6. Mask Register

Bit	Value	Result
0	0	This bit is always 0.
	1	Not available.
1	0	$\overline{PO_1}$ is low when OCR bit 1 = 1.
	1	$\overline{PO_1}$ is low when SR charging bit = 1.
2	0	$\overline{PO_2}$ is low when OCR bit 2 = 1.
	1	$\overline{PO_2}$ is low when the secondary battery voltage is at or below the EDV threshold defined by the CSR1 number of cells field value and the EDCV register value.
3	0	$\overline{PO_3}$ is low when OCR bit 3 = 1.
	1	$\overline{PO_3}$ is low when CSR2 TOK bit = 0.
4	0	$\overline{PO_4}$ is low when OCR bit 4 = 1.
	1	$\overline{PO_4}$ is low when SR DC valid bit = 1.
5	0	$\overline{PO_5}$ is low when OCR bit 5 = 1.
	1	$\overline{PO_5}$ is low when the gas gauge reaches or exceeds the programmed gas gauge threshold.
6	0	$\overline{PO_6}$ is low when OCR bit 6 = 1.
	1	$\overline{PO_6}$ is low when SR secondary battery fault bit = 1.
7	0	Undefined.
	1	Undefined.

OCR also contains the EEPROM program bit and a reserved bit.

The ***program*** bit (PGM) enables the EEPROM programming feature of the EMU. When PGM is written to 1, data must be written only to the 12 programmable bytes of the control and status registers. (See Listing 1.)

The ***reserved*** bit must remain 0 for normal device operation. Device operation may be permanently impaired if the reserved bit is 1 during EEPROM programming.

Status Register (SR)

The read-only status register (SR) indicates the status of various battery operations and conditions. The bits are defined in Table 7.

Table 7. Status Register

SR Bit	Bit Name	If Set to 1
0	PSI	Power switch interrupt
1	CHG	Charging
2	EDVI	End-of-discharge voltage interrupt
3	BCL	Backup cell low
4	DCV	DC valid
5	GGI	Gas gauge interrupt
6	SBF	Secondary battery fault
7	PS	Power switch state ON

Power switch interrupt (PSI) is set when $\overline{PS}$ goes low. PSI is reset to 0 when the SR byte is read.

Charging (CHG) is set whenever a charge action is in progress. CHG equals 0 during no action or during trickle charge.

End-of-discharge voltage interrupt (EDVI) is set when the secondary battery voltage falls to or goes below the threshold defined by the CSR1 number of cells field value and the EDCV register value. EDVI is reset to 0 when SR is read.

Backup cell low (BCL) is set to indicate low backup cell voltage. If the voltage at BC_I is less than or equal to 2.2 (± 0.1)V, then BCL is set to 1. Otherwise this bit is 0.

DC valid (DCV) is set to indicate valid DC. The bit is set to 1, allowing charge action to occur, if DC is greater than 2.5V. The bit is set to 0 whenever DC is invalid. If this bit is 0, no charge action may occur.

Gas gauge interrupt (GGI) is set when the gas gauge reaches or exceeds the programmed gas gauge threshold. GGI is reset to 0 when SR is read.

Secondary battery fault (SBF) is set to indicate a possible open or short cell. This bit is set to 1 if the voltage monitored at SB is typically less than 0.5V times the number of cells defined in CSR1. If this bit is set, no charge action will occur. The CSR1 number-of-cells value must be ≥3 for SBF to be detected.

Power switch state (PS) indicates $\overline{PSC}$ status. This bit is set to one by a $\overline{PS}$ input that activates $\overline{PSC}$ and reset to 0 by execution of the CMR power-off command to deactivate $\overline{PSC}$. The application may need to ensure that the power switch state bit reflects the system power status.

Trickle Period Register (TPR)

The trickle period register (TPR) is programmed to define the charge period during trickle charge. This register is used following full charge determination to provide a lower effective current for charge maintenance. The trickle period may be programmed to be 1 to 256 of the 256 time segments per 8-second interval. The charge period is one plus the programmed value. The programmed value may be 0 to 255.

TPR examples include:

TPR	Result
7	Provides for an average current of about 1/32 of the continuous charge current.
0	Provides for an average current of 1/256 of the continuous charge current.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{DC}	DC voltage applied on DC relative to V_{SS}	-0.3 to 18	V	
V_{SB}	DC voltage applied on SB relative to V_{SS}	-0.3 to 18	V	
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_{BCI}	DC voltage applied on BCI relative to V_{SS}	-0.3 to 7.0	V	
V_{OP}	DC voltage applied on all open-drain outputs relative to V_{SS} except CC and $\overline{INT}$	-0.3 to 18	V	
V_{PMP}	DC voltage applied on CC output relative to V_{SS}	-0.3 to 36	V	
V_{SR}	DC voltage applied on S_R relative to V_{SS}	-0.3 to 18	V	$V_{SR} \leq V_{SB} + 0.4$
V_{IF}	DC voltage applied on $\overline{DS}$, RS, DQ, and $\overline{INT}$ relative to V_{SS}	-0.3 to 7.0	V	
V_{PS}	Power switch input	-0.3 to 18	V	
V_{TS}	Temperature/V_{PP} input	-0.3 to 16	V	
I_{BC}	Output current on BC	2	mA	
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-10 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (1 of 2) (T_A = 0 to 70°C)

Symbol	Parameters	Minimum	Typical	Maximum	Unit	Notes
V_{DC}	DC supply voltage	5.5	-	18	V	
V_{SB}	SB supply voltage	3.0	-	18	V	
V_{CC}	V_{CC} supply voltage	4.5	5.0	5.5	V	
V_{BCI}	BCI supply voltage	2.0	-	6.0	V	
V_{BC}	BC output supply voltage	V_{BCI} - 0.3	V_{BCI}	V_{BCI} + 0 .1	V	Regulated $V_{SB} > V_{BCI}$; $0 < I_{BC} < 1mA$
		V_{BCI} - 0.3	-	V_{BCI}	V	Regulated $V_{SB} < V_{BCI}$; $0 < I_{BC} < 1mA$

Continued on next page.

Recommended DC Operating Conditions (2 of 2) (T_A = 0 to 70°C)

Symbol	Parameters	Minimum	Typical	Maximum	Unit	Notes
V_{REG}	V_{SB} headroom above V_{BCI} for V_{SB} to be regulated to V_{BC}	1.7	-	-	V	I_{BC} = 50µA, V_{BC} = 3V
		2.0	-	-	V	I_{BC} = 50µA, V_{BC} = 4V
		2.2	-	-	V	I_{BC} = 50µA, V_{BC} = 5V
		2.0	-	-	V	I_{BC} = 1mA, V_{BC} = 3V
		2.2	-	-	V	I_{BC} = 1mA, V_{BC} = 4V
		2.4	-	-	V	I_{BC} = 1mA, V_{BC} = 5V
V_{SS}	Supply voltage	0	0	0	V	
V_{SR}	Sense resistor input voltage	V_{SS}	-	V_{SB} + 0.3	V	
V_{IL}	Logic low-level input voltage for $\overline{DS}$, RS, DQ	-0.3	-	0.8	V	
V_{IH}	Logic high-level input voltage for $\overline{DS}$, RS, DQ	2.2	-	V_{CC} + 0.3	V	
V_{OL}	Logic low-level output voltage for DQ	-	-	0.4	V	I_{OL} = 4.0mA
V_{OH}	Logic high-level output voltage for DQ	2.4	-	-	V	I_{OH} = -2.0mA
V_{OCC}	Charge control output voltage	-	-	36	V	I_{OCC} = 0
V_{OD}	Open-drain output voltage	-	-	18	V	All open-drain outputs other than CC and $\overline{INT}$, high-impedance state
I_{OD}	Open-drain sink current for $\overline{PO_1}$–$\overline{PO_6}$, CD, $\overline{PSC}$, $\overline{INT}$	-	-	5	mA	V_{OD} = 1.0V
I_{OCC}	Open-drain sink current for CC	-	-	0.5	mA	V_{OCC} = 1.0V
I_{LI}	Input leakage current for $\overline{DS}$, RS	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current for DQ	-	-	± 1	µA	DQ in high impedance
I_{CC}	Operating current, V_{CC} supply	-	0.7	2.0	mA	
I_{DC}	Operating current, DC supply	-	2	3	mA	
I_{CCDR}	Data-retention current from BC_I input	-	0.1	1	µA	I_{BC} = 0
I_{CCSR}	Data-retention current from S_R input	-	40	100	µA	I_{BC} = 0
I_{BC}	Output current on BC	-	-	1	mA	V_{BC} = 3.0V, T_A = 25°C
V_{OFF}	Offset voltage measured from SB to S_R with zero current flowing through the sense resistor	-3.3	-2.8	-2.3	mV	T_A = 25°C
V_{ILPS}	Logic low-level input voltage for $\overline{PS}$	-0.3	-	0.4	V	
V_{IHPS}	Logic high-level input voltage for $\overline{PS}$	1.5	-	18	V	
V_{PP}	EEPROM programming voltage	15	-	16	V	
I_{PP}	EEPROM programming current	-	-	3.0	mA	

DC Thresholds

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{SBF}	Secondary battery fault	0.4 x N	0.5 x N	0.6 x N	V	N = number of cells per CSR1; 10–40mV per cell hysteresis
V_{MAXC}	Maximum charge voltage	MCV x (0.95 x N)	MCV x N	MCV x (1.05 x N)	V	N = number of cells per CSR1
V_{EDV}	End-of-discharge voltage	EDCV x (0.95 x N)	EDCV x N	EDCV x (1.05 x N)	V	N = number of cells per CSR1; 10–40mV per cell hysteresis
V_{BCL}	Backup cell low voltage	2.0	2.2	2.3	V	10–40mV hysteresis
V_{DCV}	DC valid voltage (min.)	2.4	2.5	2.6	V	10–40mV hysteresis
V_{TSH}	Temperature OK high/ maximum charge temperature	2.46	2.50	2.54	V	
V_{TSL}	Temperature OK low	-	V_{TSH} - 0.32	-	V	10–40mV hysteresis

Note: Typical values indicate operation at T_A = 25°C.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{SB}	SB input resistance	850	1100	1350	KΩ	V_{CC} or DC valid

Notes: Typical values indicate operation at T_A = 25°C.
This parameter is sampled and not 100% tested.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Logic input/output capacitance (DQ)	-	-	10	pF	$V_{I/O}$ = 0V
C_{IN}	Logic input capacitance ($\overline{DS}$, RS)	-	-	8	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load for DQ (including scope and jig)	See Figures 7 and 8
Output load for all open-drain outputs except CC	See Figure 9

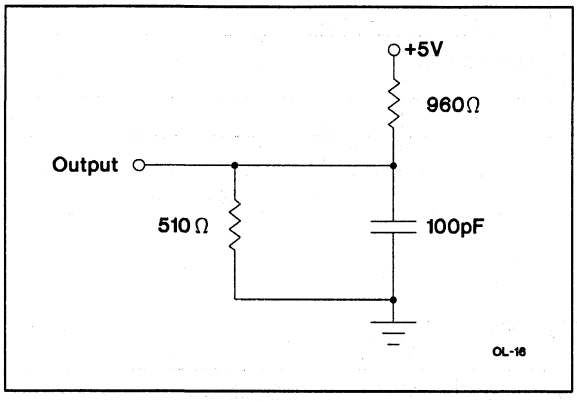


Figure 7. Output Load A

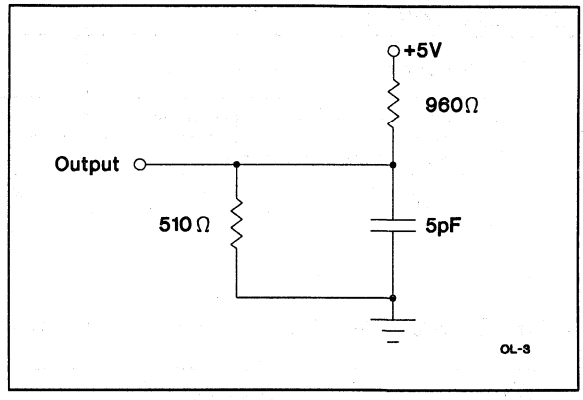


Figure 8. Output Load B

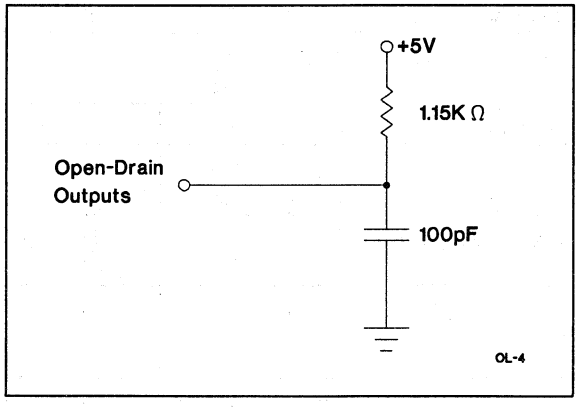


Figure 9. Output Load C

Status Timing (T_A = 0 to 70°C)

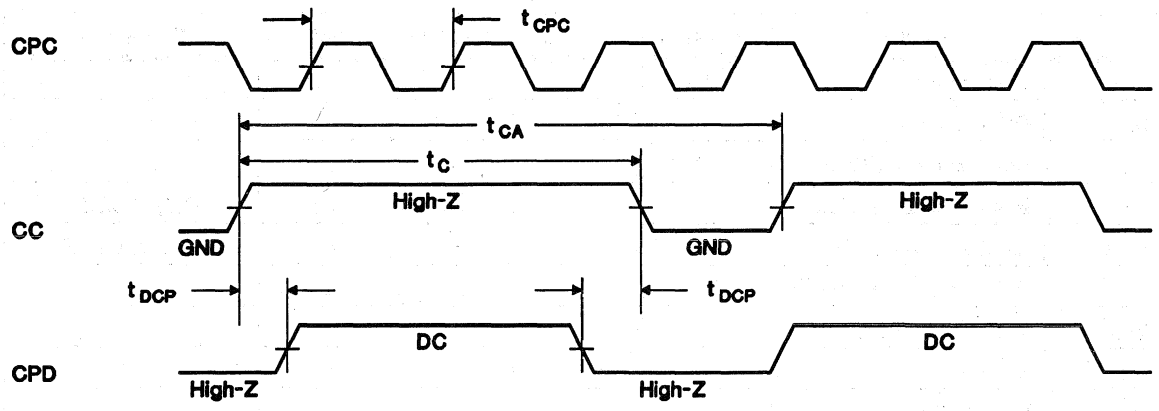
Status	Minimum	Maximum	Units	Conditions
Start charge	-	0.5	ms	
Abort charge	-	0.5	ms	
EDV to EDVI active	-	4	ms	
MCV to charge termination	-	4	ms	
Maximum temperature to charge termination	-	4	ms	
Battery removed to BR set	-	1	µs	
Battery fault to SBF set/cleared	-	1	µs	
DC valid to DCV set	-	1	µs	
GGT to GGI active	-	½ gas gauge count	-	
$\overline{PS}$ to PSI active (system power status off)	-	1	µs	
$\overline{PS}$ to PSI active (system power status on)	-	50	ms	
$\overline{PS}$ debounce period	30	-	ms	PS status bit = 1

Charge Action Timing (T_A = 0 to 70°C, DC = 4.5V to 18V)

Signal	Characteristic	Minimum	Typical	Maximum	Units
t_{DCS}	DC slew rate 0V to operational	-	-	18	mV/µs
t_{CPC}	Charge pump time	14.0	15.3	16.5	µs
t_{DCP}	CPD transition to CC transition	30	60	120	ns
t_{DTC}	Discharge phase to charge phase transition time	$\frac{t_{CA}}{512}$	-	-	µs
t_{CA}	Charge action interval	7.3	8	8.7	s
t_C	Charge period	$\frac{t_{CA}}{256}$	-	t_{CA}	s
t_I	Charge period to discharge period transition time	-	$\frac{t_{CA}}{512}$	-	s
t_D	Discharge period	0	-	$\left(t_{CA} \times \frac{255}{256}\right) - t_C$	s
t_T	Trickle charge period	$\frac{t_{CA}}{256}$	-	t_{CA}	s

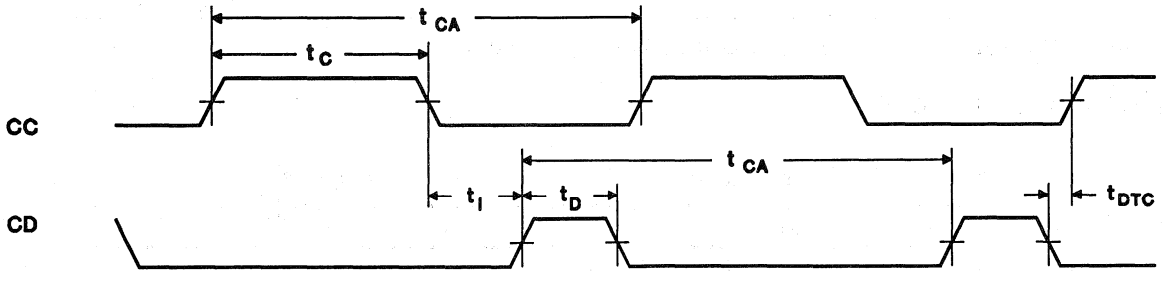
Note: Typical values indicate operation at T_A = 25°C.

Charge Pump Timing



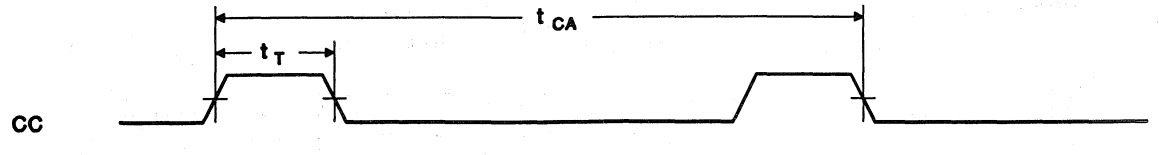
CC-1.1

Charge Action Timing



CC-2

Trickle Charge Timing



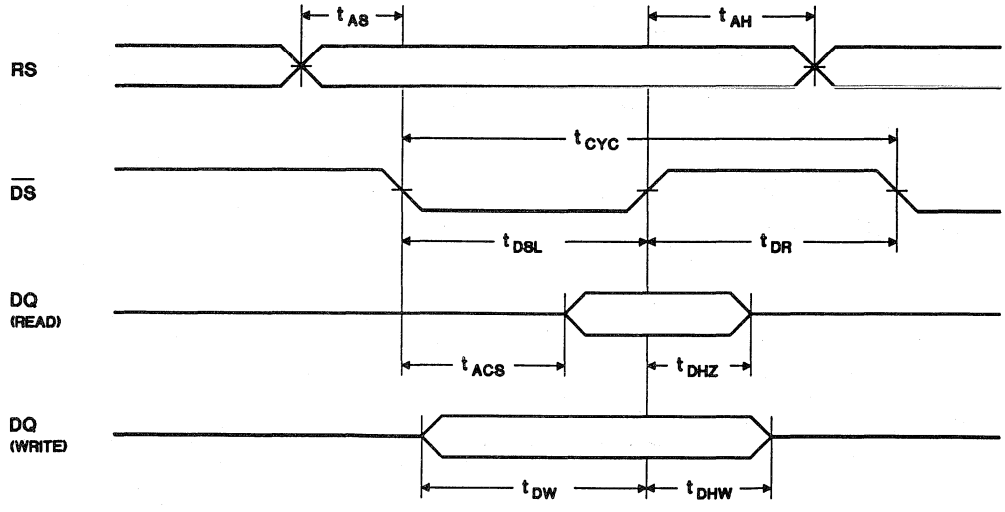
CC-3

Bus Timing (T_A = 0 to 70°C, V_{CC} = 5V± 10%)

Signal	Characteristic	Minimum	Typical	Maximum	Unit	Conditions
t_{CYC}	Cycle time	250	-	-	ns	
t_{DR}	$\overline{DS}$ recovery time	155	-	-	ns	
t_{DSL}	Data strobe low time	80	-	-	ns	
t_{ACS}	Read data access time	-	-	30	ns	Output load A
t_{DHZ}	Read data to high Z	0	-	30	ns	Output load B
t_{DW}	Write data setup time	40	-	-	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	RS setup time	0	-	-	ns	
t_{AH}	RS hold time	0	-	-	ns	
t_{INIT}	Register initialization time	-	-	50	ms	After application of V_{CC} or DC following absence of all power; registers and RAM inaccessible until completed.

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5.0V.

Read/Write Timing



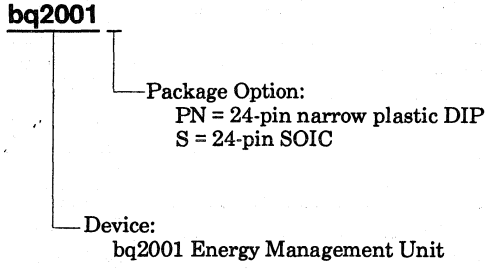
RC-8.1

Data Sheet Revision History

Change #	Page No.	Description	Nature of Change
1	2-5, 2-17	Gas gauge threshold indication	Clarification
1	2-7, 2-17	Removed charge formula denominator	Was 46; is 45
1	2-8, 2-10	Maximum temperature full-charge determination	Addition
1	2-14	EDCV, MCV increment size	Was 10mV; is 9.5mV
1	2-14	CTR, MCT increment size	Was 8 minutes; is 4.25 minutes
1	2-15	-ΔV threshold selections	Was 4–12/8–16mV; is 2.5–5.0/7.5–10.0mV
1	2-17	-ΔV sample time selections	Was 8, 32, 128, 512; is 32, 64, 128, 256
1	2-20	Absolute maximum V_{SR}–V_{SB}	Was 0.7V, is 0.4V
1	2-21	V_{OFF} from SB to S_R	Addition
1	2-21	$V_{REGULATE}$ headroom, V_{SB} above V_{BCI}	Addition
1	2-21	$\overline{PS}$ logic-level input voltages	Addition
1	2-22	Hysteresis	Clarification
1	2-22	SB impedance	Change
1	2-24	Status timing	Addition
2	2-3, 2-6	$\overline{INT}$ active on application of V_{CC}	Addition
2	2-4, 2-24	$\overline{PS}$ debounce	Clarification
2	2-7, 2-17	Removed charge formula denominator	Was 45; is 47
2	2-8	Temperature control of charge phase	Clarification
2	2-10, 2-16	BR bit qualification of discharge-before-charge	Clarification
2	2-13	"Start charge" command sequence	Clarification
2	2-21	I_{CCSR}	Was 1 typ., 10 max.; is 40 typ., 100 max.
2	2-21	V_{OFF} from SB to S_R	Was -1.7 ("contact factory"); is -2.8
2	2-22	R_{SB}	Was 750 min., 1000 typ., 1250 max.; is 850 min., 1100 typ., 1350 max.
3	2-6, 2-17	CTR reset when gas gauge reset	Change
3	2-7	Multiple "DC-initiated" charges allowed independent of V_{CC}	Clarification
3	2-9, 2-11, 2-16	Trickle charge precedes or follows full charge when DC is valid and trickle is enabled	Change
3	2-11	PS initialized to 0 when $\overline{PS}$ is low	Clarification
3	2-21	I_{CC}	Was 400μA typ., 700μA max.; is 0.7mA typ., 2.0mA max.
4	2-7, 2-19, 2-22	Secondary battery fault (V_{SBF})	Was 0.45N V_{MIN}, 0.55N V_{MAX}; is 0.4N V_{MIN}, 0.6N V_{MAX}
5	2-7, 2-17	CTR register description	Clarification

Note: Change 1 = Aug. 1991 E changes from Apr. 1991 D.
Change 2 = Sept. 1991 F changes from Aug 1991 E.
Change 3 = Feb. 1992 G "Final" changes from Sept. 1991 F "Preliminary."
Change 4 = Aug. 1992 H changes from Feb. 1992 G.
Change 5 = Nov. 1993 I changes from Aug. 1992 H.

Ordering Information



BENCHMARQ

EV2001

Evaluation/Development System

Features

- Compact MCS51-based system controlled by any ASCII terminal
- Complete bq2001 functional evaluation and target application evaluation
- Application software development using the EM2001 software emulation library on any IBM®-compatible PC
- On-board A-to-D converter for battery characterization to determine voltage threshold values
- bq2001 EEPROM default settings programmer including 5V-to-15.5V converter
- bq2001 in a 24-pin DIP or SOIC zero-insertion-force socket
- Test points and connections for interfacing with application hardware

General Description

The EV2001 board provides an evaluation and application development environment for the bq2001 EMU™ battery-management IC. The EV2001 incorporates an 80C32 processor and firmware allowing the board to be operated across an RS-232 connection by any ASCII terminal, or any personal computer running terminal emulation software such as Kermit, PROCOMM™, Crosstalk™, Windows/Terminal™, or an equivalent.

The user provides the terminal, a 5V supply, the battery, the charging supply, and an appropriate discharge load. The full functionality of the bq2001 can be evaluated using simple "natural language" commands and responses. The EV2001 firmware "translates" between the terminal input/output and the bq2001 register data.

For IBM PC-compatible application software development, the EV2001 kit includes a PC-compatible software emulation library (EM2001) that drives the EV2001, which appears to be a bq2001, via the serial port. A simple conversion modifies the tested application code to reside in its final location.

The EV2001 includes a 5V-to-15.5V converter and supports programming of the bq2001 EEPROM default settings for either bq2001 DIP or SOIC packages. A separate 10-bit A-to-D converter digitizes the voltage of the battery under test, allowing any battery to be characterized through charge/discharge cycles. Downloading the data to the host PC allows data analysis to select the bq2001 settings appropriate to the battery.

The EV2001 hardware allows realistic evaluation of system design alternatives. Each of the six bq2001 programmable open-drain outputs shown in Figure 1 may be connected to an on-board LED or to an external connector. The battery can be discharged into the target system load. The gas gauge sense resistor (0.100Ω) may be replaced with another resistor more precisely suited to the target application discharge characteristics. For charge/discharge temperature control, an LM335 temperature sensor is provided to optionally monitor the battery temperature. Other temperature sensors may also be used.

User-supplied support hardware includes:

- An ASCII terminal (or PC using terminal emulation) or a PC-XT/AT (if using EM2001 software)
- V_{CC} system supply
- DC battery charging supply
- Battery
- System and/or discharge load

Introduction

The *EV2001 User's Guide* includes the EV2001 Hardware Guide and the EV2001 Software Guide.

The hardware guide includes:

- Board overview
- EV2001 hardware operation
- System setup procedures

The software guide includes:

- Quick-start exercise
- EV2001 embedded software (for terminal-controlled operation)

The software floppy diskette includes:

- EM2001 software emulation library (for PC-based application software development)
- DEMOT PC-based terminal emulator utility
- ORCAD- and AUTOCAD-compatible bq2001 part files
- bq2001 interface source code files for 8051, 8086, and V.25 processors.

Appendixes provide the parts and connections locator, EV2001 schematic, connector pinouts, and test points.

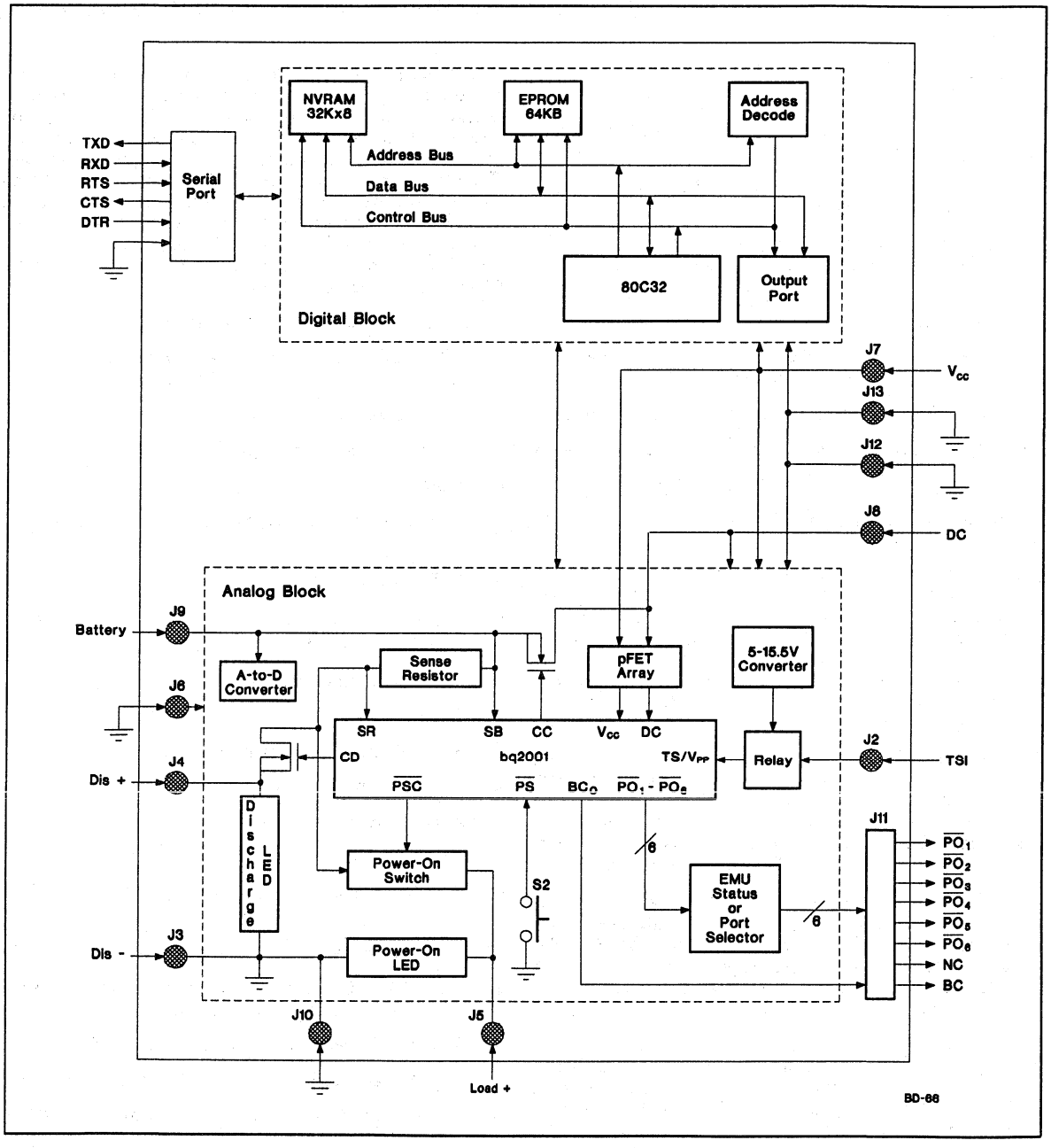


Figure 1. EV2001 Block Diagram

BENCHMARQ

bq2002

Fast Charge IC

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast charge termination by -ΔV, peak voltage detection (PVD), maximum temperature, and maximum time
- Optional top-off charge
- Selectable pulse trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002 Fast Charge IC is a low-cost CMOS battery charge controller providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002 to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002 integrates fast charge with optional top-off and pulsed trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

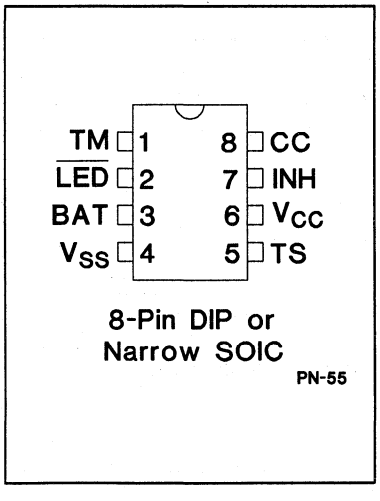
Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum temperature
- Maximum time

After fast charge, the bq2002 will optionally top-off and pulse-trickle the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002 may also be placed in low-standby-power mode to reduce system power consumption.

Pin Connections



8-Pin DIP or
Narrow SOIC

PN-55

Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	Vcc	5.0V ±20% power
BAT	Battery voltage input	INH	Charge inhibit input
Vss	System ground	CC	Charge control output

Pin Descriptions

TM **Timer mode input**

TM is a three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse trickle, and voltage hold-off time.

$\overline{LED}$ **Charging output status**

This open-drain output indicates the charging status.

BAT **Battery input voltage**

BAT is the battery voltage sense input. This potential is generally developed by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **System ground**

TS **Temperature sense input**

This input is for an external battery temperature monitoring thermistor.

V_{CC} **V_{CC} supply input**

5.0V ±20% power input.

INH **Charge inhibit input**

When high, the bq2002 suspends the fast charge in progress. When returned low, the bq2002 resumes operation at the point where initially suspended.

CC **Charge control output**

CC is an open-drain output that is used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figure 1 illustrates the charge control status during a bq2002 charge cycle. Table 1 outlines the various bq2002 operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2002 initiates a charge action by the application of power on V_{CC} or by battery replacement. Control of the charge action is then determined by the inputs from TM, TS, and BAT.

Following charge initiation, the bq2002 checks for acceptable battery voltage and temperature. If the battery voltage or temperature is outside of the fast charge limits, pulse-trickle initiates at a rate determined by the TM pin. If the battery temperature and voltage are valid at charge initiation, fast charge begins.

The bq2002 then tests for the full-charge conditions: -ΔV, PVD, maximum temperature, or maximum time.

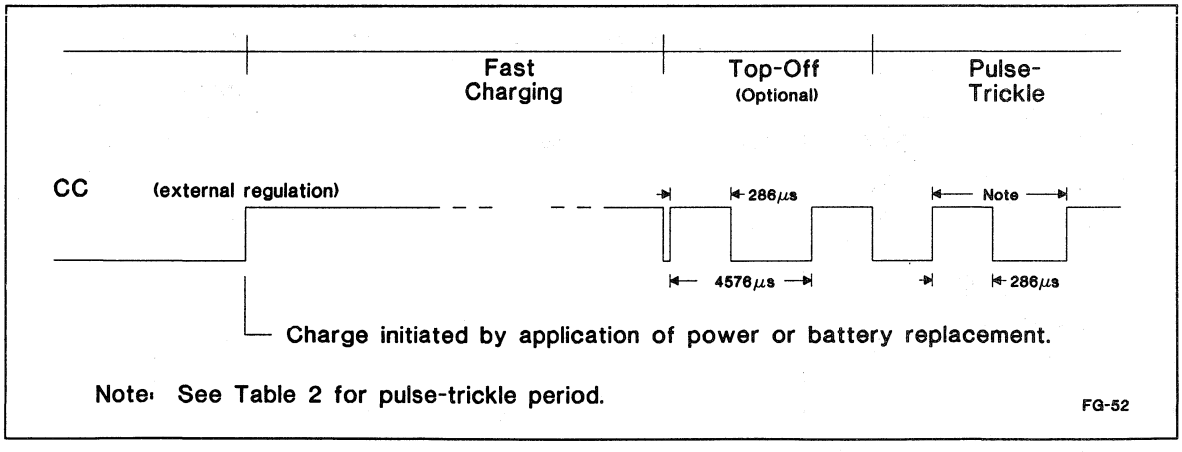


Figure 1. Example Charging Action Events

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all conditions other than fast charge. Table 1 outlines the state of the $\overline{LED}$ pin during charge.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{R1}{R2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the negative battery terminal. See Figure 2.

Note: This resistor-divider network input impedance to BAT should be above 200KΩ to protect the bq2002.

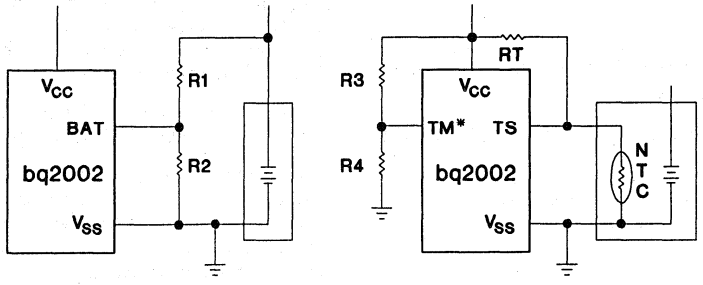
A ground-referenced negative temperature coefficient thermistor placed in close proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 2.

2

Table 1. bq2002 Operational Summary

Charge Action State	Conditions	CC Output	$\overline{LED}$
Battery absent	$V_{BAT} \geq V_{MCV}$	Trickle charge activated for period specified in Table 2	High Z
Charge initiation	V_{CC} applied, V_{BAT} drops from $\geq V_{MCV}$ to $< V_{MCV}$ (battery replaced)	–	–
Fast charging	Charge initiation occurred and $V_{TS} > V_{TCO}$ and $V_{BAT} < V_{MCV}$	High Z	Low
Charge complete	-ΔV or PVD or maximum time or maximum temperature[1]	–	–
Top-off (optional; see Table 2)	Charge complete and top-off time not exceeded and $V_{TS} > V_{TCO}$ and $V_{BAT} < V_{MCV}$[1]	Activated for 286µs of every 4290µs	High Z
Trickle	Charge complete and top-off disabled or top-off complete	Trickle charge activated for period specified in Table 2	High Z
Charge inhibit	INH high	Trickle charge activated for period specified in Table 2	Low
Low power	$V_{BAT} > V_{PD}$	High Z	High Z

Note 1: $V_{BAT} > V_{MCV}$ stops fast charge or top-off.



NTC = negative temperature coefficient thermistor.

* Mid-level - TM at V_{CC} /2 ± 0.5V.

FG-53

Figure 2. Voltage and Temperature Limit Measurement

TM Pin

The TM pin is a three-level pin used to select the various charge timer, top-off, voltage termination mode, trickle rates and voltage hold-off periods. Table 2 describes the various states selected by the TM pin. The mid-level selection input is developed by a resistor divider between VCC and ground. See Figure 2.

Charge Initiation

Application of power or battery voltage falling from above 2V initiates a charge action. If the battery is within the configured temperature and voltage limits, the bq2002 begins fast charge. The valid battery voltage range is BAT < 2V. The valid temperature range is TS > 0.5 • VCC. If the battery voltage or temperature is outside of these limits, the bq2002 pulse-trickle charges until the next valid charge initiation.

The bq2002 continues to fast charge the battery until termination by one or more of the four possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum time
- Maximum temperature (TCO)

$V_{BAT} > V_{MCV}$ stops fast charge or top-off.

Voltage Termination Hold-off

A hold-off time occurs at the start of fast charging. During the hold-off time, the PVD and -ΔV terminations are disabled (see Table 2). Once past the initial fast charge hold-off time, the PVD and -ΔV terminations are re-enabled. Maximum temperature is not affected by the hold-off period.

PVD and -ΔV Termination

The bq2002 has two modes for voltage termination depending on the state of TM. For standard -ΔV (TM = high), if V_{BAT} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated. For PVD termination (TM = low or mid), a threshold of 0 to 5mV typical is used. The PVD and -ΔV tests are valid for: 1V < BAT < 2V.

Maximum Time and Temperature

The bq2002 also terminates fast charge for maximum temperature (TCO) and maximum time. TCO reference levels provide the maximum limits for battery temperature during fast charge. If this limit is exceeded, then fast charge or optional top-off charge is terminated.

Maximum time selection is programmed using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C.

Top-off Charge

An optional top-off charge phase is selected to follow fast charge termination for 1C and C/2 rates. This may be necessary to accommodate battery chemistries that have a tendency to terminate charge prior to achieving full capacity. With top-off enabled, charging continues after fast charge termination for a period of time selected by the TM pin (see Table 2). During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This results in an average rate 1/16th that of the fast charge rate. Maximum time and temperature (TCO) terminations are the only methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged after fast charge or top off by driving the CC pin active for a period of 286µs for every 18.0ms of inactivity for 1C and 2C selections, and 286µs for every 8.86ms of inactivity for C/2 selection. This results in a trickle rate of C/64 for the top-off enabled mode and C/32 otherwise.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin of the bq2002. When high, the bq2002 suspends all fast charge and top-off activity and the internal charge timer control. Temperature detection is not affected by the INH pin. During charge inhibit, the bq2002 continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH went active.

Low-Power Mode

When BAT is driven above V_{PD}, the bq2002 assumes a low-power operational state. Both the CC pin and the $\overline{LED}$ pin are driven to the high-Z state. The operating current of the bq2002 is reduced to less than 1µA in this mode. Subsequently, when BAT returns to a value below V_{PFD}, trickle charge is initiated.

Table 2. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM	Fast Charge Top-off and Safety Time (minutes)	PVD and -ΔV Hold-Off Time (seconds)	Top-Off	Pulse-Trickle Rate	Pulse-Trickle Period (ms)
		Typical	Typical			
C/2	Mid	160	600	Y	C/64	9.14
1C	Low	80	300	Y	C/64	18.3
2C	High	40	150	N	C/32	18.3

Notes: $T_A = 25°C$, $V_{CC} = 5.0V$.

Mid = 0.5 * V_{CC}.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.5 * V_{CC}	±5%	V	$V_{TS} \leq V_{TCO}$ inhibits charge
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} > V_{MCV}$ inhibits/terminates charge

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{DET}	-ΔV, PVD detect voltage	1	-	2	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	TS < 0.5V prohibited
V_{IH}	Logic input high	0.5	-	-	V	INH
	Logic input high	V_{CC} - 0.5	-	-	V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 500mV	-	$\frac{V_{CC}}{2}$ + 500mV	V	TM
V_{IL}	Logic input low	-	-	0.1	V	INH
	Logic input low	-	-	0.5	V	TM
V_{OL}	Logic output low	-	-	0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5	-	V_{CC} - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current	-	-	250	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current	-	-	1	µA	V_{CC} = 5.1V, $V_{BAT} = V_{PD}$
I_{OL}	$\overline{LED}$, CC sink	10	-	-	mA	@$V_{OL} = V_{SS}$ + 0.8V
I_L	Input leakage	-	-	±1	µA	INH, CC, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Fast charge safety time variation	0.80	1.0	1.20	-	

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

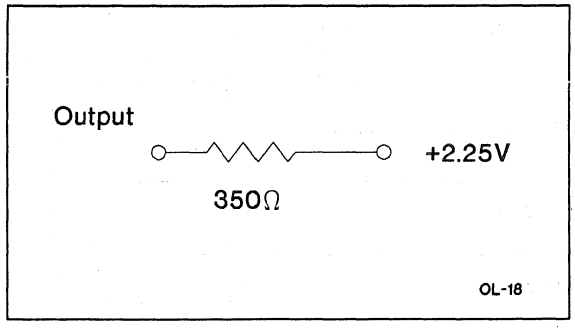
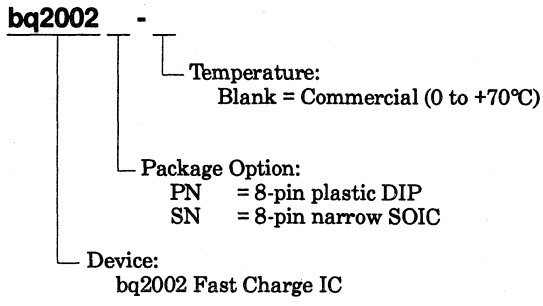


Figure 3. Output Load

Ordering Information



Preliminary **bq2002T**

Fast Charge IC With ΔT/Δt

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast charge termination by Δ temperature/Δ time, maximum temperature, and maximum time
- Optional top-off charge
- Selectable pulse trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002T Fast Charge IC is a low-cost CMOS battery charge controller providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002T to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002T integrates fast charge with optional top-off and pulsed trickle control in a single IC for charging one or more NiCd or NiMH cells.

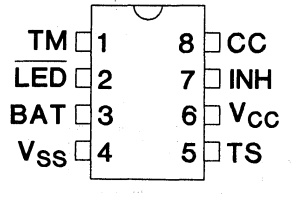
Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Delta temperature/delta time (ΔT/Δt)
- Maximum temperature
- Maximum time

After fast charge, the bq2002T will optionally top-off and pulse-trickle the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002T may also be placed in low-standby-power mode to reduce system power consumption.

Pin Connections



8-Pin DIP or
Narrow SOIC

PN-55

Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	V_{CC}	5.0V ±20% power
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

Pin Descriptions

TM **Timer mode input**

TM is a three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse trickle, and voltage hold-off time.

$\overline{\text{LED}}$ **Charging output status**

This open-drain output indicates the charging status.

BAT **Battery input voltage**

BAT is the battery voltage sense input. This potential is generally developed by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

Vss **System ground**

TS **Temperature sense input**

This input is for an external battery temperature monitoring negative temperature coefficient (NTC) thermistor.

Vcc **Vcc supply input**

5.0V ±20% power input.

INH **Charge inhibit input**

When high, the bq2002T suspends the fast charge in progress. When returned low, the bq2002T resumes operation at the point where initially suspended.

CC **Charge control output**

CC is an open-drain output that is used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figure 1 illustrates the charge control status during a bq2002T charge cycle. Table 1 outlines the various bq2002T operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2002T initiates a charge action by the application of power on Vcc or by battery replacement. Control of the charge action is then determined by the inputs from TM, TS, and BAT.

Following charge initiation, the bq2002T checks for acceptable battery voltage and temperature. If the battery voltage or temperature is outside of the fast charge limits, pulse-trickle initiates at a rate determined by the TM pin. If the battery temperature and voltage are valid at charge initiation, fast charge begins.

The bq2002T then tests for the full-charge conditions: $\Delta T/\Delta t$, maximum temperature, or maximum time.

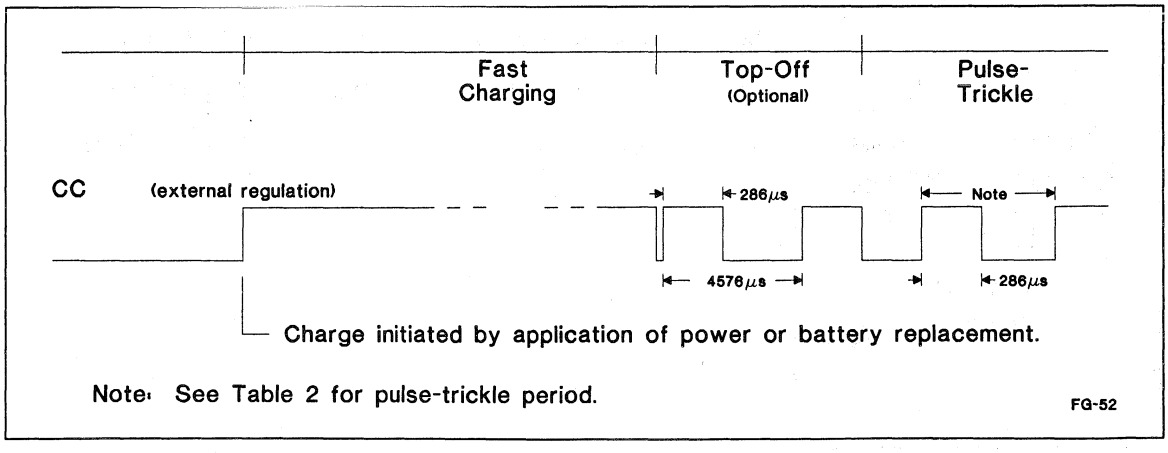


Figure 1. Example Charging Action Events

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all conditions other than fast charge pend, inhibit, or fast charge. Table 1 outlines the state of the $\overline{LED}$ pin during a charge cycle.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{R1}{R2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the negative battery terminal. See Figure 2.

Note: This resistor-divider network input impedance to BAT should be above 200KΩ to protect the bq2002T.

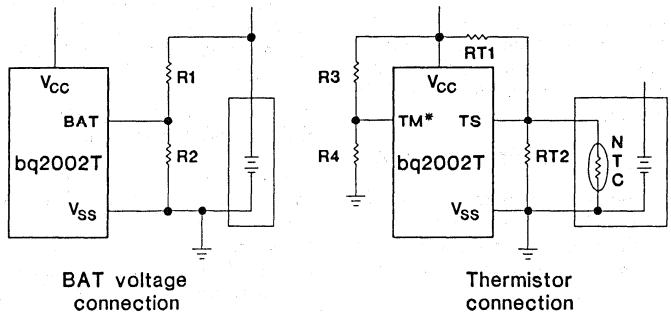
A ground-referenced negative temperature coefficient thermistor placed in close proximity to the battery should be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 2.

2

Table 1. bq2002T Operational Summary

Charge Action State	Conditions	CC Output	$\overline{LED}$
Battery absent	$V_{BAT} \geq V_{MCV}$[1]	Trickle charge activated for period specified in Table 2	High Z
Charge initiation	V_{CC} applied, V_{BAT} drops from ≥ V_{MCV} to < V_{MCV} (battery replaced)	–	–
Charge pending	Charge initiation occurred and $V_{TS} < V_{TCO}$ or $V_{TS} > V_{LTF}$	Trickle charge activated for period specified in Table 2	Low
Fast charging	Charge initiation occurred and $V_{TS} > V_{TCO}$ and $V_{BAT} < V_{MCV}$	High Z	Low
Charge complete	$\Delta T/\Delta t$ or maximum time or maximum temperature[1]	–	–
Top-off (optional; see Table 2)	Charge complete and top-off time not exceeded and $V_{TS} > V_{TCO}$ and $V_{BAT} < V_{MCV}$[2]	Activated for 286µs of every 4290µs	High Z
Trickle	Charge complete and top-off disabled or top-off complete	Trickle charge activated for period specified in Table 2	High Z
Charge inhibit	INH high	Trickle charge activated for period specified in Table 2	Low
Low power	$V_{BAT} > V_{PD}$	High Z	High Z

Notes: 1. V_{MCV} (battery presence threshold) = 2V.
2. $V_{BAT} > V_{MCV}$ stops fast charge or top-off.



NTC = negative temperature coefficient thermistor (103AT type recommended).

* Mid-level - TM at V_{CC} /2 ± 0.5V.

FG-69

Figure 2. Voltage and Temperature Limit Measurement

TM Pin

The TM pin is a three-level pin used to select the various charge timer, top-off, voltage termination mode, trickle rates and voltage hold-off periods. Table 2 describes the various states selected by the TM pin. The mid-level selection input is developed by a resistor divider between VCC and ground. See Figure 2.

Charge Initiation

Application of power or battery voltage falling from above 2V initiates a charge action. If the battery is within the configured temperature and voltage limits, the bq2002T begins fast charge. The valid battery voltage range is BAT < 2V. The valid temperature range is between the internal low-temperature fault reference (V_{LTF} = 0.4 * VCC) and the external hot-temperature fault reference (V_{HTF} = 0.25 * VCC). If the battery voltage or temperature is outside of these limits, the bq2002T pulse-trickle charges until the battery enters the valid charge range. The hot-temperature cut-off reference (V_{TCO} = 0.225 * VCC) provides hysteresis between the maximum temperature cut-off and the valid charge temperature.

The bq2002T continues to fast charge the battery until termination by one or more of the three possible termination conditions:

- Delta temperature/delta time (ΔT/Δt)
- Maximum time
- Maximum temperature (TCO)

V_{BAT} > V_{MCV} stops fast charge or top-off.

ΔT/Δt Fast Charge Termination

The bq2002T uses ΔT/Δt fast charge termination. The bq2002T makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 19 seconds typical. If V_{TEMP} is 25.6mV (typical) less than the voltage measured 60 seconds previously, the fast charge phase of the charge is terminated.

The ΔT/Δt test is valid only for:

$$0.225 * V_{CC} \leq V_{TEMP} \leq 0.4 * V_{CC}$$

Using the recommended resistor divider network and thermistor, this represents a detection threshold of 1°C/minute typical at 30°C. The valid charge temperature range corresponds to 10°C (LTF), 43°C (HTF), and 50°C (TCO), respectively.

Maximum Time and Temperature

The bq2002T also terminates fast charge for maximum temperature (TCO) and maximum time. TCO reference level (V_{TCO} = 0.225 * VCC) provides the maximum limit for battery temperature during fast charge. Once fast charge is initiated, exceeding TCO terminates fast charge or optional top-off charge.

Maximum time selection is programmed using the TM pin. Time settings are available for corresponding charge rates of C/4, 1C, and 2C.

Top-off Charge

An optional top-off charge phase is selected to follow fast charge termination for 1C and C/4 rates. This may be necessary to accommodate battery chemistries that have a tendency to terminate charge prior to achieving full capacity. With top-off enabled, charging continues after fast charge termination for a period of time selected by the TM pin (see Table 2). During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This results in an average rate 1/16the that of the fast charge rate. Maximum time and temperature (TCO) terminations are the only methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged after fast charge or top off by driving the CC pin active for a period of 286µs for every 72.9ms of inactivity for 1C and 2C selections, and 286µs for every 17.9ms of inactivity for C/4 selection. This results in a trickle rate of C/256 for the 1C rate and the C/4 rate, and C/128 for the 2C rate.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin of the bq2002T. When high, the bq2002T suspends all fast charge and top-off activity and the internal charge timer. *Fast charge termination due to maximum temperature is not affected by the INH pin.* During charge inhibit, the bq2002T continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH went active and the ΔT/Δt circuit is reset.

Low-Power Mode

When BAT is driven above V_{PD}, the bq2002T assumes a low-power operational state. Both the CC pin and the $\overline{LED}$ pin are driven to the high-Z state. The operating current of the bq2002T is reduced to less than 5µA in this mode. Subsequently, when BAT returns to a value below V_{PD}, trickle charge is initiated. A new charge cycle begins when BAT falls below 2V.

Table 2. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM	Fast Charge Top-off and Safety Time (minutes)	Top-Off	Pulse-Trickle Rate	Pulse-Trickle Period (ms)
		Typical			
C/4	Mid	320	Y	C/256	18.3
1C	Low	80	Y	C/256	73.1
2C	High	40	N	C/128	73.1

Notes: T_A = 25°C, V_{CC} = 5.0V.

Mid = 0.5 * V_{CC}.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (TA = 0 to 70°C; VCC ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.225 * V_{CC}	±5%	V	$V_{TS} \leq V_{TCO}$ inhibits charge
V_{HTF}	High-temperature fault	0.25 * V_{CC}	±5%	V	$V_{HTF} \leq V_{TS} \leq V_{LTF}$ initiates charge
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±5%	V	$V_{TS} > V_{LTF}$ inhibits charge
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} > V_{MCV}$ inhibits/terminates charge

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	TS < 0.5V prohibited
V_{IH}	Logic input high	0.5	-	-	V	INH
	Logic input high	V_{CC} - 0.5	-	-	V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 500mV	-	$\frac{V_{CC}}{2}$ + 500mV	V	TM
V_{IL}	Logic input low	-	-	0.1	V	INH
	Logic input low	-	-	0.5	V	TM
V_{OL}	Logic output low	-	-	0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5	-	V_{CC} - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002T; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current	-	-	500	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current	-	-	1	µA	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage	-	-	±1	µA	INH, TM, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Fast charge safety time variation	0.80	1.0	1.20	-	

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

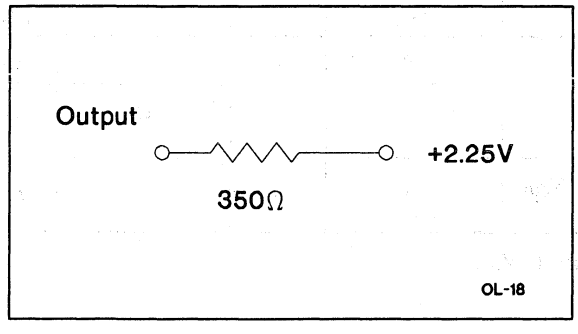
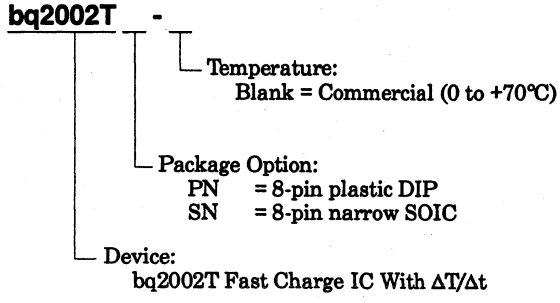


Figure 3. Output Load

Ordering Information



2

Preliminary **DV2002L2**

Fast Charge Development System

Control of LM317 Linear Regulator

Features

- bq2002/bq2002T fast charge control evaluation and development
- Charge current sourced from an on-board linear regulator (up to 1.5 A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast charge termination by negative delta voltage (-ΔV) or peak voltage detect (bq2002), ΔT/Δt (bq2002T), maximum temperature, and maximum time
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Inhibit fast charge by logic-level input

General Description

The DV2002L2 Development System provides a development environment for the bq2002/bq2002T Fast Charge IC. The DV2002L2 incorporates a bq2002 or bq2002T and a linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: -ΔV or peak voltage detect (bq2002 only), ΔT/Δt (bq2002T only), maximum temperature, maximum time, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2002L2 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off).

Please review the bq2002 or bq2002T data sheet before using the DV2002L2 board.

Connection Descriptions

JP4

TH	Thermistor connection
BAT+	Positive battery terminal
BAT–	Battery ground
GND	Ground from charger supply
DC	DC input from charger supply

JP3 NOC	Select number of cells
JP2 INH	Inhibit input
JP1 TM	Timer, etc. setting

Fixed Configuration

The DV2002L2 board has the following fixed characteristics :

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector JP4 (DC: GND).

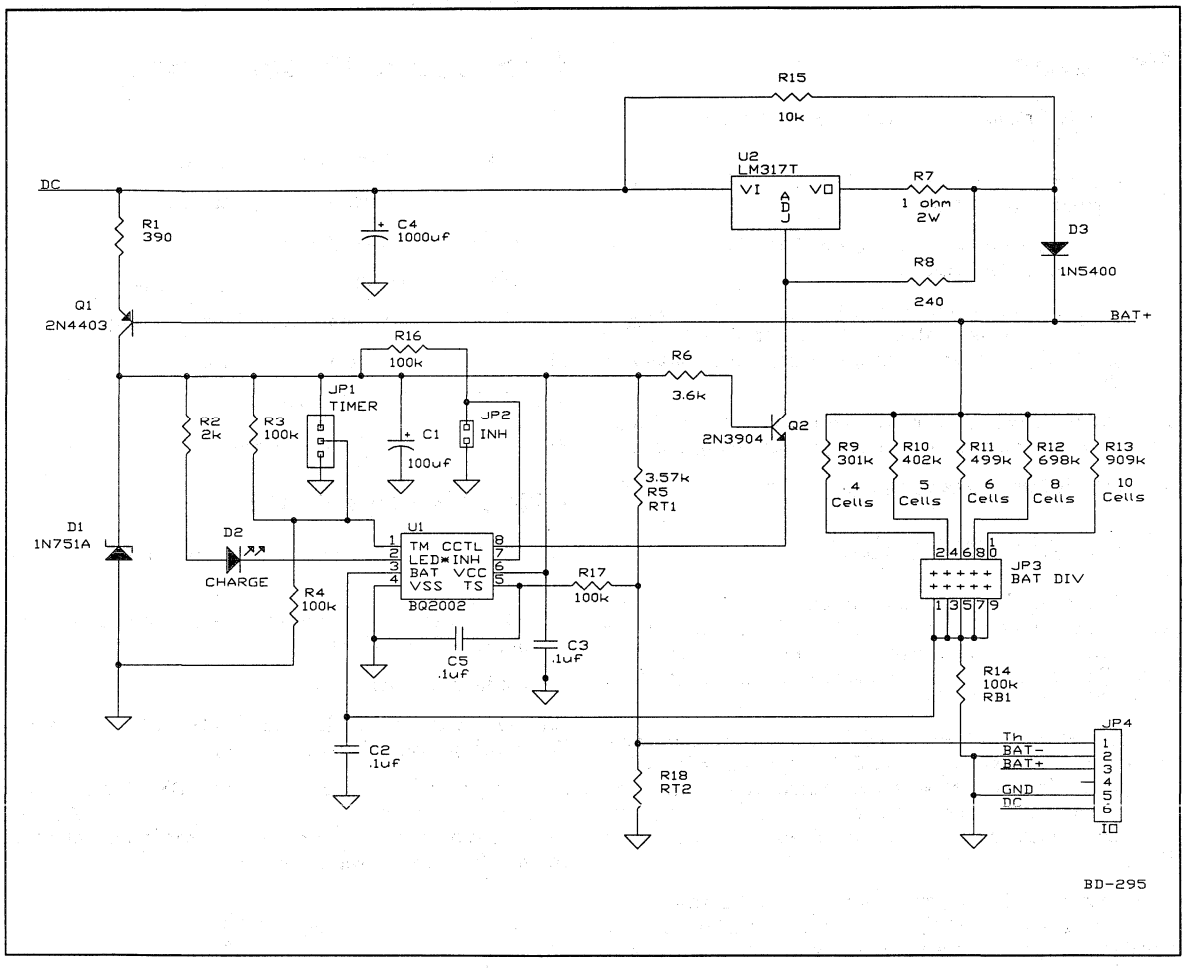
$\overline{LED}$ indicates charge status.

Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2002.

As shipped from Benchmarq, the DV2002L2 linear regulator is configured to a charging current of 1.25A. This current level is controlled by the value of sense resistor R_{SNS} by the relationship:

$$I_{CHG} = \frac{1.25V}{R_7}$$

DV2002L2 Board Schematic



bq2003

Fast Charge IC

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Flexible current regulation:
  - Frequency-modulated switching current regulator
  - Gating control for use with external regulator
- Easily integrated into systems or as a stand-alone charger
- Pre-charge checks for temperature and voltage faults
- Direct LED outputs display battery and charge status
- Fast charge termination by Δ temperature/Δ time, -ΔV, maximum temperature, maximum time, and maximum voltage
- Optional top-off charge

General Description

The bq2003 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Flexible control of constant-current or current-limited charging supply allows the bq2003 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2003-based chargers to support battery conditioning and capacity determination.

High-efficiency switched constant-current regulation is accomplished using the bq2003 as a frequency-modulated controller for switched regulation of the charging current.

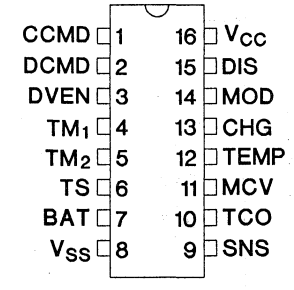
The bq2003 may alternatively be used with a transistor or SCR to gate an external charging current.

Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV)
- Maximum temperature
- Maximum time
- Maximum voltage

Pin Connections



16-Pin DIP or SOIC

PN-31

Pin Names

CCMD	Charge command/select	SNS	Sense resistor input
DCMD	Discharge command	TCO	Temperature cutoff
DVEN	-ΔV enable/disable	MCV	Maximum voltage
TM_1	Timer mode select 1	TEMP	Temperature status output
TM_2	Timer mode select 2	CHG	Charging status output
TS	Temperature sense	MOD	Charge current control
BAT	Battery voltage	DIS	Discharge control
V_{SS}	System ground	V_{CC}	5.0V ±10% power

The bq2003 uses delta temperature/delta time (ΔT/Δt) and/or negative delta voltage (-ΔV) as primary decisions for fast charge cutoff. ΔT/Δt detection is very reliable for fast charge termination for NiCd and NiMH batteries and is compatible with varying current during charge. ΔT/Δt requires the use of a single thermistor to monitor the rate of temperature increase for contacted cells. Compared to the delta temperature method (using two sensors and comparing battery temperature to ambient temperature), the ΔT/Δt approach is relatively immune to corruption when the initial battery temperature and ambient temperature are significantly different.

-ΔV detection monitors the voltage across all of the cells and is very reliable as a primary charge terminator for NiCd batteries. -ΔV detection for the bq2003 may be disabled temporarily (for periods of time when the current fluctuates) or permanently.

To provide maximum safety for the battery and system, fast charging also terminates based on a hot-temperature cutoff threshold (TCO), a safety time period, and a maximum cell voltage threshold (MCV). To avoid possible premature fast charge termination when charging batteries after long periods of storage, the maximum voltage and -ΔV tests are disabled during a short "hold-off" period at the start of charge.

The bq2003 may be configured to have one, two, or three charge stages. With a two-stage fast charge configuration, the fast charge stage controlled by the bq2003 is preceded and followed by a continuous trickle charge at a rate controlled by a current-limiting resistor outside the bq2003.

With a three-stage charge configuration, the fast charge stage is followed by a "top-off" charge stage at 1/8 the fast charge rate. This allows the battery to be quickly and safely brought to a completely full charge state. Following "top-off," externally controlled trickle charge maintains the battery at a minimal charge-sustaining level (i.e., C/40 or C/50). The maximum top-off time period is the same as for the safety time period selected for fast charge, with TCO or MCV as backup terminations.

Discharge-before-charge may be switch-selected to discharge the battery to a nominal 1V per cell (V_{EDV}) and then automatically fast charge the battery. Discharge-before-charge on demand provides conditioning services (useful to correct or prevent the NiCd voltage depression, or "memory," effect) and capacity-determining services (discharge to empty to calibrate battery capacity).

Charger status is indicated by readily distinguishable LED patterns showing:

- Charge pending
- Discharge
- Fast charge in progress
- Charge complete
- Battery removed or charge aborted

Cold or hot temperature faults are indicated by the temperature LED.

Figure 1 shows a block diagram of the bq2003 Fast Charge IC.

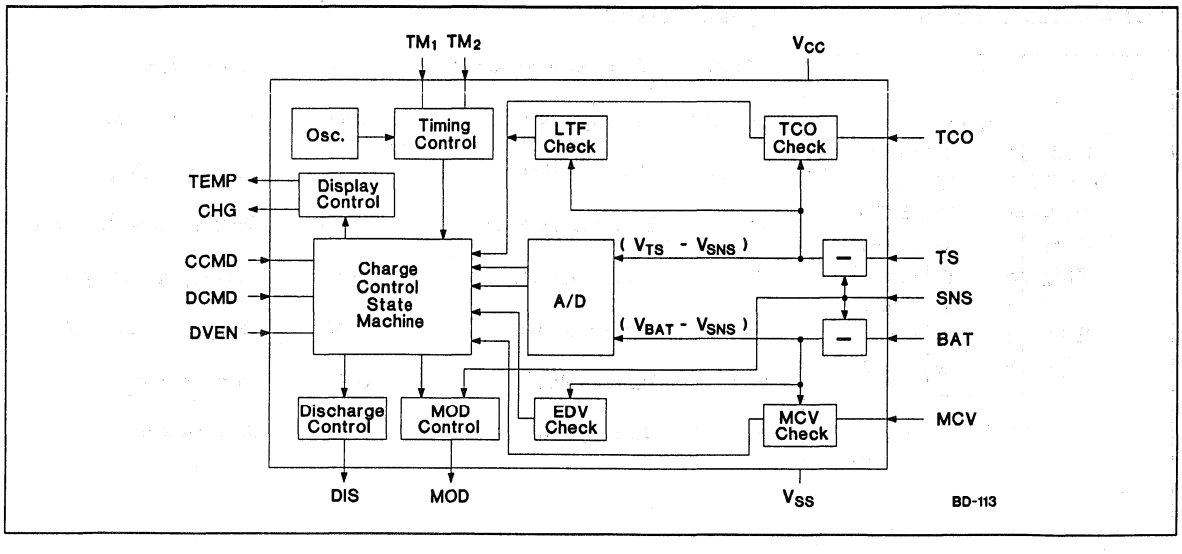


Figure 1. Block Diagram

Pin Descriptions

BAT **Single-cell voltage input**

Single-cell voltage for the battery pack being charged. This is generally developed by a high-impedance resistor divider network connected between the positive and the negative terminals of the battery.

MCV **Maximum-Cell-Voltage threshold input**

Maximum single-cell voltage. If the difference in potential between BAT and SNS (pins 7 and 9) is greater than or equal to the voltage at the MCV input, then all charging activity is inhibited. (See Figure 3.)

Note: For valid device operation, the voltage level on MCV must not exceed 0.6 * V_{CC}.

TS **Temperature sense input**

Input for external battery temperature monitoring thermistor. $\Delta T/\Delta t$ determination is valid only for $V_{TCO} \leq V_{TS} \leq V_{TCO} + 0.2\ V_{CC}$.

TCO **Temperature cutoff threshold input**

Maximum allowable battery temperature voltage. If the potential between TS and SNS (pins 6 and 9) is less than the voltage at the TCO input, then any fast charging or "top-off" charging is terminated. (See Figure 3.)

CCMD, DCMD **Charge initiation and discharge-before-charge control inputs**

These two pins control charge initiation and discharge-before-charge. When both CCMD and DCMD pins are connected to V_{CC} or when both are connected to V_{SS}, charge automatically initiates on battery replacement or when V_{CC} is applied. Charge is also initiated by: (1) a rising edge to V_{CC} at CCMD if both CCMD and DCMD are connected to V_{SS}, or (2) a falling edge to V_{SS} at CCMD if both CCMD and DCMD are connected to V_{CC}.

Discharge-before-charge is initiated at any time by: (1) a rising edge to V_{CC} at DCMD if both DCMD and CCMD are connected to V_{SS}, or (2) a negative-going pulse (from V_{CC} to V_{SS} and then back to V_{CC}) at DCMD if both DCMD and CCMD are connected to V_{CC}.

DVEN **-ΔV enable input**

This input controls the -ΔV charge termination test. If DVEN is high, the -ΔV test is enabled. If DVEN is low, -ΔV test is disabled. DVEN may change state at any time.

DIS **Discharge FET control output**

Push-pull output used to control an external transistor to discharge the battery before charging. DIS is active high.

TEMP **Temperature status output**

Push-pull output indicating temperature status. TEMP is low if the temperature input voltage at the TS pin is not within the acceptable temperature window to initiate fast charging.

CHG **Charging status output**

Push-pull output indicating charging status. See Table 1, bq2003 Operational Summary, for output pattern details.

TM_1, TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-level inputs that control the settings for fast charge safety timer and "top-off" enable/disable. See Table 2 for details.

MOD **Current-switching control output**

MOD is a push/pull output that is used to control the charging current to the battery. MOD switches high to enable charging current flow and low to inhibit charging current flow.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor. This provides the reference potentials for both the TS and BAT pins (pins 6 and 7).

If SNS is connected to V_{SS}, MOD switches high at the beginning of charge and low at the end of charge.

V_{CC} **V_{CC} supply input**

5.0 V, ±10% power input.

V_{SS} **Ground**

Functional Description

Figure 2 illustrates charge control and display status during a bq2003 charge cycle. Table 1 outlines the various bq2003 operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2003 charge action is controlled by inputs from the CCMD, DCMD, and DVEN input pins and from the TM_1 and TM_2 programming input pins.

The bq2003 controls the initiation of a charge action, checks for acceptable battery temperature (between LTF—low temperature fault and HTF—high temperature fault) and voltage (between EDV—end-of-discharge voltage and MCV—maximum cell voltage), and performs any required discharge-before-charge operation prior to fast charging. Once fast charging is initiated, the bq2003 tests for the full charge conditions: delta temperature/delta time ($\Delta T/\Delta t$) and/or negative delta voltage ($-\Delta V$), with temperature cut-off (TCO), time, and voltage safety terminations.

Charge Status Indication

Charge status is indicated by the CHG output. The CHG output may be connected directly to an LED indicator. The various charge action states and associated CHG output patterns are described in Table 1.

Temperature status is indicated by the TEMP output. The TEMP output may be connected directly to an LED indicator. TEMP is in the high state whenever battery temperature is within the temperature window defined

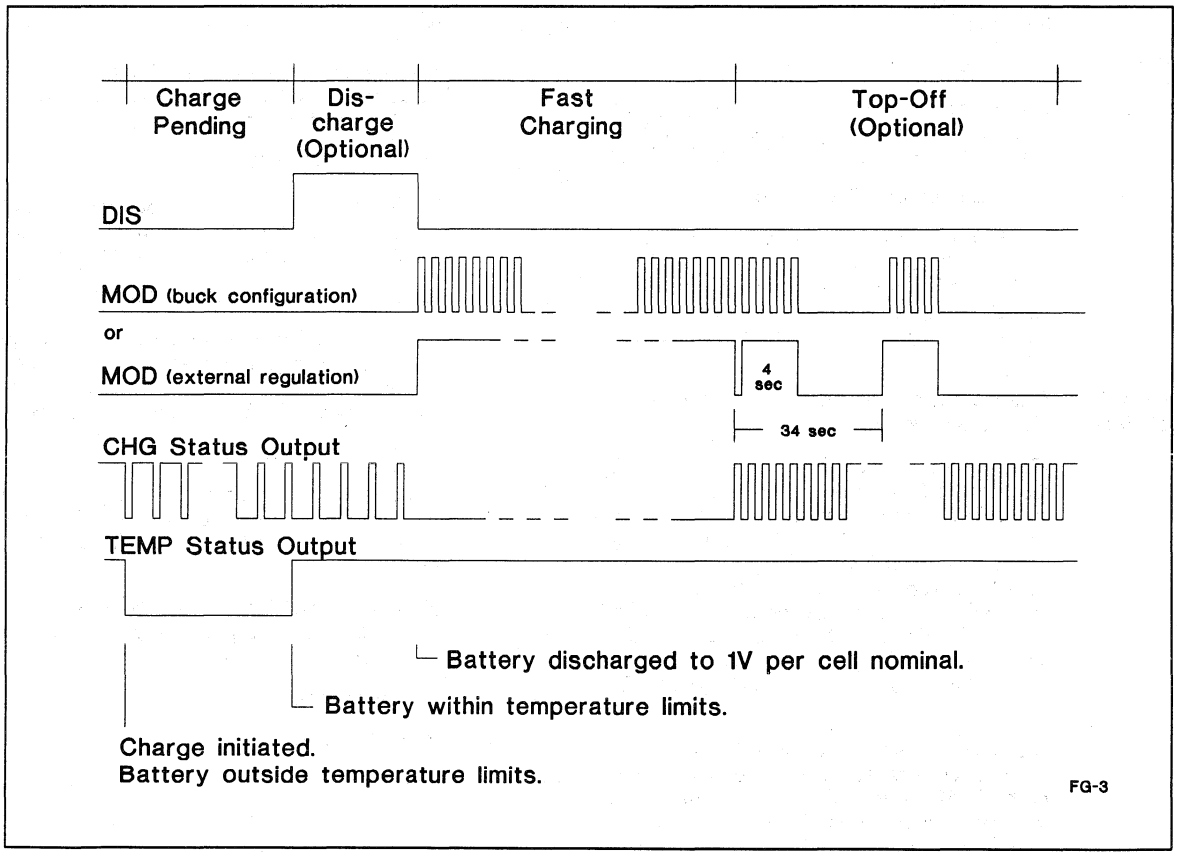


Figure 2. Example Charging Action Events

by the V_{LTF} and V_{HTF} temperature limits. When the battery temperature is outside these limits, TEMP is in the low state, as indicated in Table 1.

In all cases, if the battery voltage at the BAT pin exceeds the voltage threshold at the MCV pin, both CHG and TEMP outputs are held high regardless of other conditions.

Table 1. bq2003 Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output	CHG Status Output	
				Low	High
Battery absent/abort	V_{CELL}[1] ≥ V_{MCV}	Low	Low	-	Continuous
Charge initiation	(1) CCMD = V_{SS} and V_{CC} applied or V_{CELL} drops from ≥ V_{MCV} to < V_{MCV} (battery insertion) or (2) CCMD = V_{CC} and low-going pulse applied to CCMD	Low	Low	-	Continuous
Discharge-before-charge initiation (optional)	DCMD low-to-high transition	Low	Low	-	Continuous
Pending	Initiation occurred and V_{TEMP}[2] ≥ V_{LTF} or V_{TEMP} ≤ V_{HTF} or V_{CELL} < V_{EDV}	Low	Low	1/8 sec	1 3/8 sec
Discharging (optional)	Discharge-before-charge initiation and V_{HTF} < V_{TEMP} < V_{LTF} and V_{EDV} < V_{CELL} < V_{MCV}	Low	High	1 3/8 sec	1/8 sec
Fast charging	Initiation occurred and V_{HTF} < V_{TEMP} < V_{LTF} and V_{EDV} ≤ V_{CELL} < V_{MCV}	Low if V_{SNS} > 250mV, nominal; high if V_{SNS} < 220mV, nominal	Low	Continuous	-
Charge complete	-ΔV ≥ 12mV nominal or $\Delta V_{TEMP}/\Delta T$ > 14mV/minute or V_{TEMP} < V_{TCO} or maximum time or maximum voltage	Low	Low	1/8 sec	1/8 sec
Top-off (optional; see Table 2)	Charge complete and top-off time not exceeded and V_{TEMP} > V_{TCO} and V_{CELL} < V_{MCV}	Activated per V_{SNS} (see fast charging state) for 4 sec of every 34 sec	Low	1/8 sec	1/8 sec
Temperature State	**Conditions**	**TEMP Status Output**			
Temp fault	V_{TEMP} ≤ V_{HTF} or V_{LTF} ≤ V_{TEMP}	Low		-	
Temp OK	V_{HTF} < V_{TEMP} < V_{LTF}	-		High	

Notes: 1. V_{CELL} = V_{BAT} - V_{SNS}.
2. V_{TEMP} = V_{TS} - V_{SNS}.

Battery Voltage and Temperature Measurement

Battery voltage and temperature are monitored for maximum and minimum allowable values. The bq2003 requires that the thermistor used for temperature measurement have a negative temperature coefficient. See Figure 3.

The per-cell voltage for a battery containing N cells is defined by the resistor divider ratio:

$$\frac{R_1}{R_2} = N\text{-}1$$

where r_1 is the resistor connected to the positive battery terminal, and r_2 is the resistor connected to the negative battery terminal.

External Trickle Resistor

An external trickle resistor serves two purposes in the charging system. First, it supplies a high-voltage reference that allows the bq2003 to detect a battery insertion. Second, it supplies a small amount of trickle current to the battery that can be used to condition a deeply discharged battery for charging or maintain the charge state of a fully charged battery.

Temperature and Voltage Prequalifications

Discharge and charge are both prequalified by battery temperature and voltage. For discharge and charge to be performed, the battery temperature and voltage must fall within predetermined acceptable limits.

V_{CELL} (V_{BAT} - V_{SNS}) is compared to an internal low-voltage reference, V_{EDV} (0.2 * V_{CC}), which is the minimum acceptable battery voltage for fast charging.

V_{TEMP} voltage is compared to the internal lowtemperature reference, V_{LTF} (0.4 * V_{CC}) and the internal hot-fault temperature reference, V_{HTF} [(1/8 * V_{LTF}) + (7/8 * V_{TCO})], where V_{TCO} is the cutoff temperature reference level on the TCO pin.

These limits establish the acceptable temperature sense voltage window for fast charge initiation. If the battery fails either of these two prequalifications for discharge or charge, the bq2003 enters a charge-pending mode, waiting for battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cool, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2003 waits until the battery voltage is an acceptable level before starting the charge action. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2003 to remain in the charge-pending state.

Initiating Charge Action and Discharge-Before-Charge

The CCMD and DCMD pins are described together in this section because these pins must be tied to the same potential for proper functionality.

A battery charge action (prequalification, fast charge, and optional "top-off") is initiated under control of the

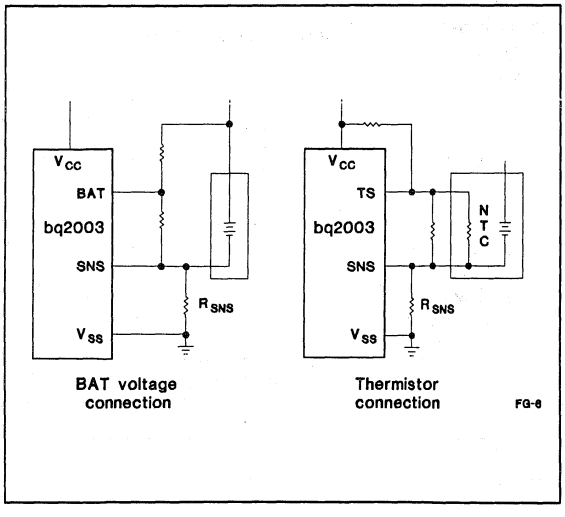


Figure 3. Voltage and Temperature Limit Measurement

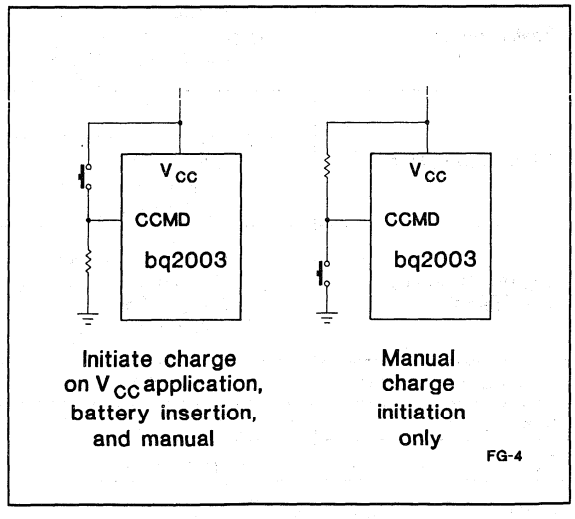


Figure 4. Charge Action Initiation

CCMD pin. The DCMD pin supports automatic discharge-before-charge to V_{EDV} to provide conditioning as well as capacity calibration.

Because the CCMD and DCMD pins must be tied to the same potential, these pins can be treated electrically in two ways. Both pins can be connected to V_{CC} or to V_{SS}. Either treatment allows for automatic charge initiation on battery replacement or when V_{CC} is applied. Battery replacement is recognized when the voltage at the BAT pin falls from above the MCV pin reference level to below that level.

Otherwise, charge is initiated by: (1) a rising edge to V_{CC} at CCMD if both CCMD and DCMD are connected to V_{SS}, or (2) a falling edge to V_{SS} at CCMD if both CCMD and DCMD are connected to V_{CC}.

Discharge-before-charge is initiated at any time by: (1) a rising edge to V_{CC} at DCMD if both DCMD and CCMD are connected to V_{SS}, or (2) a negative-going pulse (from V_{CC} to V_{SS} and then back to V_{CC}) at DCMD if both DCMD and CCMD are connected to V_{CC}.

When the discharge begins, the DIS output goes high to activate an external transistor that connects a load to the battery. When discharge reaches $V_{CELL} = V_{EDV}$, DIS goes low and fast charge begins (provided the pre-charge qualifications are met).

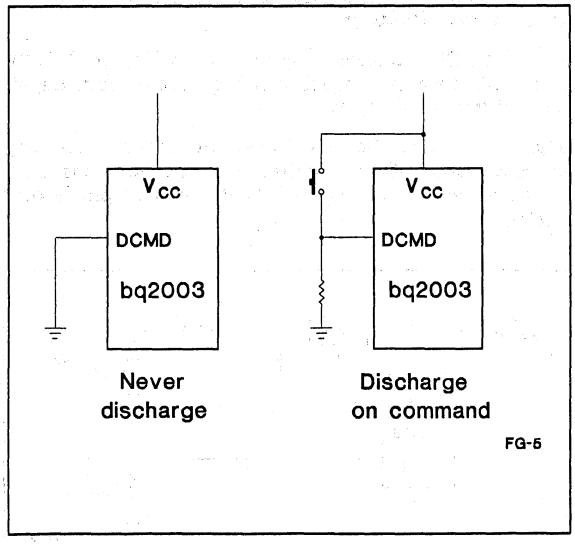


Figure 5. Discharge-Before-Charge

Fast Charge

Once temperature and voltage prequalifications are met and any required discharging of the battery is completed, fast charging begins and continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Negative delta voltage ($-\Delta V$)
- Maximum temperature
- Maximum charge time
- Maximum battery voltage

Voltage Termination Hold-Off

At the start of fast charging, there is a hold-off time during which $-\Delta V$ and maximum cell voltage (MCV) terminations are disabled. (See Table 2.) Once past the initial fast charge hold-off time, these terminations are re-enabled.

$\Delta T/\Delta t$ and maximum temperature terminations are not affected by the hold-off period.

-ΔV Fast Charge Termination

The bq2003 makes a termination decision based on negative delta voltage ($-\Delta V$) every 34 seconds. If V_{CELL} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated.

The $-\Delta V$ test is valid only for $V_{MCV} - (0.2 * V_{CC}) \leq V_{CELL} \leq V_{MCV}$. $-\Delta V$ detection may be enabled or disabled at any time using the DVEN pin.

ΔT/Δt Fast Charge Termination

The bq2003 makes a termination decision based on delta temperature/delta time ($\Delta T/\Delta t$) every 34 seconds based on temperature measurements over a 68-second time period. If V_{TEMP} + 16mV (typical) is less than the voltage measured 68 seconds previously, the fast charge phase of the charge action is terminated.

The $\Delta T/\Delta t$ test is valid only for $V_{TCO} \leq V_{TEMP} \leq V_{TCO} + 0.2 * V_{CC}$.

Maximum Voltage, Maximum Time, and Maximum Temperature Safety Terminations

The bq2003 also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV).

MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during fast charging. If either of these limits is exceeded, both fast charging and any optional top-off charge are terminated.

Table 2. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM_1	TM_2	Fast Charge Safety Time (minutes) Typical	-ΔV/MCV Hold-Off Time (seconds) Typical	Top Off
C/4	Low	Low	360	137	N
C/2	Float	Low	180	820	N
1C	High	Low	90	410	N
2C	Low	Float	45	200	N
4C	Float	Float	23	100	N
C/2	High	Float	180	820	Y
1C	Low	High	90	410	Y
2C	Float	High	45	200	Y
4C	High	High	23	100	Y

Note: $T_A = 25°C$, $V_{CC} = 5.0V$.

Maximum time selection is programmed using the TM_1 and TM_2 pins (see Table 1). Time settings are available for corresponding charge rates ranging from C/4 to 4C.

Temperature Monitoring

Temperature is represented as a voltage input to the bq2003 at the TS pin. Generally, this voltage is developed from a thermistor. The bq2003 recognizes an internal voltage level of $V_{LTF} = 0.4 * V_{CC}$ as the Low-Temperature Fault (LTF) level. If $V_{TEMP} \geq V_{LTF}$, charging is inhibited ($V_{TEMP} = V_{TS} - V_{SNS}$). Similarly, the external reference voltage level presented at the TCO pin represents the temperature cutoff point at which fast charging is terminated.

All temperature prequalifications and $\Delta T/\Delta t$ termination may be disabled by connecting TCO to V_{SS} and fixing the TS pin level at $0.1 * V_{CC}$.

Top-Off Charge

An optional top-off charge phase is selectable to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins. (See Table 2.) If selected, the bq2003 "tops off" the battery at a pulsed rate. The charge control cycle is modified so that MOD is activated for only 4 seconds of every 34 seconds. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to the fast charge safety time (see Table 2). Temperature (TCO) and voltage (MCV) terminations are the only termination methods enabled during "top off."

Charge Current Control

The bq2003 controls charge current through the MOD output pin. The current control is designed to support implementation of a constant-current switching regulator. See Figure 6.

Nominal regulated current is:

$$I_{REG} = 0.235V/R_{SNS}$$

When used in this configuration, the charge current is monitored at the SNS input by the voltage drop across a resistor, R_{SNS}. R_{SNS} can be chosen to provide a variety of charging currents.

The MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.220V nominal), the MOD output is switched high to gate charge current through the inductor to the battery.

When the SNS voltage is greater than V_{SNSHI} (0.250V nominal), the MOD output is switched low—shutting off current from the supply.

The MOD pin can be used to gate an external charging current source. When an external current source is used, no sense resistor is required, and the SNS pin is connected to V_{SS}.

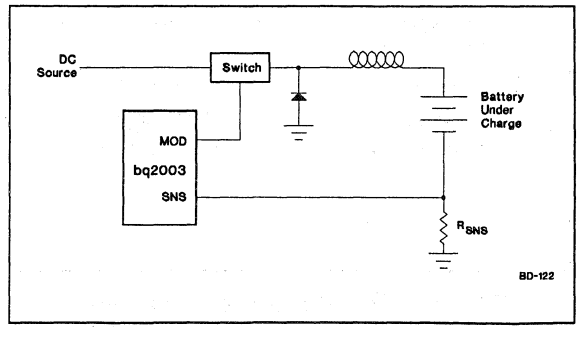


Figure 6. Constant-Current Regulation

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±0.025	V	Tolerance is common mode deviation.
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.044 * V_{CC}	±0.025	V	Tolerance is common mode deviation.
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits charge
V_{HTF}	High-temperature fault	(1/8 * V_{LTF}) + (7/8 * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.2 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits charge

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{MCV}	Maximum cell voltage	V_{EDV}	-	V_{EDV} + (0.2 * V_{CC})	V	
V_{TCO}	Temperature cutoff	V_{LTF} - (0.2 * V_{CC})	-	V_{LTF}	V	
V_{IH}	Logic input high	V_{CC} - 1.0	-	-	V	CCMD, DCMD, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	1.0	V	CCMD, DCMD, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS, TEMP, CHG, MOD, $I_{OH} \leq$ -5mA (see Figure 7)
V_{OL}	Logic output low	-	-	0.5	V	DIS, TEMP, CHG, MOD, $I_{OL} \leq$ 5mA (see Figure 7)
I_{CC}	Supply current	-	0.75	2.2	mA	Outputs unloaded
I_{OH}	DIS, TEMP, MOD, CHG source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	DIS, TEMP, MOD, CHG sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_{IL}	Input leakage	-	-	±1	µA	CCMD, DCMD, DVEN, V = V_{SS} to V_{CC}
	Logic input low source	-	-	70	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0	-	2.0	µA	TM_1, TM_2 may be left disconnected (floating) for Z logic input state
V_{THERM}	Thermistor input resolution for $\Delta T/\Delta t$	-	16 ± 4	-	mV	V_{CC} = 5.0V, T_A= 25°C
-ΔV	Negative delta voltage	-	12 ± 4	-	mV	V_{CC} = 5.0V, T_A= 25°C

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{MCV}	MCV input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for CCMD, DCMD pulse commands	1	-	-	µs	Pulse start for charge or discharge-before-charge
d_{FCV}	Fast charge safety time variation	0.84	1.0	1.16	-	V_{CC} = 4.5V to 5.5V; see Table 2.
t_{REG}	MOD output regulation frequency	-	-	100	kHz	Typical regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	200	250	300	ms	If $V_{CELL} \geq V_{MCV}$ for t_{MCV}, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

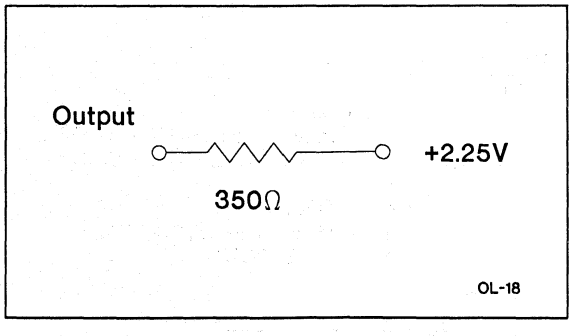


Figure 7. Output Load

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2-59	DCMD transition to initiate discharge-before-charge	Was low-to-high; is pulse with period t_{PW}.
1	2-60	Table 2 ¾ charge rate -ΔV/MCV hold-off time changed	Was 1640 seconds; is 137 seconds.
1	2-62	Changed MCV allowable voltage range	Was 0.2 * V_{CC} min and 0.6 * V_{CC} max; is V_{EDV} min and V_{EDV} + (0.2 * V_{CC}) max.
2	2-62	Added tolerance to -ΔV typical value	Was 12 typ; is 12 ±4 typ.
2	2-63	Changed impedance parameters	Were 50 typ; are 50 min.
2	2-63	Changed t_{REG} value	Was 100 typ; is 100 max.
3	2-55, 2-58, 2-59	CCMD and DCMD pins must be tied together	Clarification
4	2-54	Changed description of -ΔV fast charge termination from "If V_{CELL} is lower than the previous measured value..." to "If V_{CELL} is lower than *any* previous measured value..."	Clarification
4	2-63	Added TS input impedance	Additional specification

Note: Change 1 = Aug. 1992 B changes from Apr. 1992 A.
Change 2 = Oct. 1992 C "Final" changes from Aug. 1992 B "Preliminary."
Change 3 = Dec. 1992 D changes from Oct. 1992 C.
Change 4 = Oct. 1993 E changes from Dec. 1992 D.

Ordering Information

bq2003 -

- Temperature:
  - blank = Commercial (0 to +70°C)
  - N = Industrial (-40 to +85°C)*
- Package Option:
  - PN = 16-pin narrow plastic DIP
  - S = 16-pin SOIC
- Device:
  - bq2003 Fast Charge IC

* Contact factory for availability.

BENCHMARQ

DV2003L1

Fast Charge Development System

Control of On-Board Linear Current Regulator or External Current Source

2

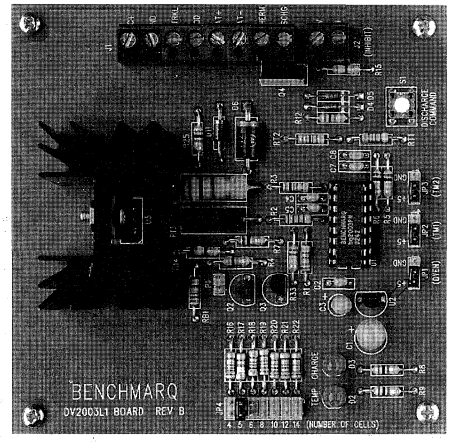
Features

- bq2003 fast charge control evaluation and development
- Charge current sourced from an on-board linear regulator (1.25A, modifiable for 0.1 to 1.5 A) or an external current source
- Fast charge of 4 to 14 NiCd or NiMH cells
- Fast charge termination by $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, time, and voltage
- $-\Delta V$ enable, hold-off, top-off, maximum time, number of cells, and off-board current source control are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input

General Description

The DV2003L1 Development System provides a development environment for the bq2003 Fast Charge IC. The DV2003L1 incorporates a bq2003 and an LM317 linear regulator to provide fast charge control for 4 to 14 NiCd or NiMH cells. The DV2003L1 also supports on/off control of an external current source.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, and external inhibit command. Jumper settings select the $-\Delta V$ enabled state, select the hold-off, top-off, and maximum time limits, and enable the use of an external current source.

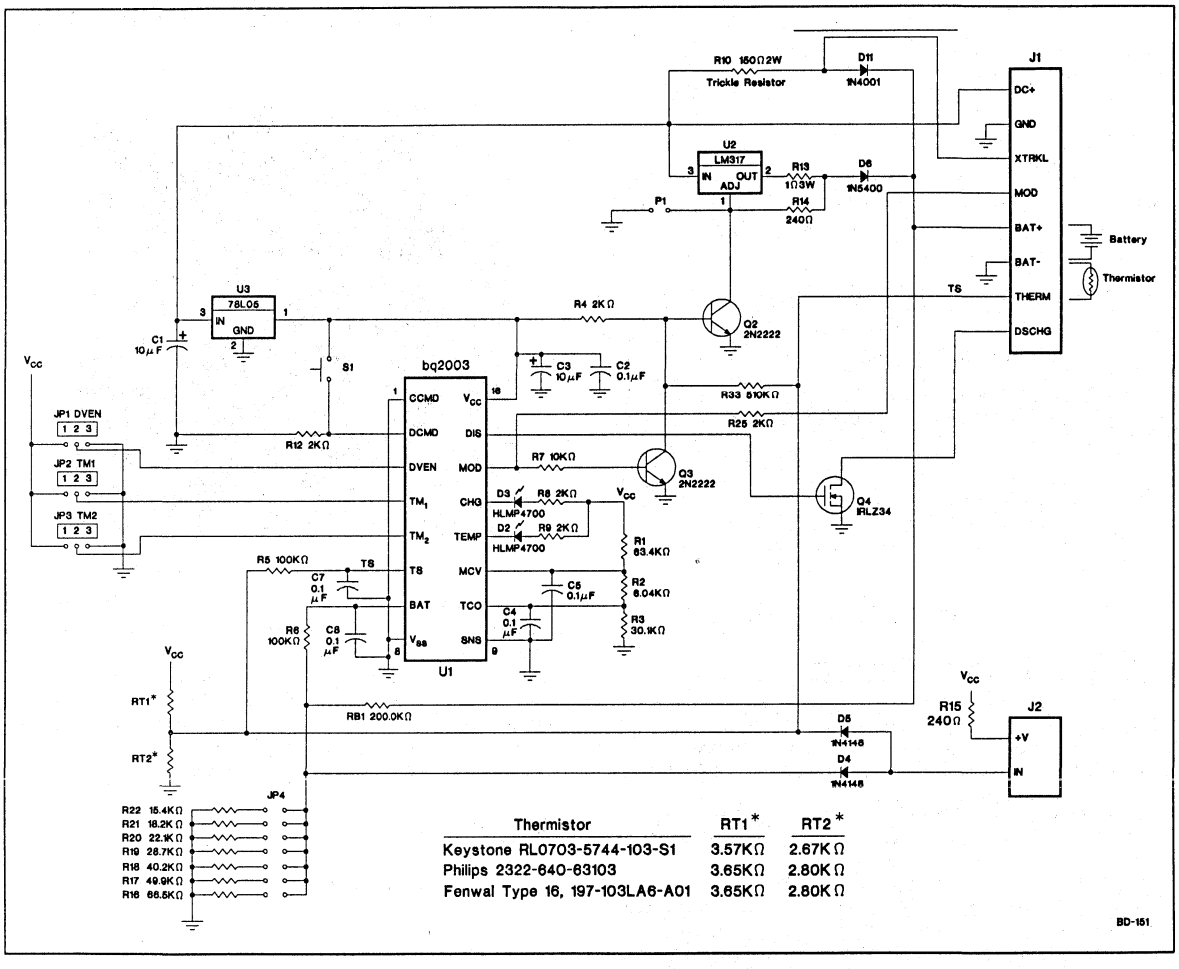


The user provides a power supply and batteries. If the on-board 1.25A linear regulator is disabled, the external current source must have an appropriate digitally controlled switch (active high). The user configures the DV2003L1 for the number of cells, $-\Delta V$, charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.

Contents

1	DV2003L1 printed circuit board containing: a) bq2003 PDIP IC b) LM317 c) All programming jumpers d) NTC thermistor
1	bq Charge Configuration diskette
1	Documentation kit including user's guide, schematics, and data sheets

DV2003L1 Board Schematic



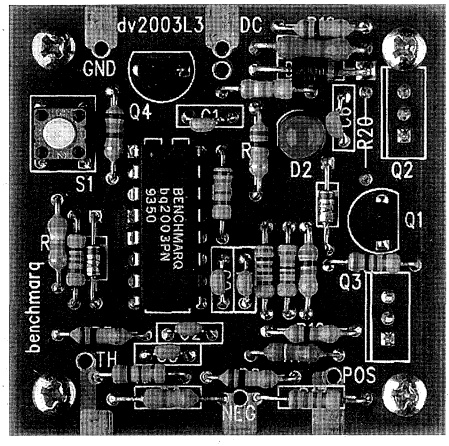
BENCHMARQ DV2003L3

Fast Charge Development System

Control of Frequency-Modulated Linear Regulator

Features

- ➤ bq2003 fast charge control evaluation and development
- ➤ Charge current controlled with frequency-modulated linear design
- ➤ Fast charge of 2 to 12 NiCd and/or NiMH cells
- ➤ Fast charge termination by -ΔV, ΔT/Δt, maximum temperature, time, and voltage
- ➤ Discharge-before-charge option



General Description

The bq2003L3 Development System provides a cost-effective component-reduced development environment for the bq2003 Fast Charge IC. The DV2003L3 incorporates a frequency-modulated linear regulator for fast charge control of NiCd and/or NiMH cells.

Contents

1 DV2003L3 Development Board (includes 6W heat sink)

1 bq Charge Configuration Diskette

1 Documentation kit including user's guide, schematics, and data sheets

DV2003L3 Configuration—Complete Before Ordering

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

DC input voltage (V) _____

-ΔV enabled (yes/no) _____

ΔT/Δt enabled (yes/no) _____

Number of battery cells (2—12) _____

Charge current (A) (1.5A max.) _____

Battery capacity (mAh) _____

Battery type (NiCd and/or NiMH) _____

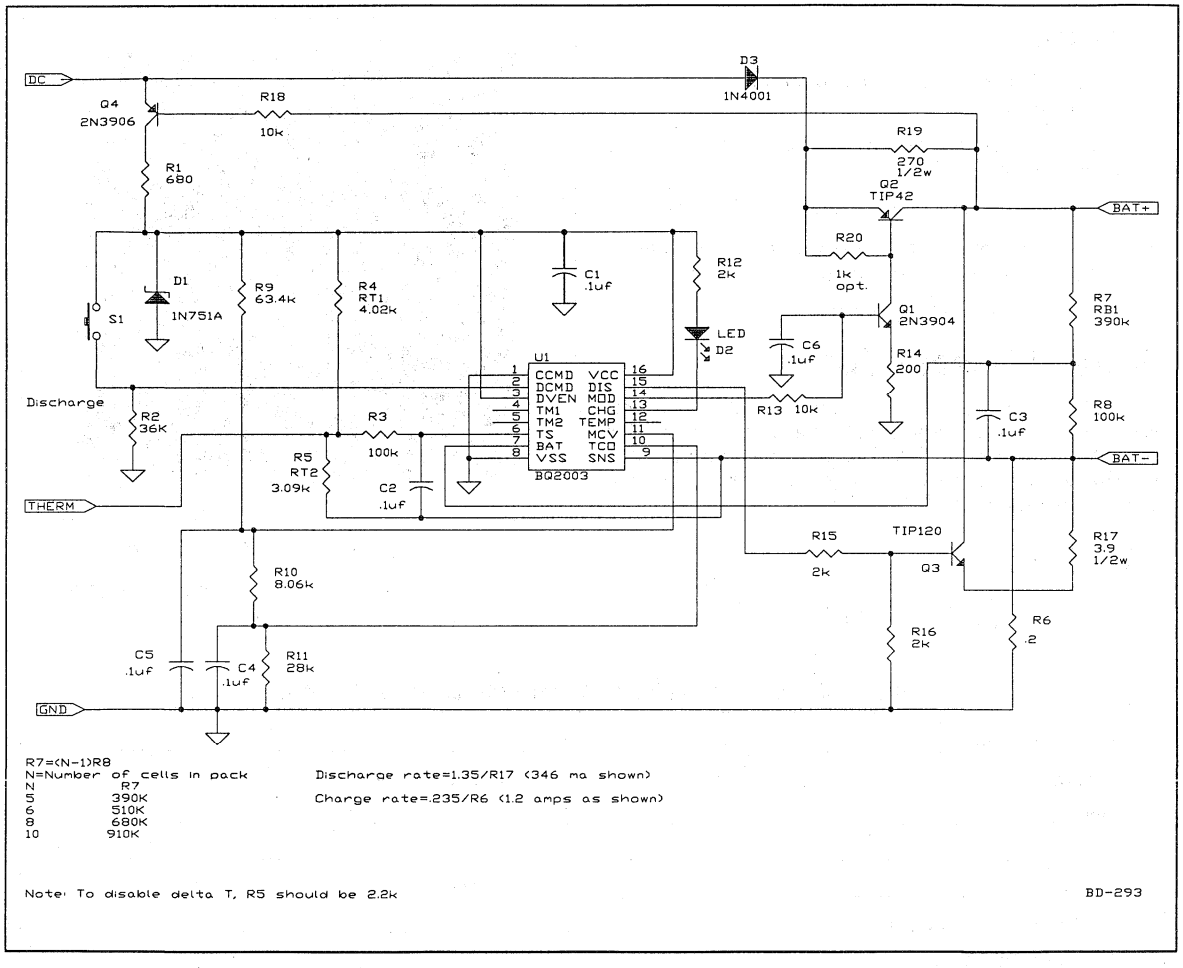
Top-off (yes/no) _____

Discharge-before-charge (yes/no) _____

Discharge current (mA) _____

Oct. 1994

DV2003L3 Board Schematic



BENCHMARQ

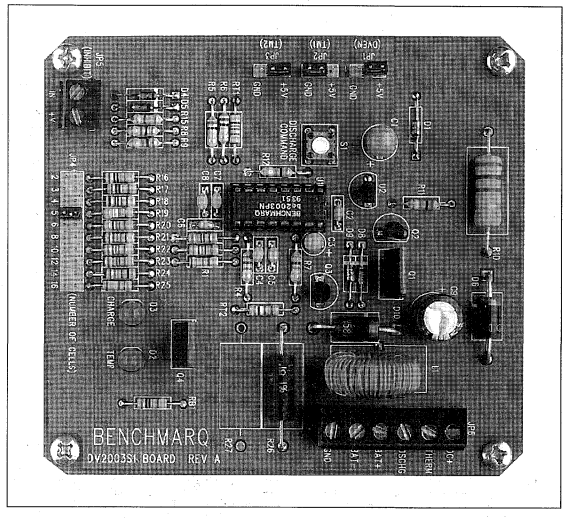
DV2003S1

Fast Charge Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2003 fast charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)
- Fast charge of 2 to 16 NiCd or NiMH cells
- Fast charge termination by $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, time, and voltage
- $-\Delta V$ enable, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input



General Description

The DV2003S1 Development System provides a development environment for the bq2003 Fast Charge IC. The DV2003S1 incorporates a bq2003 and a buck-type switch-mode regulator to provide fast charge control for 2 to 16 NiCd or NiMH cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, and external inhibit command. Jumper settings select the $-\Delta V$ enabled state, select the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2003S1 for the number of cells, $-\Delta V$ charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.

Contents

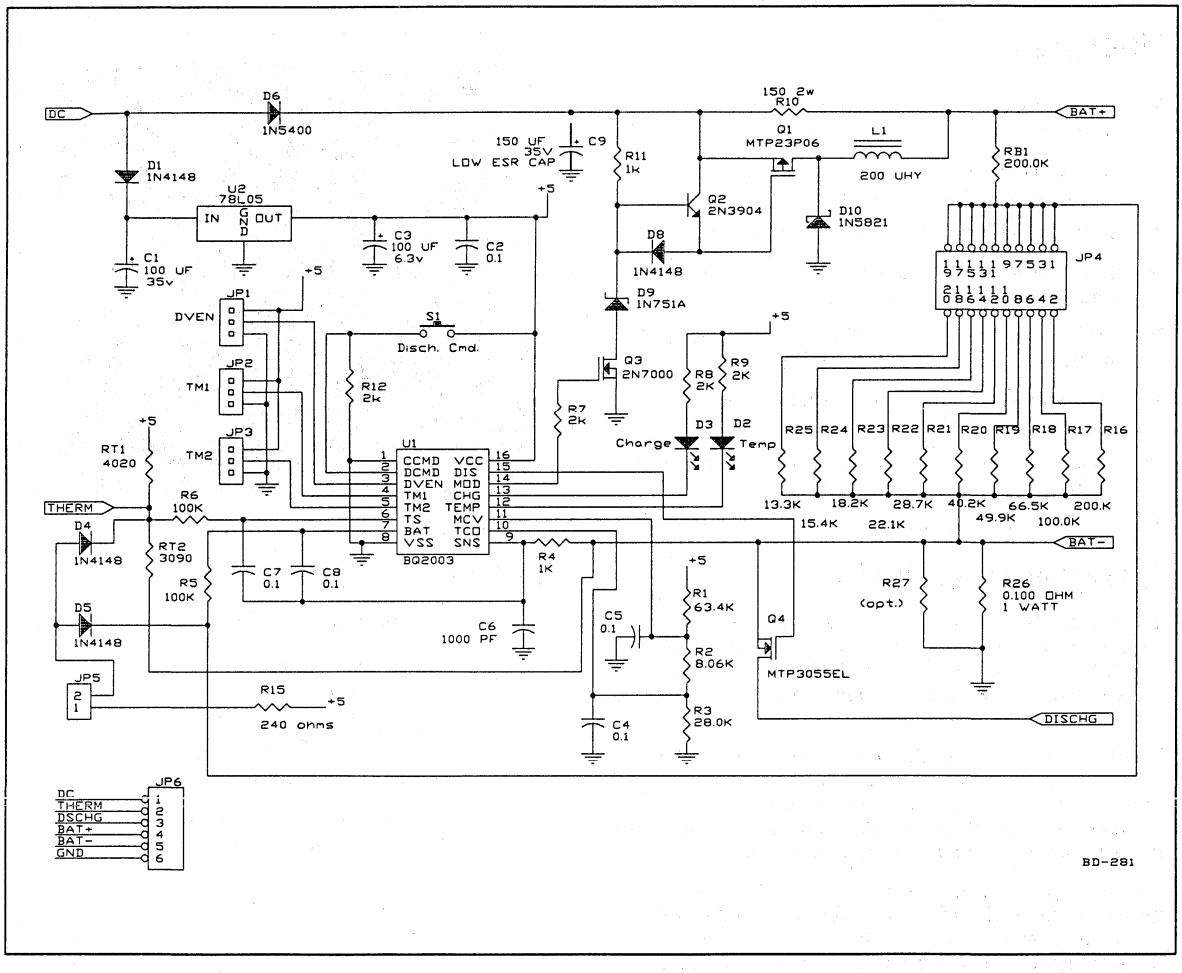
1 DV2003S1 printed circuit board containing:

a) bq2003 PDIP IC
b) Switch-mode current regulator
c) All programming jumpers
d) NTC thermistor

1 bq Charge Configuration diskette

1 Documentation kit including user's guide, schematics, and data sheets

DV2003S1 Board Schematic



BENCHMARQ

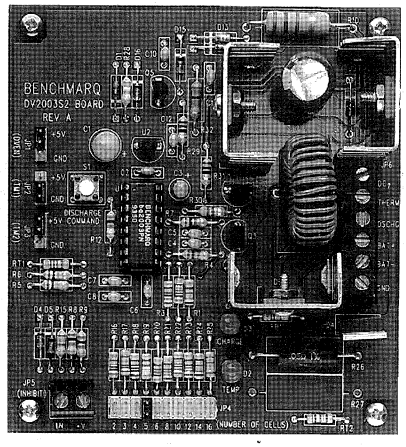
DV2003S2

Fast Charge Development System

Control of On-Board n-FET Switch-Mode Regulator

Features

- bq2003 fast charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 6.0 A)
- Fast charge of 2 to 16 NiCd or NiMH cells
- Fast charge termination by ΔT/Δt, -ΔV, maximum temperature, time, and voltage
- -ΔV enable, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input



General Description

The DV2003S2 Development System provides a development environment for the bq2003 Fast Charge IC. The DV2003S2 incorporates a bq2003 and an n-FET buck-type switch-mode regulator to provide fast charge control for 2 to 16 NiCd or NiMH cells. The primary difference between the DV2003S2 and the DV2003S1 is in the switching FET Q1. The DV2003S1 uses a p-FET for battery charge currents of 3.0A or less, whereas the DV2003S2 uses an n-FET to support charge currents up to 6.0A.

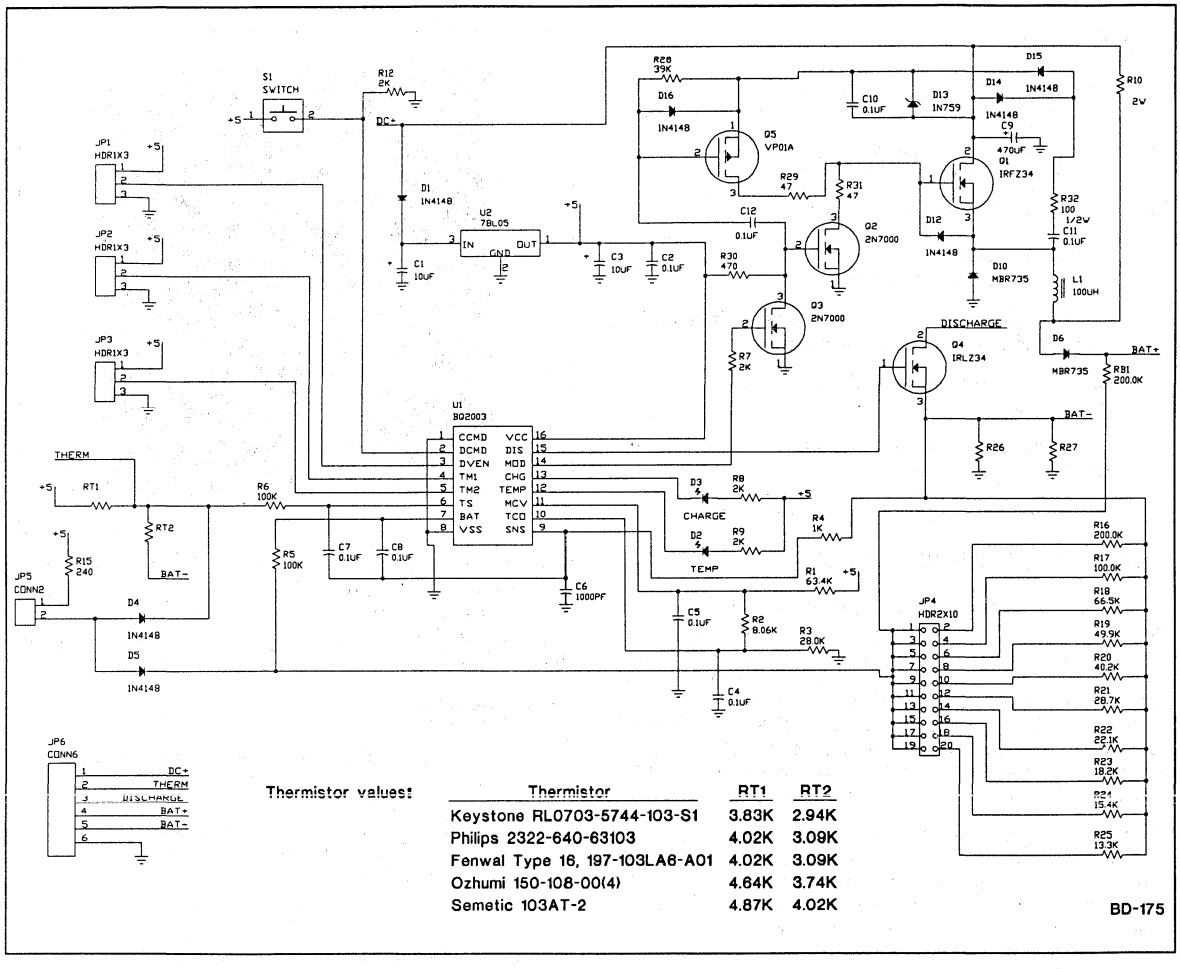
The fast charge is terminated by any of the following: ΔT/Δt, -ΔV, maximum temperature, maximum time, maximum voltage, and external inhibit command. Jumper settings select the -ΔV enabled state, select the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2003S2 for the number of cells, -ΔV charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.

Contents

1	DV2003S2 printed circuit board containing: a) bq2003 PDIP IC b) Switch-mode current regulator c) All programming jumpers d) NTC thermistor
1	bq Charge Configuration diskette
1	Documentation kit including user's guide, schematics, and data sheets

DV2003S2 Board Schematic



BENCHMARQ

Using the bq2003 to Control Fast Charge

Introduction

This application note describes the use and functions of the bq2003 gating a current source to fast charge NiCd or NiMH batteries. Examples describe the ease with which the bq2003 is incorporated into applications.

The bq2003 may also serve as the modulator for a switching-mode constant-current regulator to provide an efficient charge current source. This is discussed in the Application Note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC."

Examples for additional applications are being developed. Please contact Benchmarq if your application is not supported by one of these examples.

The bq2003 is targeted for applications requiring state-of-the-art fast-charging performance at minimal cost. It provides sophisticated full-charge detection techniques such as $\Delta T/\Delta t$ (delta temperature/delta time) and $-\Delta V$ (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2003 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

A significant advantage of the bq2003 over other fast-charge solutions is the use of $\Delta T/\Delta t$ and/or $-\Delta V$ as the primary decisions for fast-charge termination. $\Delta T/\Delta t$ detection is one of the most sensitive and reliable methods for fast-charge termination when charging NiMH and NiCd batteries. Near maximum charge acceptance, the temperature rise begins to accelerate at the same time that voltage rise accelerates. The $\Delta T/\Delta t$ decision typically precedes the peak voltage, allowing for minimal overcharge stress.

The $\Delta T/\Delta t$ method also tolerates varying rates of charge, which may be desirable when charging during system operation.

Compared to the ΔT method, which uses two sensors to monitor battery temperature and ambient temperature, the $\Delta T/\Delta t$ method uses a single thermistor to monitor the rate of temperature increase. This approach is more tolerant in cases when the initial battery temperature is significantly different from the ambient temperature.

bq2003 temperature monitoring may be permanently disabled without affecting other bq2003 charge-termination functions.

The bq2003 monitors the voltage across the battery to detect $-\Delta V$, which is a very reliable charge terminator for NiCd batteries. $-\Delta V$ detection in the bq2003 may be temporarily disabled during periods when the charge current fluctuates greatly or during the beginning of a fast charge to eliminate false peaks. $-\Delta V$ may be permanently disabled without affecting other bq2003 charge-termination functions.

To ensure safety for the battery and system, fast charging also terminates based on a hot-temperature cutoff threshold (TCO), a safety time period, and a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2003 disables MCV and $-\Delta V$ detection during a short "hold-off" period at the start of fast charge. This hold-off period is configured as described in the bq2003 data sheet.

The bq2003 may be configured to have one, two, or three charge stages. As a one-stage charger, the bq2003 controls charge with no trickle. In a two-stage configuration, the fast-charge stage controlled by the bq2003 is preceded and followed by a continuous trickle charge at a rate controlled by a current-limiting resistor outside of the bq2003. In a three-stage configuration, the fast charge is followed by a "top-off" charge stage at 1/8 the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, an external resistor controls trickle charge to the battery at a minimal charge-sustaining rate, typically C/40 or C/50.

Basic Charge-Control Operation

Two detailed applications follow this section. One provides direct control of a linear regulator, and the other provides control of any external current source.

Gating Current

Figure 1 shows an example of external source gating. With SNS tied to chip ground, the bq2003 enables charge current to the battery by taking MOD high at the start of charging and maintaining this state until charging is terminated. In this example, R7, Q2, R15, and Q1 form the switching circuit. When MOD goes high, Q2 switches on—turning on Q1. When MOD goes low, the base current in Q1 collapses, breaking the charging path.

The current-handling capability of this circuit is limited by the product of the current gains of the transistors and by the 5mA drive capability of the MOD pin.

This limitation may be removed by replacing the PNP at Q1 with a pFET. See Table 1 for suggested transistors.

Table 1. Suggested Transistors (Q1)

Q1	Type	Package	Maximum Current	Maximum Voltage
IRFR9010	pFET	DPAK	5.3	-50
IRFR9022	pFET	DPAK	9.0	-50
IRFR9020	pFET	DPAK	9.9	-50
IRFD9014	pFET	HEXDIP	1.1	-60
IRFD9024	pFET	HEXDIP	1.6	-60
IRF9Z10	pFET	TO-220	4.7	-50
IRF9Z22	pFET	TO-220	8.9	-50
IRF9Z20	pFET	TO-220	9.7	-50
IRF9Z32	pFET	TO-220	15	-50
BD136	PNP	TO-225	1.5	-60
MJE171	PNP	TO-225	3.0	-60
TIP42A	PNP	TO-220	6.0	-60

Note: For very high currents, two paralleled pFETs or an nFET with a high-side driver circuit may be suitable.

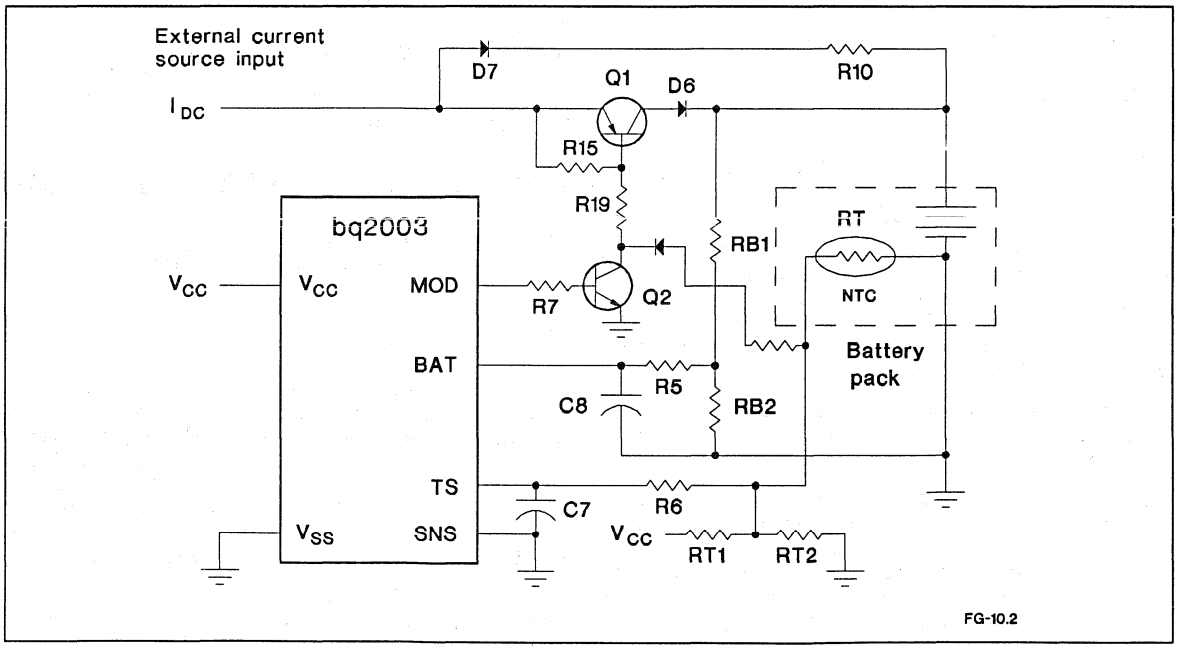


Figure 1. Gated External Source (Bipolar Switch Option)

Charge Status

The charge status of the bq2003 is indicated by two outputs. Each output may directly drive an LED. One LED uses distinctive flashing patterns to indicate the current charger status as:

Charge Action State	Charge Status Output	
	Low	High
Battery absent/abort	-	Continuous
Pending charge (waiting for proper temperature and/or voltage)	1/8 sec	1 3/8 sec
Discharging (optional)	1 3/8 sec	1/8 sec
Fast charging	Continuous	-
Charging complete	1/8 sec	1/8 sec
Top-off (optional)	1/8 sec	1/8 sec

A second LED indicates that the battery temperature detected by the bq2003 and associated thermistor is out of range for fast charging.

Charge Initiation

Charge may be initiated by power to the IC, battery replacement, or application of a digital signal. Configuration options are shown in Figure 2.

Charge initiation by application of power to the IC works as follows: When V_{CC} is applied, the bq2003 is held in reset for approximately one and one-half seconds. At the end of the reset period, the CCMD pin (pin 1) is sampled and, if CCMD and DCMD are low, a charge cycle initiates as soon as conditions allow.

Charge initiation on battery replacement relies on the BAT pin voltage being greater than MCV in the absence of a battery, and falling below MCV when the battery is connected. For example, in Figure 1 a resistor R10 is inserted between the positive battery terminal and I_{DC}. This resistor, in conjunction with RB1 and RB2, is sized to pull the BAT pin (pin 7) above the value programmed on MCV (pin 11, maximum cell voltage threshold) when the battery is removed.

When the battery is replaced in this case, the voltage on BAT should fall below MCV, at which time a charge cycle initiates as soon as conditions allow (if CCMD and DCMD are low).

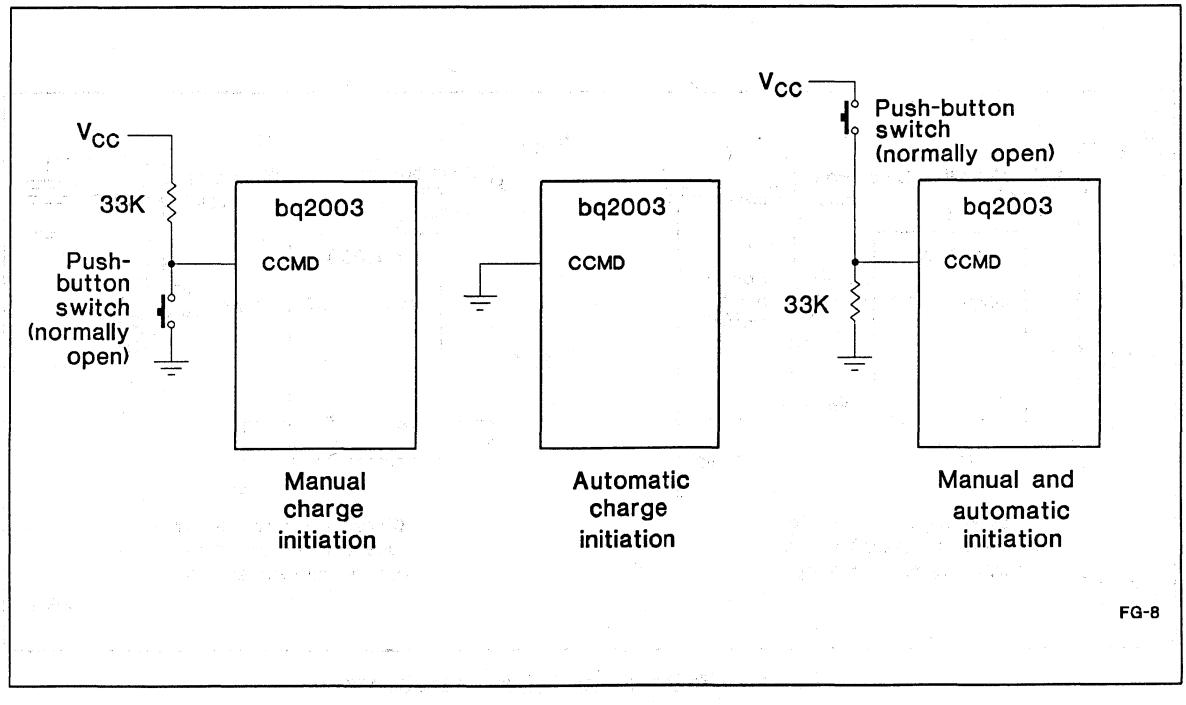


Figure 2. Charge Initiation Network

Charge initiation by digital signal occurs on the rising edge of CCMD with DCMD low. Digital charge initiation, which is simply a request to charge the battery, results in charging as soon as conditions allow.

The charge command may be issued at any time, but charging may be disqualified because the battery voltage or temperature is outside programmed limits. Fast charging remains pending until all charge qualifications become valid. When conditions allow, fast charging begins. A CCMD-initiated charge with battery absent remains pending until battery replacement.

Discharge Before Charge

It may be desirable in the application to allow the user to occasionally discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 3 illustrates the implementation of this function. Discharge-before-charge is initiated on a positive strobe signal on DCMD. **This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS to a high state until the voltage sensed on BAT falls below $V_{CC}/5$.** Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

Unlike a CCMD-initiated charge, the discharge-before-charge function is ignored or terminated when $V_{BAT} - V_{SNS} > V_{MCV}$ (battery removed).

If the discharge-before-charge function is not desired, DCMD should be tied to V_{SS}.

Configuring the BAT Input

The bq2003 uses the battery voltage sense input on the BAT pin to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, and facilitate negative delta voltage (-ΔV) detection.

V_{BAT} may be derived from a simple passive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range, which is between V_{MCV} and $V_{MCV} - 1V$.

For NiCd and NiMH batteries, the battery terminal voltage is divided down to a per-cell potential. If, for example, the battery contains four NiCd cells, RB1 may be chosen as 562KΩ and RB2 as 187KΩ.

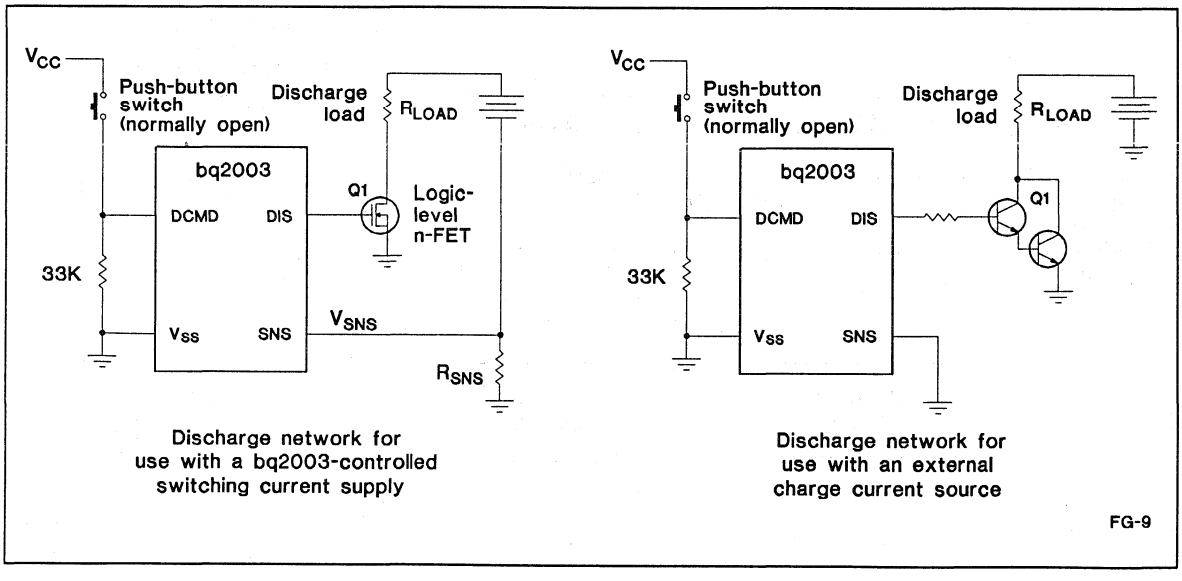


Figure 3. Battery Conditioning Network

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the BAT pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from BAT between 20KΩ and 1MΩ is acceptable over the bq2003 operating range. Total impedance between the battery terminal and V_{SS} should typically be about 300KΩ to 1MΩ . See Table 2.

Notes: (1) Because V_{SNS} may be positive in bq2003 switching regulation applications, the actual internal comparison uses $V_{BAT} - V_{SNS}$, or V_{CELL}. This internal value V_{CELL} maintains a representative single-cell voltage independent of any current through R_{SNS}.

(2) The R-C time delay in the presentation of V_{BAT} must be shorter than 200ms (t_{MCV}). A longer delay may result in a failure to determine "battery replaced."

Table 2. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1	RB2
4	562 KΩ	187 KΩ
5	649 KΩ	162 KΩ
6	590 KΩ	118 KΩ
8	931 KΩ	133 KΩ
10	953 KΩ	105 KΩ
12	374 KΩ	34 KΩ
14	649 KΩ	49.9 KΩ
16	750 KΩ	49.9 KΩ

Configuring the MCV Input

Battery over-voltage protection is accomplished by comparing V_{CELL} to the voltage on the MCV input pin. If V_{CELL} becomes greater than V_{MCV}, both charging and top-off terminate.

A typical MCV value is 1.8V for NiCd and NiMH batteries. The MCV voltage is derived from either of the networks shown in Figure 4. The combined network has the advantage of fewer resistors in generating both the MCV and TCO thresholds, but loses the independence of threshold adjustment.

To detect the presence of a battery, the DC supply voltage must be larger than MCV * N + V_{LOSST}, where V_{LOSST} is defined as the trickle charging path voltage loss and N is the V_{BAT} divisor.

Temperature Sensing and the TCO Pin

The bq2003 uses the temperature sense input on the TS pin to qualify charge initiation and termination. A negative temperature coefficient (NTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 1. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT. If this temperature sensor is to be used for charge control, it should be directly in contact with the cells.

Temperature-decision thresholds are defined as LTF (low-temperature fault), HTF (hot-temperature fault), and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-HTF range. In this case, the temperature fault indicator on TEMP is driven low, and charging does not initiate until the battery temperature enters this range.

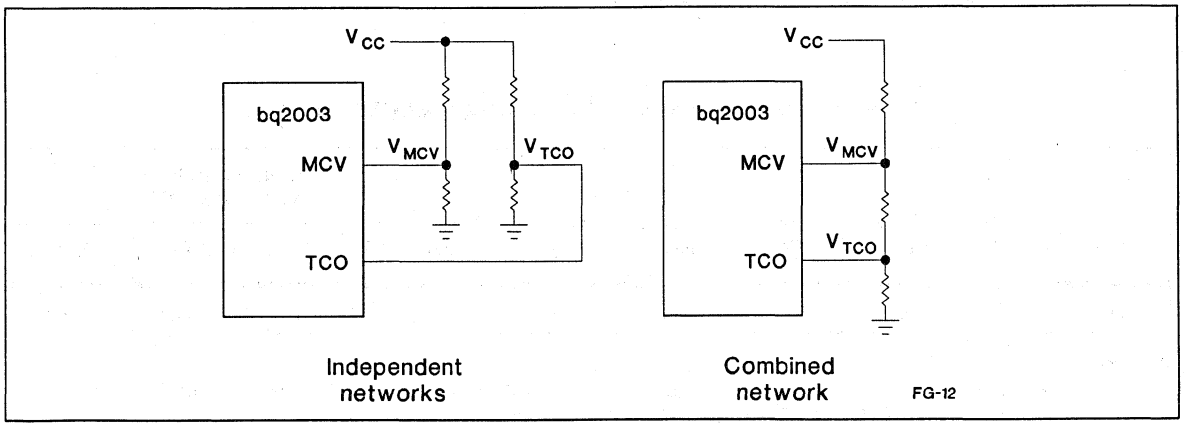


Figure 4. Threshold Networks

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2003 interprets the reference points V_{LTF}, V_{HTF}, and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at 2/5 V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 5. Note that since the voltage on pin TS decreases as temperature increases, V_{TCO} should always be less than 2/5 V_{CC}. V_{HTF} is set internally 7/8 of the way from V_{LTF} to V_{TCO}. The resistive dividers shown in Figure 4 may be used to generate the desired V_{TCO}.

Note: HTF is not meaningful for bq2003 switching current regulation chargers. See the Application Note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC."

$\Delta T/\Delta t$ detection adds an additional constraint on the selection of temperature sense components. Detection occurs when the voltage TS – SNS declines at a rate between 0.0024 V_{CC} and 0.0040 V_{CC} per 68 seconds, with a nominal 5V V_{CC} producing a nominal detection rate of 14mV/min (16mV/68sec). For example, assuming a 1°C/min desired average $\Delta T/\Delta t$ detection rate ($T_{\Delta T}$), and minimum and maximum charge temperatures of 0° and 40°C, respectively, V_{TCO} equals:

$$V_{TCO} = (2 * V_{CC}/5) - (0.0028 * V_{CC} * (T_{TCO} - T_{LTF}))$$

$$= 2 - (0.014 * (40 - 0))$$

$$= 1.44V$$

Table 3 shows the temperature control values that apply for Application Examples 1 and 2, assuming the Fenwal part number 197-103LA6-A01 thermistor. Appendix A explains the derivation of such component values.

New $\Delta T/\Delta t$ samples are processed every 34 seconds. To minimize the risk of premature termination, the design should be configured assuming a minimum charge cutoff rate of 0.0024 * V_{CC}, or 10.6mV per minute (at 25°C; V_{CC} = 5V). This is the lowest signal that may be recognized as meeting the decision threshold. Repeating samples cause a decision quickly as the voltage ramps between this minimum threshold and the nominal 14mV per minute. The system is self-compensating in that the thermistor provides increasingly overstated negative voltage change with increasing temperature, making the measurement more sensitive at higher temperatures. The last three columns of Table 3 are an example of this relationship.

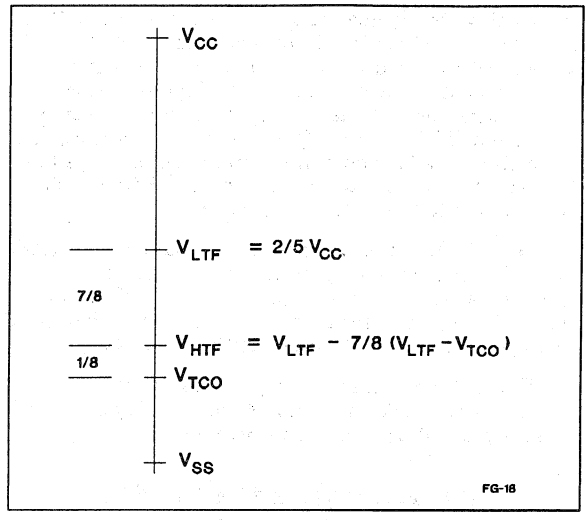


Figure 5. Temperature Reference Points

Table 3. Example Values, Temperature Sense Network

LTF (°C)	HTF (°C)	TCO (°C)	V_{TCO} (V)	RT1 (KΩ)	RT2 (KΩ)	$T_{\Delta T}$ (°C/min)	Minimum-to-Nominal $\Delta T/\Delta t$ Rate (°C/min) @ 25°C	@ 35°C	@ 45°C
10	47	50	1.50	3.65	2.80	1.04	0.94–1.26	0.75–1.00	0.64–0.85

Notes:
1. V_{SR} = 0V.
2. Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 * V_{CC}.

V_{CC} Supply

The V_{CC} supply provides both power and voltage reference to the bq2003. This reference directly affects BAT voltage and internal time-base voltage measurements.

A 5% or tighter tolerance on V_{CC} is recommended to minimize the error regarding MCV. For example, if MCV nominal is set to be 1.8V per cell, a 5% error on V_{CC} results in MCV = 1.71V to 1.89V. This range is acceptable from the perspective that an MCV charge termination represents a faulty battery. The minimum MCV must be safely above a "healthy" charging voltage. The maximum MCV must satisfy the requirement to recognize battery removed/replaced (see the section, "Configuring the MCV Input").

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = 5V. The oscillator varies directly with V_{CC}. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

Trickle Resistor

The trickle resistor, R10, is sized to limit the constant trickle current, I_T.

$$R10 = (V_{DC} - V_{BAT}) / I_T$$

The resistance of R10 is calculated using I_T = charge current desired after full (typically a C/20 to C/50 rate, possibly less) and the voltage for a fully charged battery (number of cells * 1.4V).

The wattage rating of R10 must accommodate periods of higher I_T when V_{BAT} is at a lower voltage (no fast-charge pending charge qualification).

A very low trickle current contributes to longer battery life, and is particularly critical for NiMH cells.

Top-Off Charge

The top-off charge option allows for the self-discharge replacement trickle current to be very low, but still provides for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off occurs at a 1/8 pulsed rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. It also terminates if TCO or MCV is detected.

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use.

Negative Delta Voltage Fast-Charge Detection

-ΔV full-charge detection may operate in parallel with the ΔT/Δt detection. If temperature control is disabled by design, then -ΔV should be enabled (DVEN to V_{CC}). If -ΔV is enabled, a constant-current charging source is required. Otherwise a drop in current may cause a false -ΔV determination. DVEN may change state at any time.

Mode Selection Pins TM1 and TM2

These two pins are used to select the safety time-out (5 selections, 23 to 360 minutes) and optional top-off charge (4 selections, 23 to 180 minutes, equal to the safety time selection).

The safety time-out should be selected to be longer than any reasonably expected charge time. The nominal charge time (Ahr capacity/charge rate) must be factored up to allow for both charge inefficiency and the fact that many batteries hold more than the rated charge. A safety time-out 1.3–1.5 times the nominal time is normally adequate (i.e., 90 minutes for a 1C charge). The safety time-out may be far in excess of the nominal charge time if the temperature monitor is enabled.

Note: If the charge rate varies (such as fast charging during system operation using ΔT/Δt termination), then the safety time-out selection should allow for the slowest charges that may occur. The 180- or 360-minute selection may be appropriate.

System-Controlled Charge Inhibition

Some in-system chargers may require the ability to block fast charge activity when the system is on.

Two small 1N4148-type diodes—with cathodes connected outside the R-C filter—control the bq2003 BAT and TS inputs to provide this capability. A high signal (INHIBIT) applied to anodes of these diodes blocks charge activity. See Figure 8.

With a high signal applied to BAT and TS, charge is inhibited and both LEDs are off. INHIBIT must be high for longer than t_{MCV} max (300ms) if a subsequent low state is to initiate charge.

INHIBIT could be the system V_{CC}, blocking fast charge at all times the system is ON. This may be needed if -ΔV termination is to be used and the charge supply cannot simultaneously support fast charge and peak system loads.

INHIBIT might also be CPU-controlled, allowing the charger to be inhibited as required by specific situations.

Power Supply Selection

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2003 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the charge operation, V_{DC} > (number of cells * MCV_{MAX}) + V_{LOSS} in the charging path. (MCV_{MAX} is the maximum cell voltage threshold with the maximum bq2003 V_{CC}.)

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by approximately 1V to 2V.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2003 is important when the bq2003 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept relatively isolated from the bq2003 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the V_{CC} pin.
4. 0.1µF capacitors and resistors forming R-C filters connected to pins BAT, TS, TCO, and MCV should be as close as possible to their associated pins.
5. Because the bq2003 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the DCMD input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2003-modulated switching applications:
   - A 2KΩ resistor is required between the MOD pin and the transistor.
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the SNS pin.
   - The 0.1µF capacitors for BAT and TS should be routed directly to SNS and not to ground.

Figures 6 and 7 show an example layout of the non-power path circuits in the "kernel board" available from Benchmarq. Figure 8 is a schematic of the board. Table 4 contains the parts list for the board. A comparable layout is recommended.

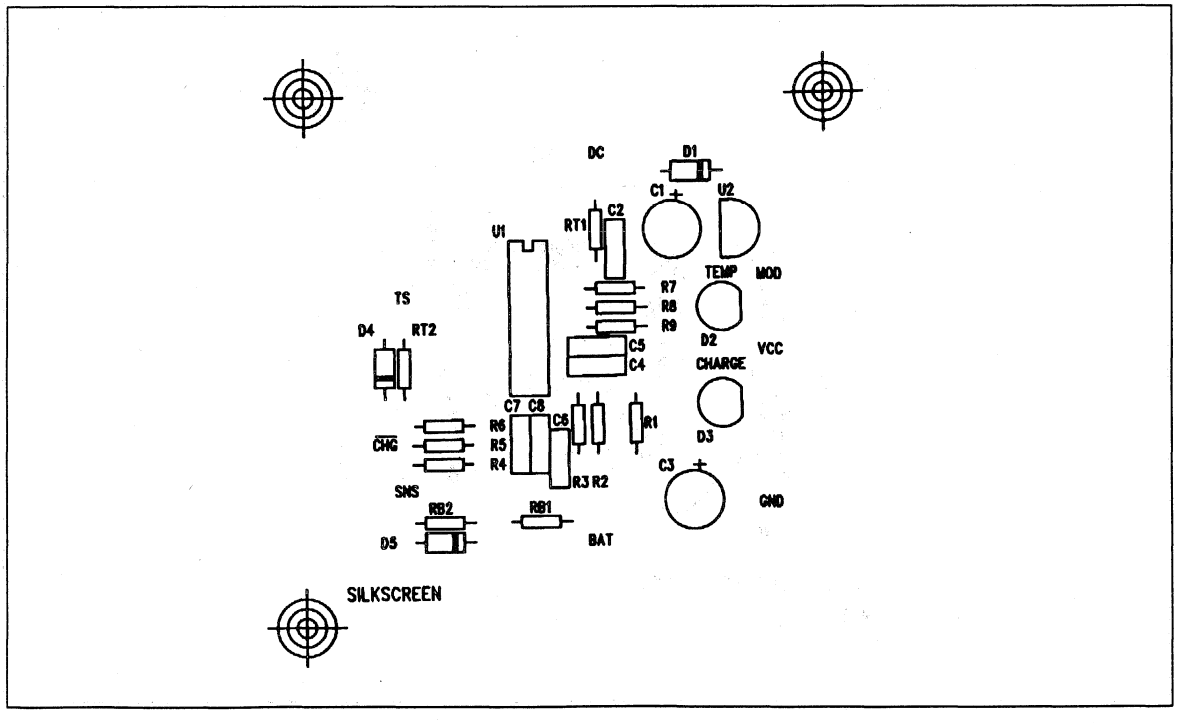
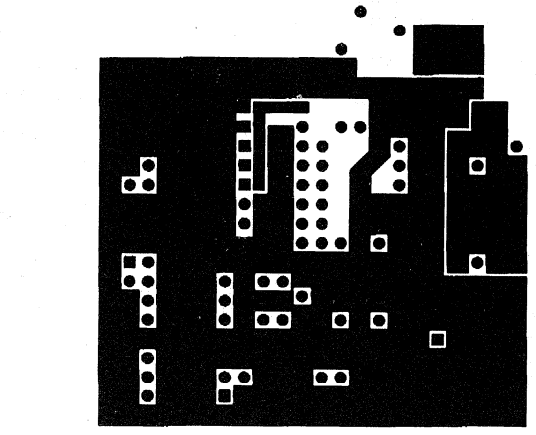
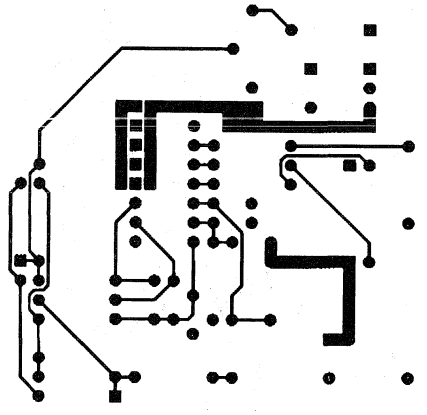


Figure 6. bq2003 Kernel Board Layout, Component Placement



LAYER 1 COMPONENT SIDE



LAYER 2 SOLDER SIDE

Figure 7. bq2003 Kernel Board Layout

Table 4. bq2003 Kernel Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
C6	1000pF ceramic
D1, D4, D5	1N4148
D2, D3	HLMP 4700 red LED
R1	User-defined 1% ¼W or ⅛W carbon film
R2	User-defined 1% ¼W or ⅛W carbon film
R3	User-defined 1% ¼W or ⅛W carbon film
R4, R7, R8, R9	1KΩ 5% ¼W or ⅛W carbon film
R5, R6	100KΩ 5% ¼W or ⅛W carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT1	User-defined 1% ¼W or ⅛W carbon film
RT2	User-defined 1% ¼W or ⅛W carbon film
U1	bq2003
U2	LM78L05ACZ

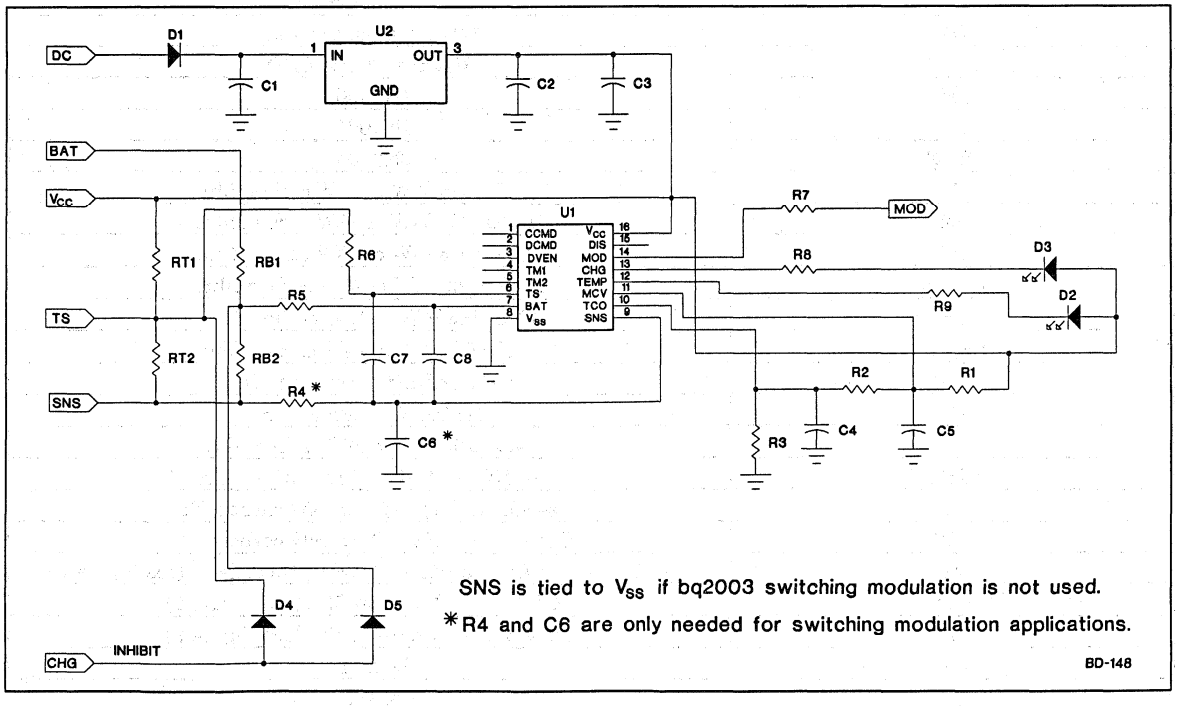


Figure 8. bq2003 Kernel Board Schematic

Application Example 1: Linear Regulator

In the example in Figure 9, the bq2003 is used to implement a linear regulator/charge controller that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 1.5A. R_{16} determines the charge rate per the formula:

$$I = 1.25V / R_{16}$$

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; HTF = 47°C; TCO = 50°C; $T_{\Delta T}$ (average ΔT/Δt) = 1.04°C/ minute. Timer-mode selection (see data sheet) and trickle resistor R10 selection are determined by the designer.

Components to complete this schematic may be selected from the preceding table:

- Table 2: BAT network RB1 and RB2 values

Table 5 contains the parts list for the board.

Notes: (1) Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 * V_{CC}.

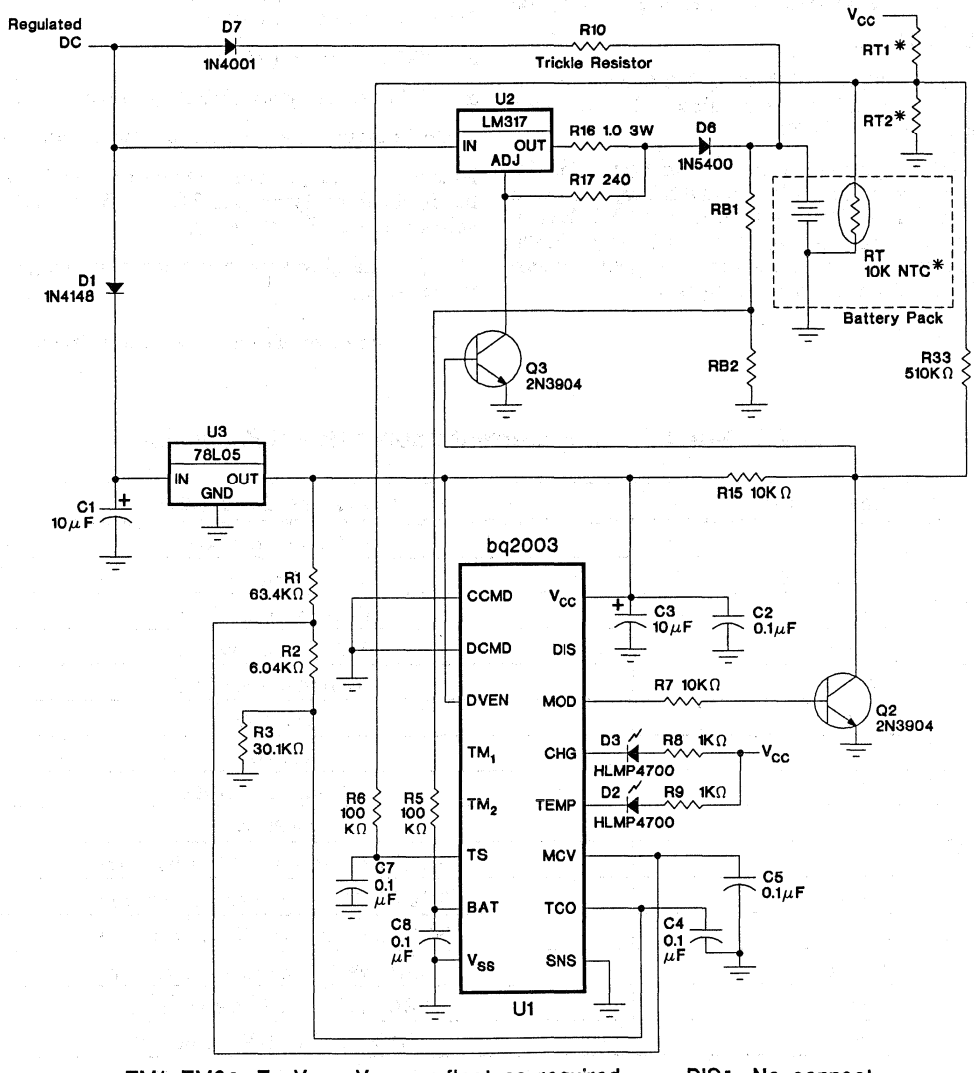
(2) The voltage drop (V_{LOSS}) across LM317, D6, and R16 is 4.25V minimum. The charging supply voltage must be greater than the following:

Number of cells * max. cell voltage + V_{LOSS}

The maximum allowable power loss across the LM317 depends on the heat sinking.

Table 5. Linear Regulator/Charge Controller Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
D1	1N4148 or equivalent
D2, D3	HLMP 4700 red LED
D6	1N5400
D7	1N4001
Q2, Q3	2N3904
R1	63.4KΩ 1% ¼W or ⅛W carbon film
R2	6.04KΩ 1% ¼W or ⅛W carbon film
R3	30.1KΩ 1% ¼W or ⅛W carbon film
R5, R6	100KΩ 5% ¼W or ⅛W carbon film
R7, R15	10KΩ 5% ¼W or ⅛W carbon film
R8, R9	1.0KΩ 5% ¼W or ⅛W carbon film
R10	User-defined 5% carbon film
R16	1Ω 1% 3W carbon film
R17	240Ω 5% ¼W or ⅛W carbon film
R33	510KΩ 5% ¼W or ⅛W carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT	Negative temperature coefficient (NTC) thermistor (see Figure 9)
RT1	1% ¼W or ⅛W carbon film (see Figure 9)
RT2	1% ¼W or ⅛W carbon film (see Figure 9)
U1	bq2003
U2	LM317T
U3	LM78L05ACZ



TM1, TM2: To V_{CC}, V_{SS}, or float as required. DIS: No connect.

The R-C filters on MCV and TCO are recommended in noisy environments.

* NTC, RT1, and RT2:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.57K	2.67K
Philips 2322-640-63103	3.65K	2.80K
Fenwal Type 16, 197-103LA6-A01	3.65K	2.80K

BD-135.2

Figure 9. Linear Regulator/Charge Controller

Application Example 2: Gated External Current Source

In the example in Figure 10, the bq2003 is used to gate an external current-limited or regulated charge source that can charge NiCd or NiMH cells.

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; HTF = 47°C; TCO = 50°C; $T_{\Delta T}$ (average $\Delta T/\Delta t$) = 1.04°C/ minute. Timer-mode selection (see data sheet) and trickle resistor R10 selection are determined by the designer.

Components to complete this schematic may be selected from these preceding tables:

- Table 1: Power switch Q1
- Table 2: BAT network RB1 and RB2 values

Table 6 contains the parts list for the board.

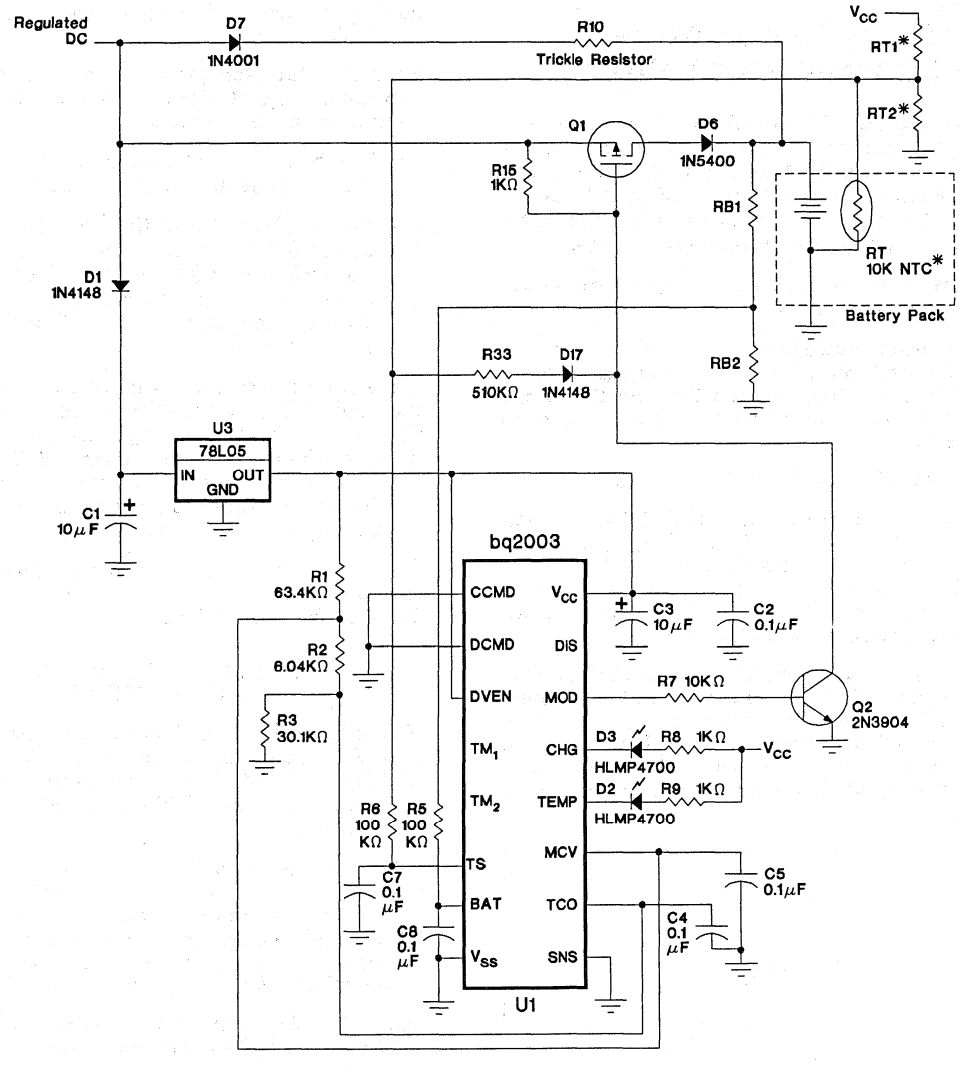
Notes: (1) Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 * V_{CC}.

(2) The charging supply voltage must be greater than the following:

Number of cells * max. cell voltage + V_{LOSS}

Table 6. Gated External Current Source Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
D1, D17	1N4148 or equivalent
D2, D3	HLMP 4700 red LED
D6	1N5400
D7	1N4001
Q1	User-defined pFET
Q2	2N3904
R1	63.4KΩ 1% ¼W or ⅛W carbon film
R2	6.04KΩ 1% ¼W or ⅛W carbon film
R3	30.1KΩ 1% ¼W or ⅛W carbon film
R5, R6	100KΩ 5% ¼W or ⅛W carbon film
R7	10KΩ 5% ¼W or ⅛W carbon film
R8, R9, R15	1KΩ 5% ¼W or ⅛W carbon film
R10	User-defined 5% carbon film
R33	510KΩ 5% ¼W or ⅛W carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT	Negative temperature coefficient (NTC) thermistor (see Figure 10)
RT1	1% ¼W or ⅛W carbon film (see Figure 10)
RT2	1% ¼W or ⅛W carbon film (see Figure 10)
U1	bq2003
U3	LM78L05ACZ



TM1, TM2: To V_{CC}, V_{SS}, or float as required. DIS: No connect.

The R-C filters on MCV and TCO are recommended in noisy environments.

* NTC, RT1, and RT2:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.57K	2.67K
Philips 2322-640-63103	3.65K	2.80K
Fenwal Type 16, 197-103LA6-A01	3.65K	2.80K

BD-137.3

Figure 10. Gating External Current Source

Appendix A
Determining Temperature-Control Component Values

The bq2003 uses an NTC thermistor to determine temperature. The ΔT/Δt sensitivity can be adjusted using different resistor values (RT1 and RT2 in Figure 1 and Application Examples 1 and 2) and a different high-temperature cutoff voltage. Table A-1 lists various thermistor manufacturers, with the appropriate part numbers.

Follow these steps to determine temperature-control component values (see Figure 5):

1a. The low-temperature fault (LTF) limit for charging must be established. LTF for charging is determined by the battery specification and the charge rate used. A typical value for the low-temperature limit is 10°C.

b. V_{LTF} is set within the bq2003 at 0.4 * V_{CC}.

2a. The high-temperature cutoff (TCO) for charging must be established. TCO for charging is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical values range from 40°C to 50°C, although values outside this range may be applicable.

b. The average ΔT/Δt sensitivity from LTF to TCO ($T_{\Delta T}$, expressed as °C/minute) for termination must be established. As mentioned in this application note, the bq2003 provides a typical ΔT/Δt charge termination of 14 mV per minute. The $T_{\Delta T}$ value is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical nominal values for $T_{\Delta T}$ range from 0.75°C/min to 1.5°C/min.

Relative to the average value $T_{\Delta T}$, the minimum-to-maximum range of ΔT/Δt at a specific temperature depends on two parameters:

- The measurement resolution of the bq2003, which contributes a ± 25% error.
- The non-linearity of the thermistor between LTF and TCO. As the temperature nears LTF, the expected ΔT/Δt is less than $T_{\Delta T}$ (less sensitive), and as the temperature nears TCO, the expected ΔT/Δt is more than $T_{\Delta T}$ (more sensitive).

The ΔT/Δt range should be considered in determining the nominal $T_{\Delta T}$. Nominal $T_{\Delta T}$ should be selected so that its minimum value represents an acceptable (non-premature) termination threshold. Thus a first bq2003 sample does not cause a premature termination. Multiple sampling ensures that the termination occurs well before the $T_{\Delta T}$ max.

c. The high-temperature cutoff voltage, V_{TCO}, must be established. This V_{TCO} limit is determined by the $T_{\Delta T}$ and may be calculated by:

$$V_{TCO} = [\ (2 * V_{CC}/5) - (0.0028 * V_{CC} * (TCO - LTF))\ ] / T_{\Delta T}$$

V_{TCO} is provided at the TCO pin by a resistor-divider network as shown in Figures 9 and 10: $V_{TCO} = V_{CC} * R3/(R1 + R2 + R3)$. In this arrangement, R1 and R2 are selected such that $MCV = V_{CC} * (R2 + R3)/(R1 + R2 + R3)$.

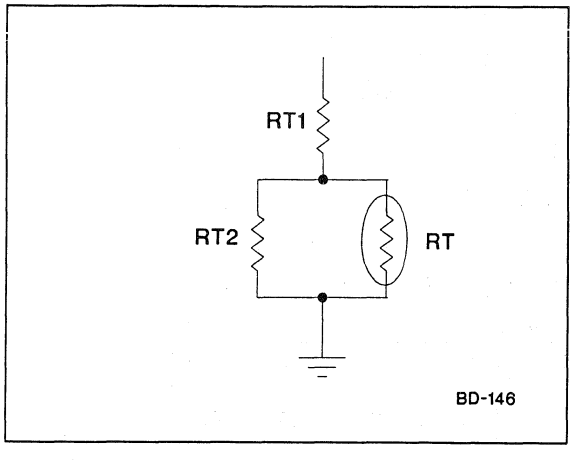


Figure A-1. Resistor Network

4. Select the thermistor to be used. If it is not from Table A-1, the thermistor sensitivity at 25°C should be at least -4% and the ΔR steps between 30°C and 50°C should be comparable to or greater than those in Table A-1 to obtain the appropriate accuracy. Lower values affect the linearity of the ΔT/Δt.

5. Determine the thermistor resistance at LTF and TCO (R_{LTF} and R_{TCO}, respectively). This may be done using the thermistor temperature versus resistance conversion table provided with the thermistor specification. These tables are usually in 5°C increments.

6. The values for RT1 and RT2 may be calculated by:

$$T1 = R_{LTF} * (1 - (2/V_{CC}))/(2/V_{CC})$$

$$T2 = R_{TCO} * (1 - (V_{TCO}/(V_{CC} - V_{SNS})))/(V_{TCO}/(V_{CC} - V_{SNS}))$$

$$RT2 = ((T2 * R_{LTF}) - (T1 * R_{TCO}))/(T1 - T2)$$

$$RT1 = (RT2 * T1)/(R_{LTF} + RT2)$$

Table A-1. 10K NTC Thermistor Types and Resistance Values

Temperature (°C)	Nominal Resistance (Ω) at Temperature			
	Keystone Carbon Co. RL0703-5744-103-S1 (Tel: 814/781-1591)	Philips Components 2322-640-63103 (Tel: 407/743-2112)	Fenwal Electronics Type 16; 197-103LA6-A01 (Tel: 508/478-6000)	Thermometrics C100Y103J (Tel: 908/287-2870)
-30	188172	173900	177000	-
-25	138043	128500	-	-
-20	102263	95890	97070	-
-15	76461	72230	-	-
-10	57672	54890	55330	-
-5	43864	42070	-	-
0	33630	32510	32650	29588
5	25988	25310	-	23515
10	20243	19860	19900	18813
15	15889	15690	-	15148
20	12562	12490	12490	12271
25	10000	10000	10000	10000
30	8013	8060	8057	8195
35	6461	6536	-	6752
40	5241	5331	5327	5593
45	4276	4373	-	4656
50	3507	3606	3603	3894
55	2894	2989	-	3273
60	2400	2490	2488	2762
65	2001	2085	-	2342
70	1677	1753	1752	1993.7
75	1412	1481	-	1704.0
80	1194	1256	1258	1462.0
85	1014	1070	-	1259.1
90	865.2	915.5	917.7	1088.3
95	741.0	786.1	-	943.9
100	636.9	677.5	680.0	821.4

Application Note Revision History

Change No.	Page No.	Description	Nature of Change
1	2-81, 2-83	Changed thermistor values on Figures 9 and 10	Correction
1	2-80 – 2-83	Added component R33 to Figure 9 and Table 5 and R33 and D17 to Figure 10 and Table 6	Correction for cold temperature charge initiation
1	2-83	Corrected R1 value	Was 6.34K; is 63.4K

Note: Change 1 = Dec. 1992 B changes from Oct. 1992 A.

BENCHMARQ

Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC

Introduction

This application note describes the use of the bq2003 Fast Charge IC as the modulator in a buck-type switch-mode regulator to fast charge NiCd and NiMH batteries. Please refer to the application note entitled "Using the bq2003 to Control Fast Charge" for a discussion of bq2003 charge control operation and for descriptions of non-switch-mode applications that gate current-limited sources to control battery charging.

Examples for additional applications are being developed. Please contact Benchmarq if your application is not supported by one of these examples.

The bq2003 is targeted for applications requiring state-of-the-art fast-charging performance at minimal cost. It provides sophisticated full-charge detection techniques such as $\Delta T/\Delta t$ (delta temperature/delta time) and $-\Delta V$ (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2003 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

The bq2003 may serve as a controller to provide a switch-mode current source configuration for battery charging. Switch-mode current source regulation is much more efficient than linear current-limited regulators.

The electrical and thermal requirements of the application determine the configuration used with the bq2003. If the charge supply is either current- or power-limited at a level compatible with fast charging the battery, switch-mode operation may not be needed. The use of a gated current configuration as described in "Using the bq2003 to Control Fast Charge" is most likely more economical.

If the charge current in a switch-mode application is less than 3A, a p-channel MOSFET buck-type power stage is generally recommended. This is desirable because of the minimal number of support components required for the bq2003. If the switch-mode charge current is above 3A, using an n-channel FET may be more economical. Several small signal support components must be added for gate drive of the n-channel MOSFET.

Thermal packaging requirements are often the practical limits in electronic design. Basic thermal management or component thermal stress/reliability issues can affect an otherwise successful product. The use of switching power-conversion techniques results in dramatically less heat being generated in the product.

A comparison of power loss demonstrates the advantage of switch-mode control versus linear control. Either may be used to charge a four-C-cell NiCd battery pack from a 12V DC source at a rate of 2A. Loss in the switch-mode circuit may be held below 2W, whereas loss in the linear circuit can be above 12W.

Operational Aspects

In Figures 1 and 2, the bq2003 MOD pin controls the switching transistor Q1. In the switch-mode operation, the SNS pin is driven by the high side of the sense resistor R26. The current waveform of the inductor is represented by a voltage waveform across R26. MOD transitions from high to low after SNS ramps up to 0.250V and from low to high after SNS ramps down to 0.220V. This action sustains a self-referenced oscillation about these two thresholds.

Both V_{TS} and V_{BAT} are referenced to V_{SNS} by an internal A-to-D converter. For this reason, both the TS and BAT pins must be well-coupled to SNS using the associated capacitors (C7 and C8) and resistors (R5 and R6). If the waveforms at TS and BAT are viewed with an oscilloscope, the AC content found at SNS is seen at TS and BAT. This is normal.

A resistor (R7) is placed in series with the Q3 gate to drive a small signal-switching FET, Q3. Internal bq2003 noise is lowered with this resistor in place.

V_{LTF}, V_{HTF}, and V_{TCO} are voltage-reference points monitored on the TS pin to qualify charge initiation and termination on temperature. Operation of the bq2003 in a non-switch-mode application is described fully in the application note entitled "Using the bq2003 to Control Fast Charge."

When the bq2003 is used as a switch-mode controller, the application of these reference points is somewhat different:

- Prior to charge initiation, $V_{SNS} = V_{SS}$.
- While charging, V_{SNS} (average) = 0.235V.

Because the bq2003 internal A-to-D converter measures differentially between V_{TS} and V_{SNS}, component selection for temperature qualification of charge initiation must be done assuming V_{SNS} = 0V, and component selection for temperature qualification of charge termination must be done assuming V_{SNS} = 0.235V.

V_{TS} is the voltage at the node of RT1, RT2, and the thermistor. The voltage is derived from reference V_{CC} (5V) by RT1 connected to V_{CC} and RT2 in parallel with the thermistor connected to SNS. Prior to charging, the voltage being divided is V_{CC}. When switching regulation is active, the bottom side of RT2 and the thermistor is biased positively by 0.235V, reducing the reference voltage to 4.65V.

Because V_{TCO} and V_{LTF} are both referenced to V_{CC}, V_{TS} for a particular temperature represents a colder temperature when the switch-mode is inactive than when the switch-mode is active. This effect could negate the HTF charge initiation qualification threshold. V_{HTF} is 1/8 * V_{LTF} + 7/8 * V_{TCO}. V_{TCO} is a threshold selected for use when the switch-mode is active. V_{LTF} is internally fixed at 0.4 * V_{CC}. The values of RT1, RT2, and the thermistor that define the LTF temperature (charging off) also define the TCO temperature (switch mode on). The resulting HTF temperature with charging off approaches or may even be above the TCO temperature (switch mode on), limiting the uselfulness of HTF to qualify the start of charge.

The bq2003 bQuick™ design disk is available to optimize these component values and thresholds for specific application objectives.

P-Channel MOSFET Buck-Topology Switch-Mode Charger

In this example, the bq2003 is used to implement a switching regulator/charge controller that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 3A.

Figure 1 is a standard configuration for a pFET switch-mode charger. MOD drives a small signal DMOS FET, Q3. When MOD is high, Q3 is on, turning on Q1 via the path through D8 and D9.

L1 inductor current ramps up linearly while MOD is high. L1 current is in series with the battery and R26. The resulting voltage across R26, V_{SNS}, is delivered via R4 to C6 at the SNS pin. The L1 inductor current ramps up linearly until V_{SNS} reaches 0.250V, at which time MOD goes low and Q1 turns off. A flux reversal occurs in L1, causing D10 to conduct. Charge is now being transferred from L1 into the battery. The L1 current ramps down linearly until V_{SNS} reaches 0.220V. At this point the cycle repeats with MOD going high.

For input voltages that are higher than the rated Q1 safe operating gate voltage, Zener diode D9 can be placed in series with the drain lead of Q3. The Zener voltage should be sized to allow full Q1 enhancement while Q3 is conducting. See Table 1.

Table 1. Lookup Table for D9 Selection

+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

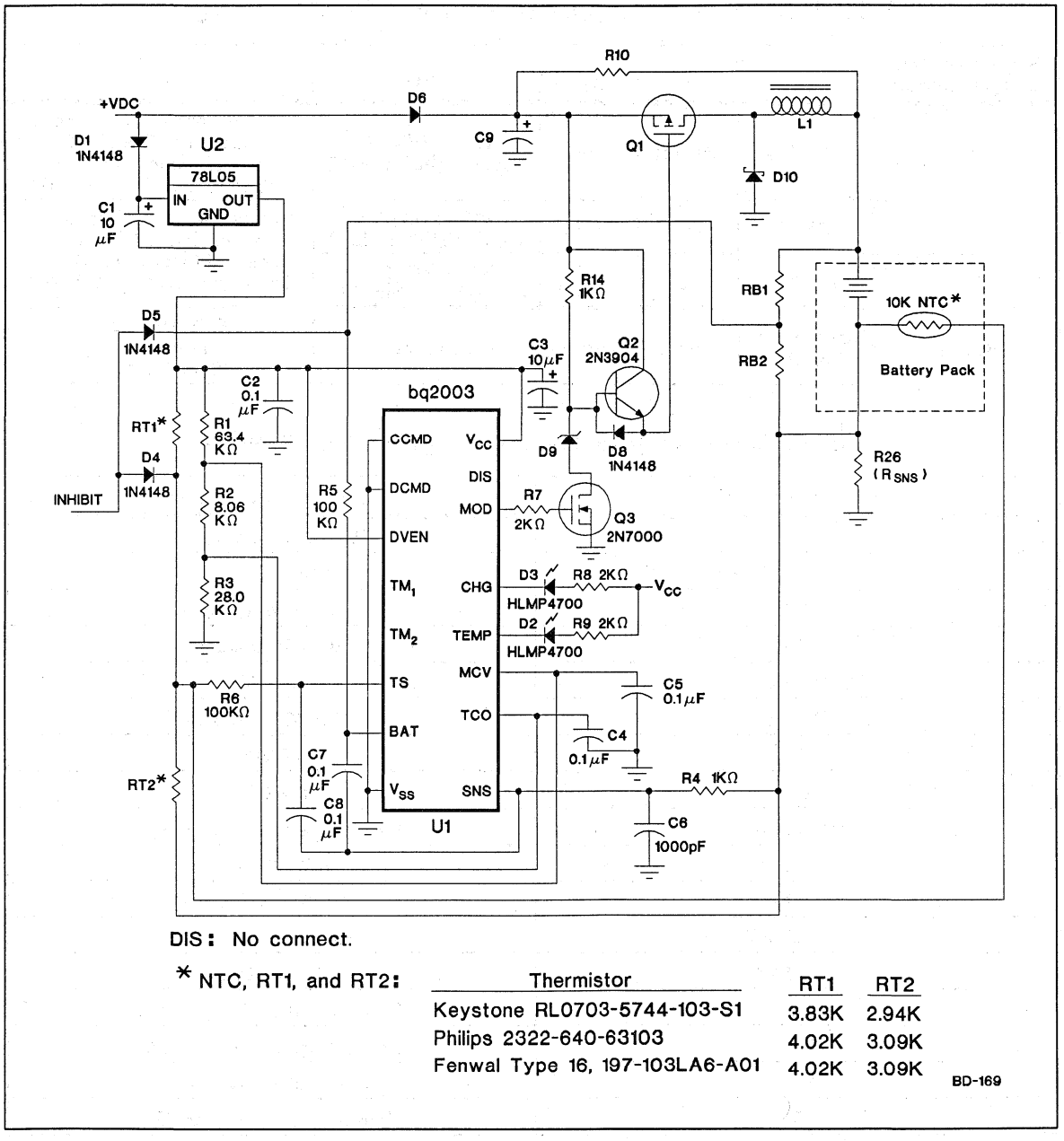
Capacitor C9 is used to provide a low-impedance for the Q1 source lead. Without C9 in place, Q1 can be connected to an overly inductive voltage supply. D6 is a blocking diode that keeps the battery from discharging via U2 during removal of the DC power source input.

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; ΔT/Δt at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 2-85 of the application note entitled "Using the bq2003 to Control Fast Charge") are determined by the designer. R26 is selected such that I_{CHG} * R26 = 0.235V.

The values of RB1 and RB2 to complete this schematic may be selected from Table 2 in the application note entitled "Using the bq2003 to Control Fast Charge."

Note: Temperature control and qualification may be disabled by tying the TCO pin to V_{SS} and fixing the voltage on the TS pin to 0.1 * V_{CC}.

Table 2 lists suggested components for different-rate chargers. Table 3 lists other components shown in Figure 1.



DIS: No connect.

* NTC, RT1, and RT2:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K

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Figure 1. P-Channel MOSFET Switching-Mode Charger

Table 2. Suggested Components—P-Channel MOSFET Charger

Suggested Max. Charging Current	Q1	D6	D10	C9	L1
1A	IRF9Z14	1N4001	1N5818	ECA-1VFQ390 39µF/35V/460mΩESR	30 turns, #26 AWG, wound on Magnetics, Inc., P/N 77040 core; nominal inductance 59µH; GFS Mfg., Inc., P/N 92-2156-1
2A	IRF9Z24	1N5821	1N5821	ECA-1VFQ560 56µF/35V/300mΩESR	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
3A	IRF9Z34	1N5821	1N5821	ECA-1VFQ121 120µF/35V/170mΩESR	
Source	International Rectifier	Motorola	Motorola	Panasonic	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 3. Other Components—P-Channel MOSFET Charger

Component Name	Component Description
C1	10µF 35V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 10V electrolytic
C6	1000pF ceramic
D1, D4, D5, D8	1N4148
D2, D3	HLMP 4700 red LED
Q2	2N3904
Q3	2N7000
R1, R2, R3	User-defined 1% ¼W or ⅛W
R4	1KΩ 5% ¼W
R5, R6	100KΩ 5% ¼W or ⅛W
R7, R8, R9	2KΩ 5% ¼W or ⅛W
R10, R26	User-defined
RB1	User-defined 1% ¼W or ⅛W
RB2	User-defined 1% ¼W or ⅛W
RT1	User-defined 1% ¼W or ⅛W
RT2	User-defined 1% ¼W or ⅛W
U1	bq2003
U2	LM78L05ACZ

N-Channel MOSFET Buck-Topology Switch-Mode Charger

The advantage of an n-FET buck topology is the price-versus-performance benefit of the n-FET family. The disadvantage is the number of additional components required to support it.

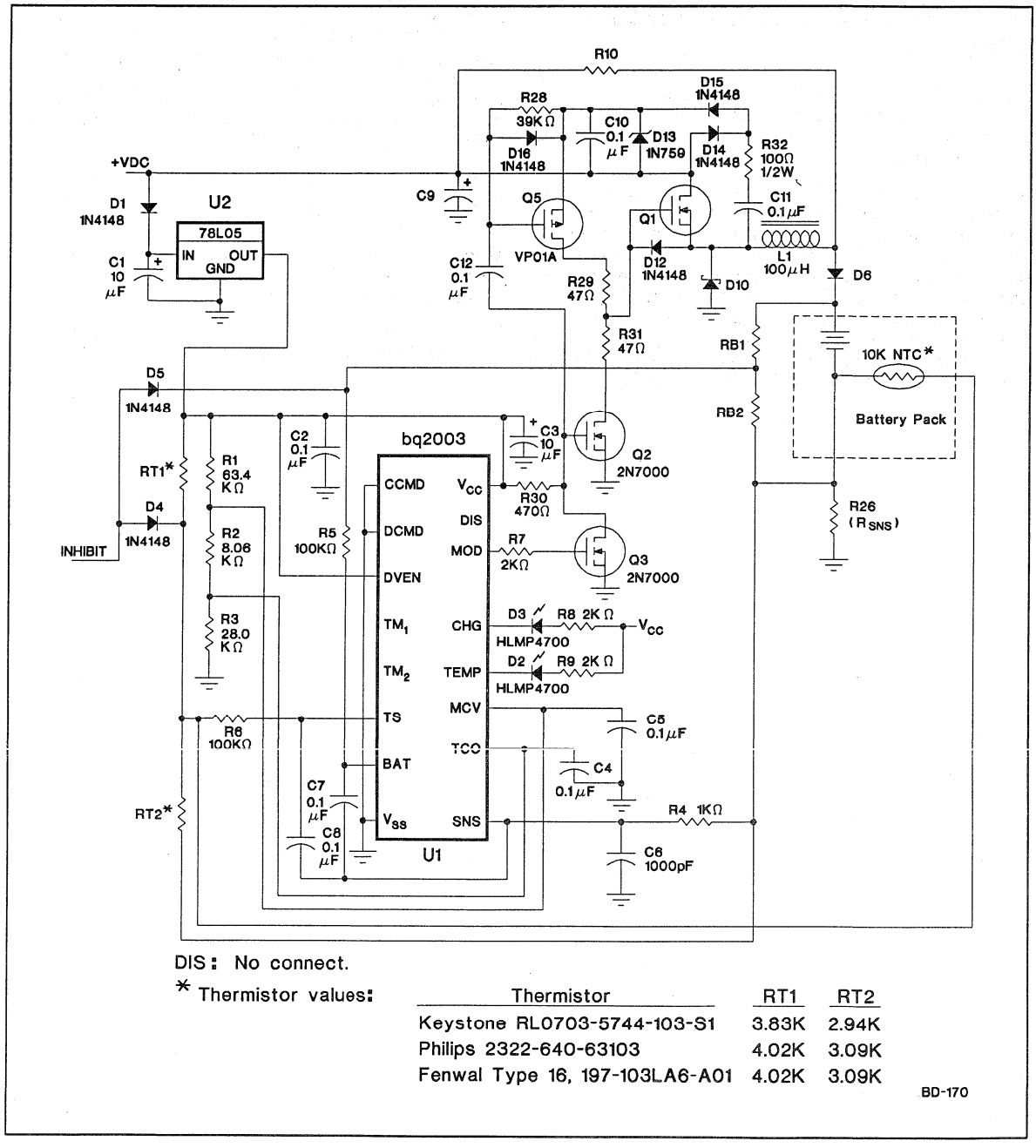
The schematic in Figure 2 is a standard configuration for an nFET switch-mode charger that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 9A. The Q1 gate must be driven positive with respect to the drain in this application to provide full enhancement of the device. When catch diode D10 is conducting, C11 is charged. When Q1 is conducting, C11 is charging C10. This charge pump allows adequate voltage to drive Q1 into full enhancement via Q5. As Q2 conducts, the Q1 gate charge is depleted, causing Q1 to turn off.

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is disabled (DVEN low), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; ΔT/Δt at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 2-85 of the application note entitled "Using the bq2003 to Control Fast Charge") are determined by the designer. R26 is selected such that $I_{CHG} * R26 = 0.235V$.

The values for RB1 and RB2 to complete this schematic may be selected from Table 2 in the application note entitled "Using the bq2003 to Control Fast Charge."

Note: Temperature control and qualification may be disabled by tying the TCO pin to V_{SS} and fixing the voltage on TS pin to $0.1 * V_{CC}$.

Table 4 lists suggested components for different-rate chargers. Table 5 lists other components shown in Figure 2.



DIS: No connect.

* Thermistor values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K

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Figure 2. N-Channel MOSFET Switching-Mode Charger

Table 4. Suggested Components—N-Channel MOSFET Charger

Suggested Max. Charging Current	Q1	D6	D10	C9	L1
3A	IRFZ34	1N5821	1N5821	ECA-1VFQ121 120µF/35V/170mΩESR	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
6A	IRFZ44	MBR735	MBR735	ECA-1VFQ391 390µF/35V/55mΩESR	33 turns, #18 AWG, wound on Magnetics, Inc., P/N 77310 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2158-1
9A	IRFZ48	MBR1035	MBR1035	ECA-1VFQ681 680µF/35V/34mΩESR	25 turns, #16 AWG, wound on Magnetics, Inc., P/N 77930 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2159-1
Source	International Rectifier	Motorola	Motorola	Panasonic	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 5. Other Components—N-Channel MOSFET Charger

Component Name	Component Description
C1	10µF 35V electrolytic
C2, C4, C5, C7, C8, C10, C11, C12	0.1µF ceramic
C3	10µF 10V electrolytic
C6	1000pF ceramic
D1, D12, D14, D15, D16	1N4148
D2, D3	HLMP4700 red LED
D13	1N759 12V 500mW Zener
Q2, Q3	2N7000
Q5	VP01A
R1, R2, R3	User-defined 1% ¼W or ⅛W
R4	1KΩ 5% ¼W or ⅛W
R5, R6	100KΩ 5% ¼W or ⅛W
R7, R8, R9	2KΩ 5% ¼W or ⅛W
R10, R26	User-defined
R28	2.7KΩ 5% ¼W or ⅛W
R29, R31	47KΩ 5% ¼W or ⅛W
R30	470KΩ 5% ¼W or ⅛W
R32	100KΩ 5% ½W or ⅛W
RB1	User-defined 1% ¼W or ⅛W
RB2	User-defined 1% ¼W or ⅛W
RT1	User-defined 1% ¼W or ⅛W
RT2	User-defined 1% ¼W or ⅛W
U1	bq2003
U2	LM78L05ACZ

Operating Switching Frequency

During Q1 on-time, the L1 current ramps up linearly. During Q1 off-time (D10 conduction), the L1 current ramps down linearly. The rate of rise and fall (slew rate) of L1 current is determined by the inductance value of L1 and the DC voltage placed across L1. The slew rate is usually different between Q1 conduction time and D10 conduction time. This is because the DC voltage across L1 is usually different during these two timing intervals.

The sum of these two timing intervals equals the switching period. The switching period reciprocal equals the switching frequency.

Use the following equation to estimate the switching frequency.

$$F = \frac{1}{\frac{L\left(\frac{0.030V}{R_{SNS}}\right)}{V_{DC}-(V_{BAT}+V_{SNS}+D6_{VF}+Q1_{DROP})} + \frac{L\left(\frac{0.030V}{R_{SNS}}\right)}{V_{BAT}+V_{SNS}+D10_{VF}}}$$

where:

- F = Frequency in Hertz
- L = L1 inductance in Henrys
- $D6_{VF}$ = D6 average forward voltage drop
- $D10_{VF}$ = D10 average forward voltage drop
- R_{SNS} = R26 value in ohms
- $Q1_{DROP}$ = Charge current times Q1 on-state-resistance
  = $(^{0.235V}/_{R_{SNS}})\ Q1_{RDSON}$
- V_{DC} = Input DC voltage
- V_{BAT} = Battery pack instantaneous voltage

Charge Current Regulation With Varying System Loads

Systems with an integrated charger and a constant-power external supply may not be capable of fast charging the batteries while simultaneously supporting system operation. In such cases the system operation takes priority, and the peak system energy demand must be supported.

In this situation, the charger designer has two options regarding charge during system operation:

1. The battery charging current may be held constant at a low level that is supportable during peak system operation loads. During periods of low system power demand, available power is not used. The charge time during system operation is typically quite long.
2. The battery charging current may be allowed to vary inversely with the system load. As the system power demand decreases, the charge rate increases and vice versa. For portable systems with varying load requirements (such as those using "power management"), this allows any surplus power during low system activity to be used for battery charging. The charge time during system operation depends on the average system power requirement, not the peak requirement.

Option 1 may be implemented when using the bq2003 as the charge current regulator by using the system V_{CC} as an "INHIBIT" signal to pull pins BAT and TS high when the system is on. (See Figures 1 and 2 and the System-Controlled Charge Inhibition discussion in "Using the bq2003 to Control Fast Charge.") When the system is on, fast charge is inhibited. The only charge path is the trickle resistor.

Option 2A may be implemented using the bq2003 as the charge current regulator with the system load return at the high end of the sense resistor R26 (Figure 3). $\Delta T/\Delta t$ charge termination is enabled and $-\Delta V$ termination is disabled.

With a battery pack cell voltage ≥ 1V per cell, the system load always receives its required current. The system load current flows through R26 along with the battery charge current. The battery receives any difference between the programmed charge current and the system load current. If the system load current exceeds the programmed charge current, then no charge current will be delivered to the battery. The system load current biases the SNS voltage via R26, which limits the buck regulator's current delivered to the battery. The total

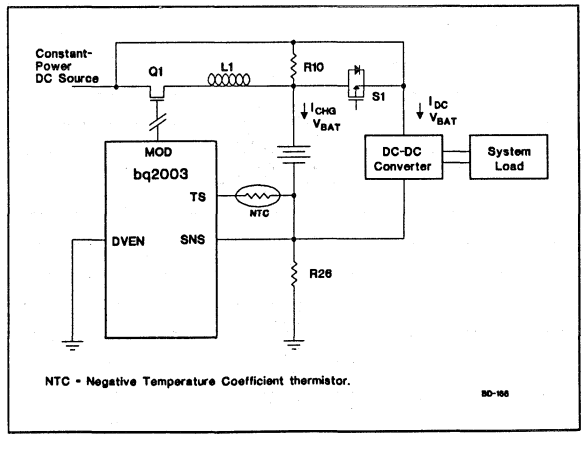


Figure 3. Option 2A

available power may be allocated between the battery charge and system operation such that power used = (I_{CHG} + I_{DC}) • V_{BAT}.

Using this method, the sense resistor R26 and its associated energy penalty are not in the battery discharge path. The charge current is regulated in a variable fashion such that R26 • (I_{CHG} + I_{DC}) = 0.235V.

Charge current regulation may occur until I_{DC} • R26 ≥ 0.250V. Above this point, the MOD output is held low (off). When actively switching, the MOD frequency remains very nearly constant.

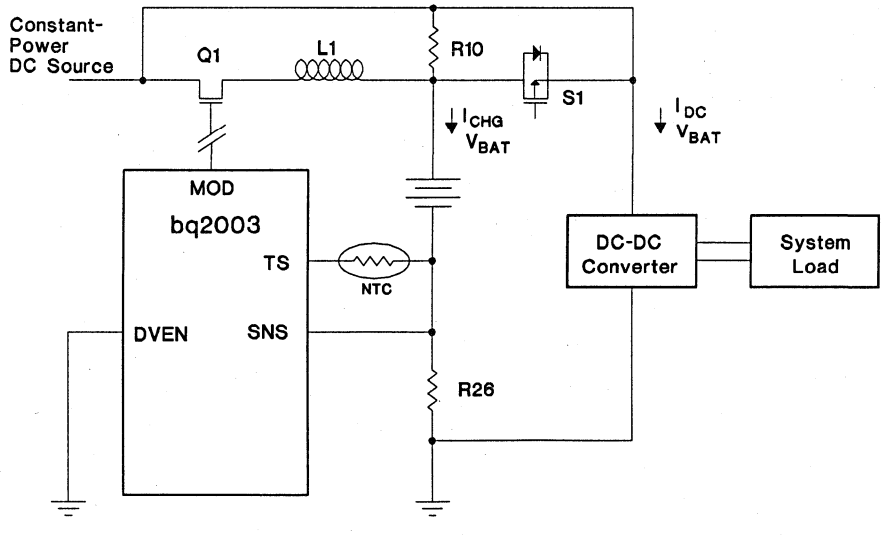
If the battery voltage is extremely low, the bq2003 does not begin charging until the battery trickle charges to 1V per cell. This protects the system voltage from being pulled down to an inoperable range by a very low battery.

-ΔV is disabled to prevent false terminations due to the varying charge current and the battery's internal impedance. Slight but significant voltage perturbations at V_{BAT} can cause a false -ΔV charge termination during variations in battery charge current in this configuration. ΔT/Δt, however, is *not* affected by variations in charge current because the battery's physical mass has a relatively slow time constant that naturally integrates all variations.

Switch S1 is turned on for battery operation and off during charge. Switch S1 is driven by appropriate logic defined by the needs of the application. The presence or absence of an input DC power source could control this logic. A Schottky diode is a simpler alternative to S1, but the voltage drop may not be desirable.

Option 2B is another variable charge rate approach (Figure 4). This option may be preferred if the available power is considerably more than the maximum I_{CHG} • V_{BAT} (ignoring voltage loss). In the first approach, the system load return is to the high end of the sense resistor R26, limiting the power used to approximately (I_{CHG} + I_{DC}) • V_{BAT}, with I_{CHG} = 0 when I_{DC} ≥ maximum I_{CHG}.

For this second approach to use all the available power, the system load return is at the low end of the sense resistor. This accomplishes the fastest possible charge during system operation, but carries a penalty during battery operation because of the energy and voltage loss from discharge through the sense resistor (or the cost and impedance of a switch to bypass the sense resistor).



NTC = Negative Temperature Coefficient thermistor.

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Figure 4. Option 2B

Layout and EMI Considerations

The best approach to PC board layout follows the strict rule of a single-point ground return. Sharing high current ground with small signal ground causes undesirable noise on the small signal nodes. Referencing Figures 1 and 2, C2 and C3 should be placed as close as possible to the V_{CC} pin. C6 should be placed at the SNS pin. C7 and C8 should be associated between the TS/SNS and the BAT/SNS pins, respectively, with short leads. Isolation resistors R5 and R6 should be placed close to the BAT and TS pins.

Layout of power components C9, D10, L1, Q1, and R26 should reduce lead-length paths between these components to an absolute minimum.

If a dual-layer PC board is used, route signal lines on the solder side. This leaves the component side to be used as a ground plate. This technique reduces noise on adjacent nodes within the circuit and helps reduce EMI by giving the high-energy fields a ground plane to work against.

pFET and nFET Layout Examples

Figures 5–7 illustrate the layout of the p-channel MOSFET switch-mode charger board, and Figures 8–10 illustrate the layout of the n-channel MOSFET switch-mode charger board.

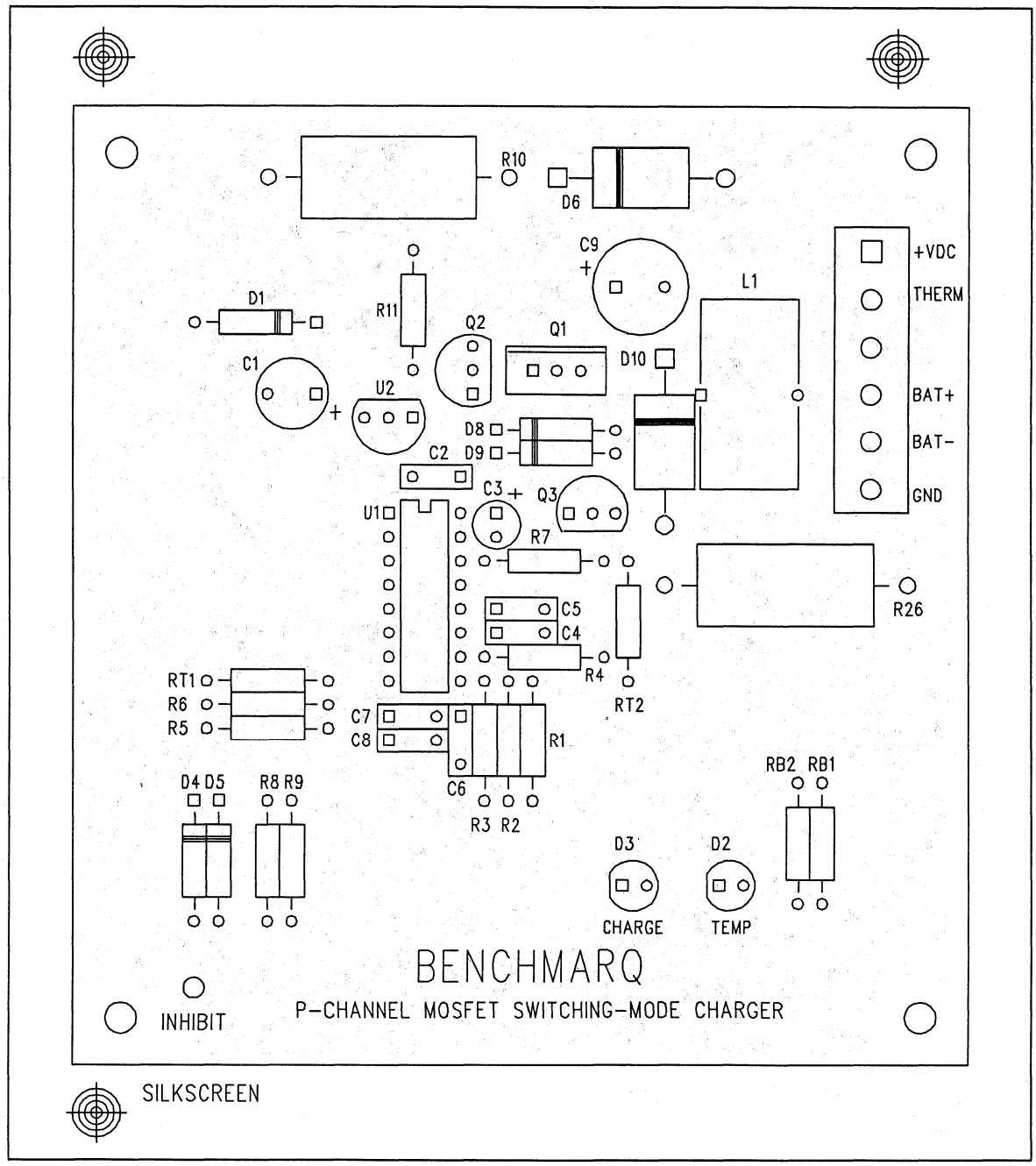


Figure 5. P-Channel MOSFET Switching Charger—Silkscreen

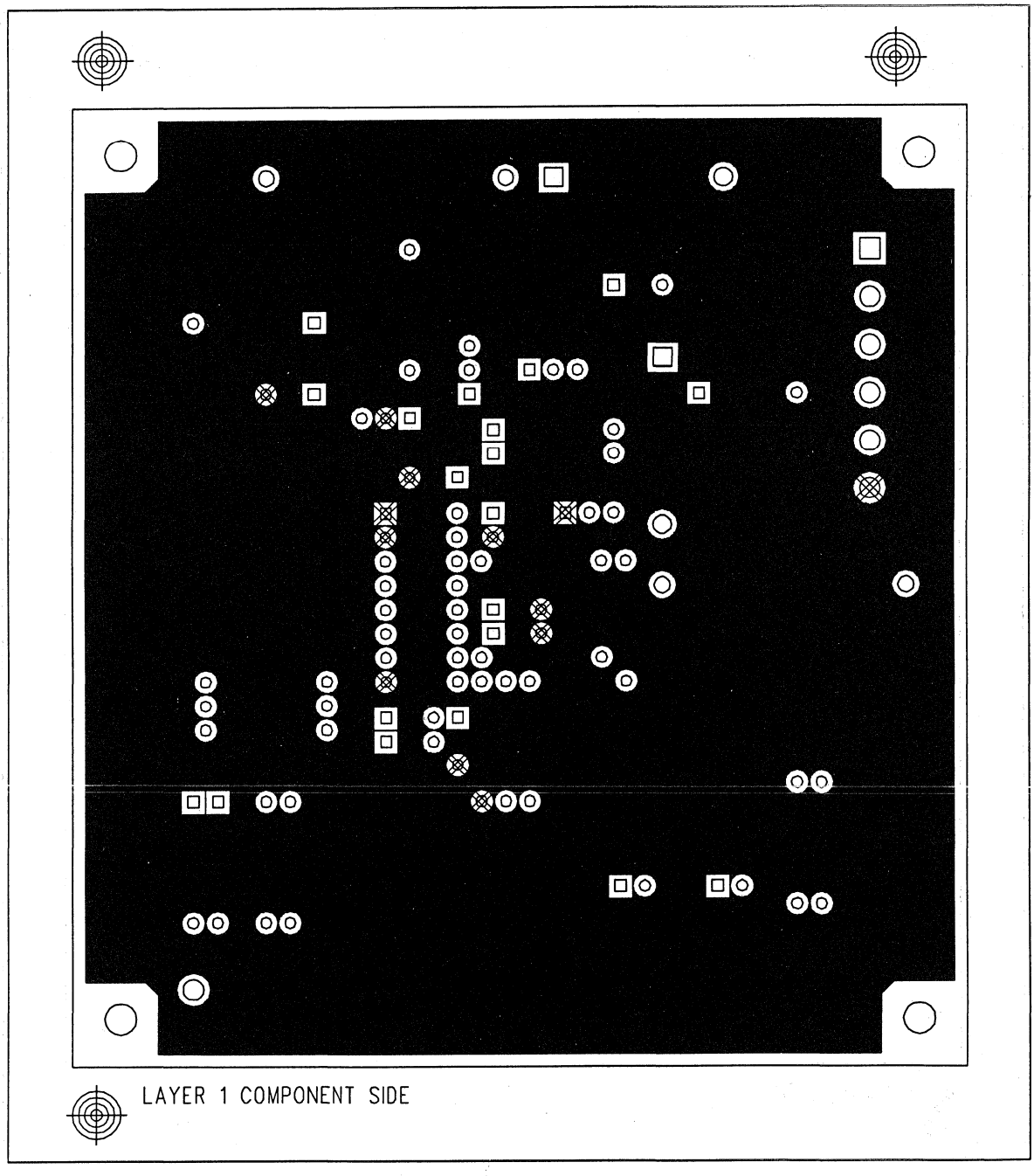


Figure 6. P-Channel MOSFET Switching Charger—Component Side

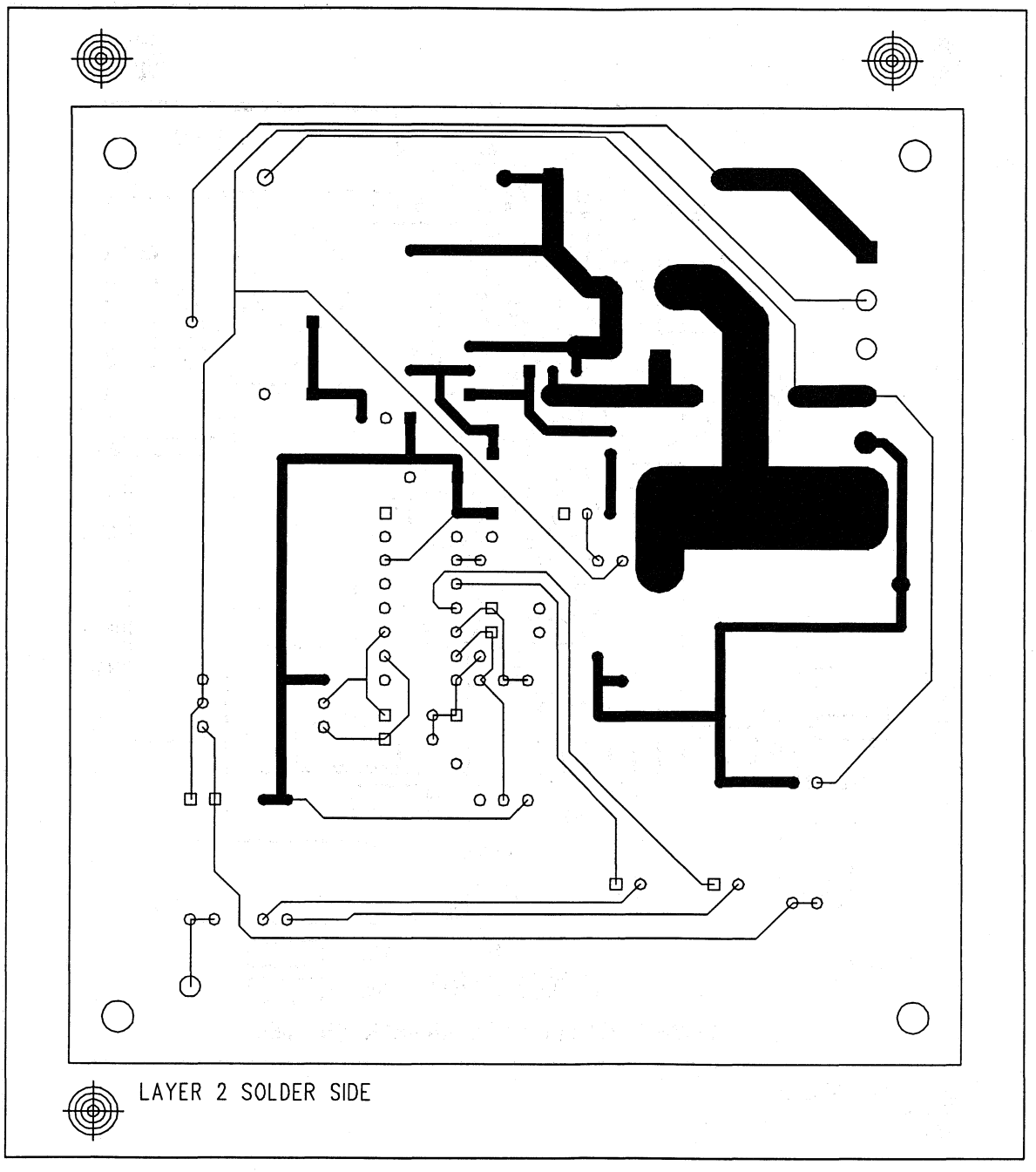


Figure 7. P-Channel MOSFET Switching Charger—Solder Side

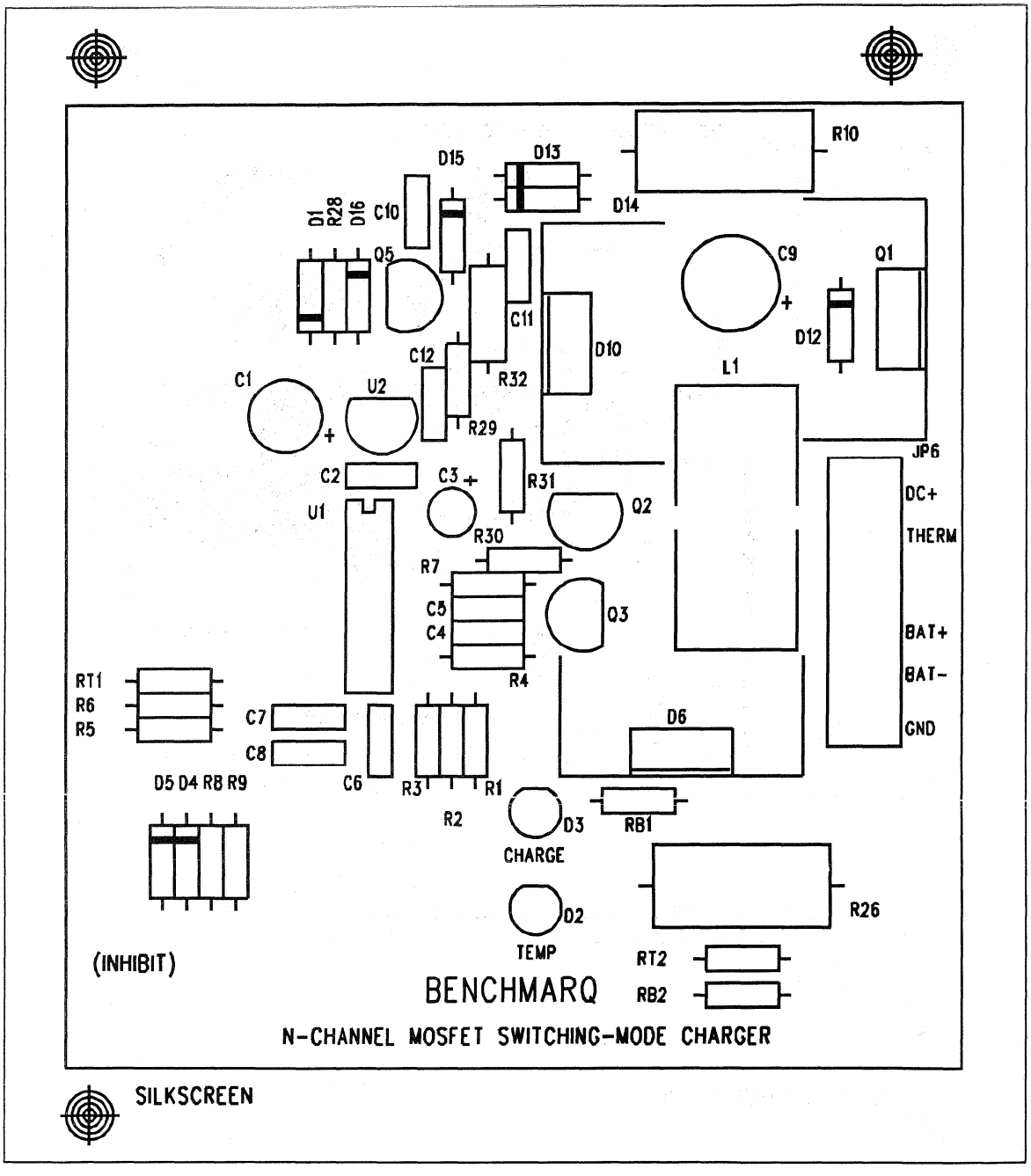


Figure 8. N-Channel MOSFET Switching Charger—Silkscreen

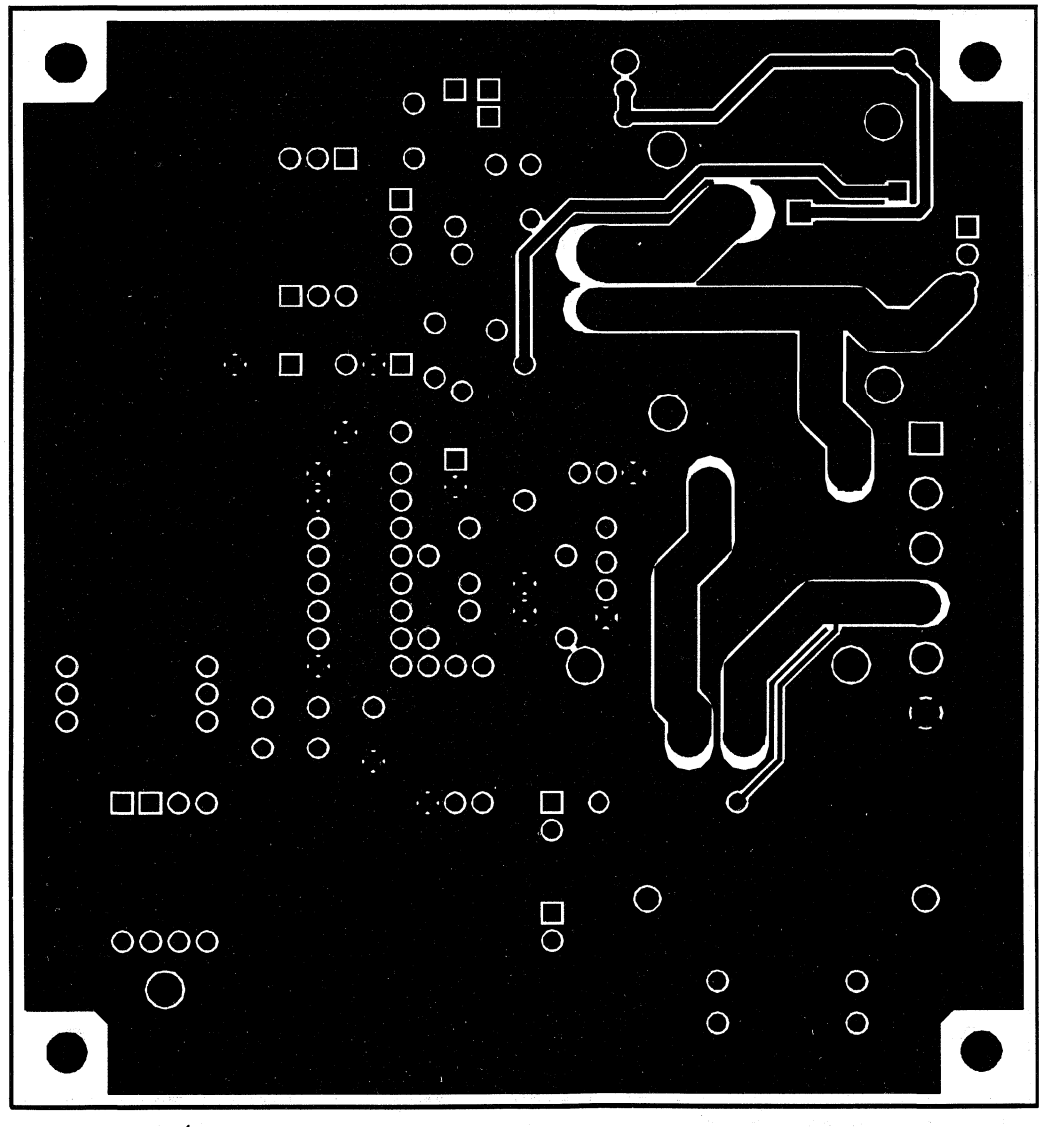


Figure 9. N-Channel MOSFET Switching Charger—Component Side

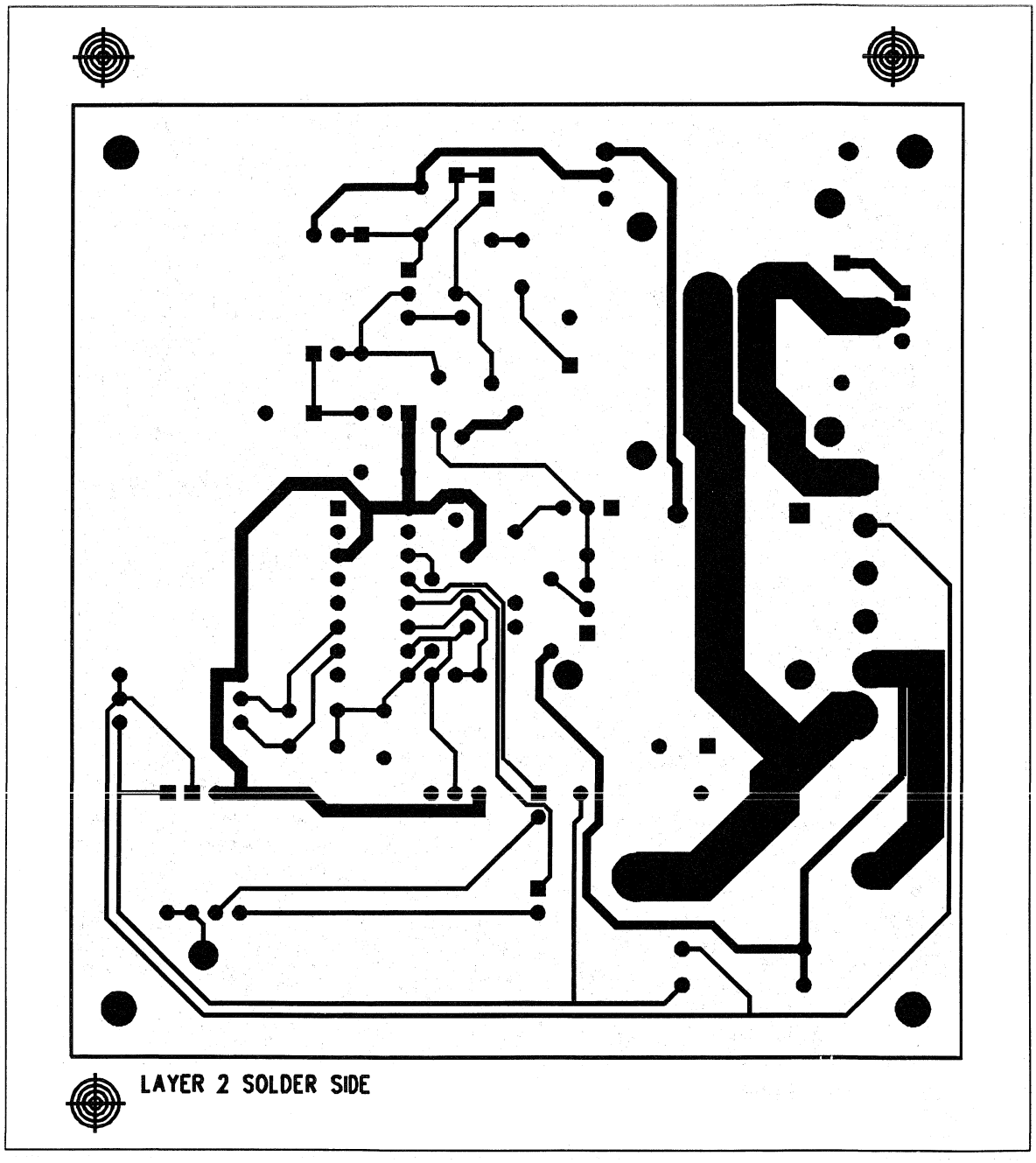


Figure 10. N-Channel MOSFET Switching Charger—Solder Side

BENCHMARQ

Using the bq2003

With High-Side Current Sensing In a Switch-Mode Charger

Introduction

This application note describes the use of the bq2003 in special applications that require high-side current sensing. Some system flexibility is gained with high-side current sensing. The DC source, the minus side of the battery, and the system load are all one common ground point. This simplifies the power-grounding architecture in applications such as automotive chargers for radio products.

Such applications may not allow for the standard low-side current sensing as referenced in the application note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC."

The Circuit

The circuit shown in Figure 1 is similar to the circuit described in Figure 1 of the application note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC," with the following exceptions.

The current-sensing resistor (R12) is placed between the inductor (L1) and the positive side of the battery. To translate the voltage waveform across R12 to the bq2003 SNS pin, a differential amplifier must be used.

The differential amplifier (U3A) is configured with a gain factor of one. Thus, this equation still applies:

$$I_{CHG} = \frac{0.235}{R12}$$

Depending on the application, a protection method to limit the U3A supply voltage may be needed. The TLC272 has a maximum supply voltage of 18 VDC. A small-signal Zener diode (15V nominal, 1N965A) could also be used to clamp this voltage to a safe level with a series current-limiting resistor.

Note that the U3A input voltages must always be less than the U3A supply voltage. To help meet this requirement, the four equal-value support resistors associated with U3A provide the secondary function of dividing the input voltages by half.

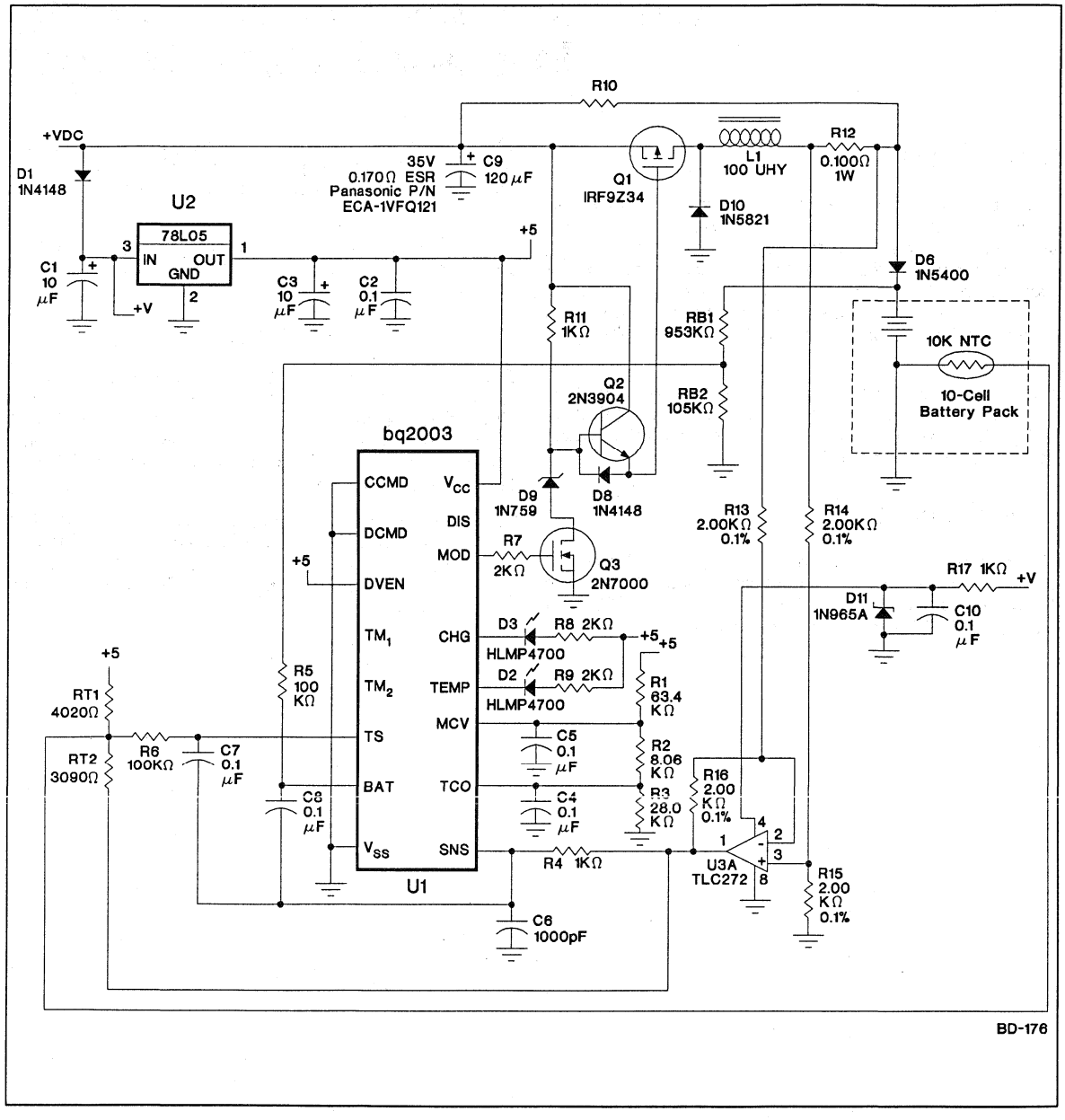


Figure 1. High-Side Sensed p-Channel Diagram

BENCHMARQ

bq2004

Fast Charge IC

2

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Supports logic-level-controlled low-power mode (< 5µA standby current)
- Optional peak voltage detect (PVD) fast-charge termination
- Flexible current regulation:
  - Frequency-modulated switching current regulator
  - Gating control for use with external regulator
- 150-mil SOIC is ideal for integration into portable systems
- Pre-charge qualification for temperature and voltage faults
- Programmable LED outputs display battery and charge status
- Fast charge termination by Δ temperature/Δ time, -ΔV or peak voltage, and maximum temperature, time, and voltage

General Description

The bq2004 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Flexible control of constant-current or current-limited charging supply allows the bq2004 to be the basis of a cost-effective system-integrated charger for batteries of two or more cells. High-efficiency switched constant-current regulation is accomplished using the bq2004 as a frequency-modulated controller. The bq2004 may alternatively be used with a transistor to gate an external charging current or in a cost-effective frequency-modulated linear regulator.

Switch-activated or automatic discharge-before-charge allows bq2004-based chargers to support battery conditioning and capacity determination.

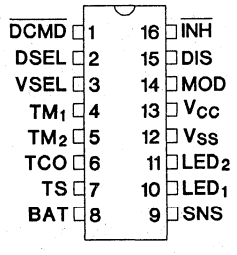
Fast charge may begin on application of V_{CC} to the bq2004, replacement of the battery, or use of the $\overline{INH}$ pin. For safety, fast charge is inhibited until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV) or peak voltage detect
- Maximum temperature
- Maximum time
- Maximum voltage

Following fast charge, the bq2004 proceeds with a pulsed top-off charge (if enabled) and a pulsed trickle charge.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-47

Pin Names

$\overline{DCMD}$	Discharge command	SNS	Sense resistor input
DSEL	Display select	LED_1	Charge status output 1
VSEL	Voltage termination select	LED_2	Charge status output 2
TM_1	Timer mode select 1	V_{SS}	System ground
TM_2	Timer mode select 2	V_{CC}	5.0V ±10% power
TCO	Temperature cutoff	MOD	Charge current control
TS	Temperature sense	DIS	Discharge control output
BAT	Battery voltage	$\overline{INH}$	Charge inhibit input

Pin Descriptions

$\overline{DCMD}$ **Discharge-before-charge control input**

$\overline{DCMD}$ controls the discharge-before-charge function of the bq2004. A negative-going pulse on $\overline{DCMD}$ initiates a discharge to EDV (0.4 * V_{CC}) followed by a charge if conditions allow. By tying $\overline{DCMD}$ to ground, automatic discharge-before-charge is enabled by the application of power, by battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. $\overline{DCMD}$ is pulled up internally.

DSEL **Display select input**

This three-level input controls the $LED_{1,2}$ charge status indication. See Table 2 for details.

VSEL **Voltage termination select input**

This three-level input controls the voltage-termination technique used by the bq2004.

TM_1, TM_2 **Timer mode inputs ($TM_{1,2}$)**

TM_1 and TM_2 are three-level inputs that control the settings for the fast charge safety timer and "top-off"/trickle charge control. See Table 3 for details.

TCO **Temperature cut-off threshold input**

Minimum allowable battery temperature-sensor voltage. If the potential between TS and SNS is less than the voltage at the TCO input, then any fast charging or top-off charging is terminated.

TS **Temperature sense input**

Input for battery temperature monitoring negative temperature coefficient (NTC) thermistor.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor network. This provides the reference potentials for both the TS and BAT pins. If SNS is connected to V_{SS}, then MOD switches high at the beginning of charge, and low at the end of charge. See Figure 1 and Table 1 for details.

BAT **Battery voltage input**

BAT is the battery voltage sense input. This potential is limited to between 0.4 * V_{CC} and 0.8 * V_{CC} and is generally developed by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

LED_1, LED_2 **Charge status outputs**

Push-pull outputs indicating charging status. See Figure 1 and Table 2 for details.

V_{SS} **Ground**

V_{CC} **V_{CC} supply input**

5.0V, ±10% power input.

MOD **Charge current control output**

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow. See Figure 1 and Table 1 for details.

DIS **Discharge control output**

Push-pull output used to control an external transistor to discharge the battery before charging. DIS is active high.

$\overline{INH}$ **Charge inhibit input**

When low, the bq2004 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a charge cycle is initiated. See page 8 for details.

Functional Description

Figure 1 illustrates charge control and display status during a bq2004 charge cycle. Table 1 outlines the various bq2004 operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2004 initiates a charge by the application of power on V_{CC}, by a battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. Control of the charge action is then determined by the inputs from $\overline{DCMD}$, VSEL, TS, BAT, and $TM_{1,2}$.

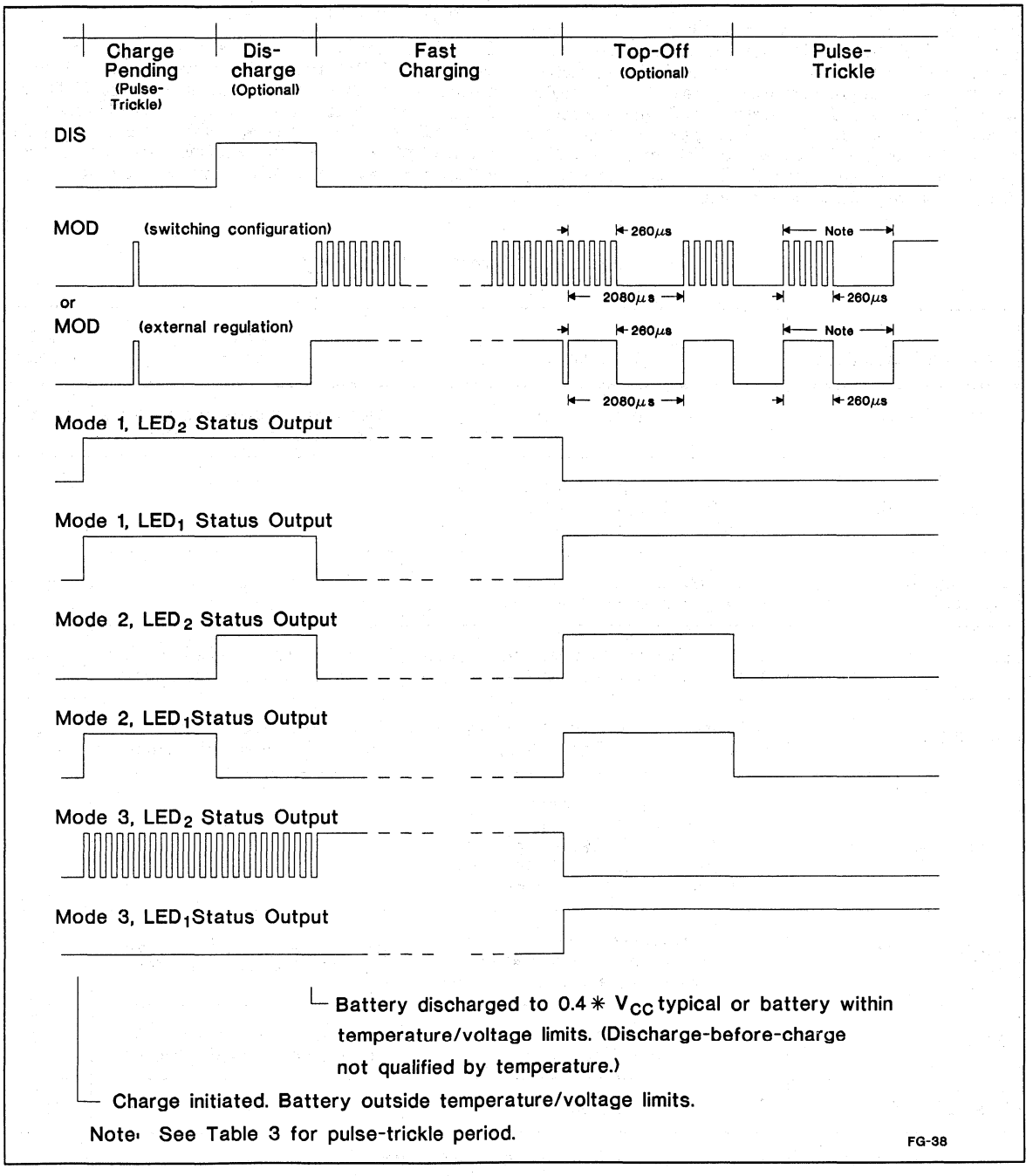


Figure 1. Example Charging Action Events

Following charge initiation, the bq2004 checks for acceptable battery temperature (between LTF—low-temperature fault and HTF—high-temperature fault) and battery voltage (between EDV—end-of-discharge voltage and MCV—maximum cell voltage). Fast charging begins when the voltage and temperature conditions are within these limits. Once the fast charging process begins, the bq2004 tests for the full-charge conditions: $\Delta T/\Delta t$ and/or $-\Delta V$ or peak voltage detect (PVD), with temperature, time, and voltage safety terminations.

Charge Status Indication

Table 1 outlines the various charge action states and the associated MOD and DIS output states. Table 2 describes the charge status indicated by the LED_1 and LED_2 outputs, which may be connected directly to an LED indicator. **In all cases, if the battery voltage at the BAT pin exceeds the maximum cell voltage (0.8 * V_{CC}), the LED_1 and LED_2 outputs are held low.**

Table 1. bq2004 Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output
Battery absent	$V_{CELL} \geq V_{MCV}$	Trickle charge activated per V_{SNS} for period specified in Table 3	Low
Charge initiation	V_{CC} applied, V_{CELL} drops from $\geq V_{MCV}$ to $< V_{MCV}$ (battery insertion), or $\overline{INH}$ transitions low to high with battery inserted	-	–
Discharge-before-charge (optional)	$\overline{DCMD}$ high-to-low pulse or tied to V_{SS} on charge initiation; $V_{EDV} < V_{CELL} < V_{MCV}$	Low	High
Pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$[1] or $V_{TEMP} \leq V_{HTF}$ or $V_{CELL} < V_{EDV}$	Trickle charge activated per V_{SNS} for period specified in Table 3	Low
Fast charging	Charge initiation occurred and $V_{HTF} < V_{TEMP} < V_{LTF}$[1] and $V_{EDV} \leq V_{CELL} < V_{MCV}$	Low if $V_{SNS} > 250mV$, nominal; high if $V_{SNS} < 200mV$, nominal	Low
Charge complete	$-\Delta V \geq 6mV$/cell or PVD ≥ 0 to 3mV/cell or $\Delta V_{TEMP}/\Delta T > 14mV$/minute or $V_{TEMP} < V_{TCO}$ or $V_{TEMP} > V_{LTF}$[1] or maximum time or voltage	–	–
Top-off (optional; see Table 3)	Charge complete and top-off time not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} (see fast charging state) for 260µs of every 2080µs	Low
Trickle	Charge complete and top-off disabled or top-off complete	Trickle charge activated per V_{SNS} for period specified in Table 3	Low
Charge inhibit	$\overline{INH}$ low	Z	Z

Definitions: $V_{CELL} = V_{BAT} - V_{SNS}$; $V_{MCV} = 0.8 * V_{CC}$; $V_{EDV} = 0.4 * V_{CC}$;
$V_{TEMP} = V_{TS} - V_{SNS}$; $V_{LTF} = 0.4 * V_{CC}$; $V_{HTF} = ((1/4 * V_{LTF}) + (3/4 * V_{TCO}))$.

Note: 1. The low-temperature fault is not considered when PVD is enabled.

Table 2. bq2004 LED Output Summary

Mode 1	Charge Action State	LED_1	LED_2
DSEL = V_{SS}	Battery absent	Low	Low
	Fast charge pending or a discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Charge complete, top-off, and/or trickle	High	Low
Mode 2	**Charge Action State**	**LED_1**	**LED_2**
DSEL = Floating	Battery absent, fast charge in progress or complete	Low	Low
	Fast charge pending	High	Low
	Discharge in progress	Low	High
	Top-off pending or in progress	High	High
Mode 3	**Charge Action State**	**LED_1**	**LED_2**
DSEL = V_{CC}	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	Low	1/8 second high 1/8 second low
	Fast charge in progress	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum and minimum allowable values. The battery voltage sense input, BAT, for a battery pack should be divided to between 0.8 * V_{CC} and 0.4 * V_{CC} for proper operation. A resistor-divider ratio of:

$$\frac{R1}{R2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the respective SNS pin. See Figure 2.

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2004.

The thermistor used for temperature measurement should have a negative temperature coefficient. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and SNS. See Figure 2.

Battery Removal Detection

Battery removal is sensed by V_{CELL} (V_{BAT} - V_{SNS}) rising above V_{MCV} (0.8 * V_{CC}). An external resistor, R_{EXT}, between the battery positive lead and the charging supply input pulls V_{CELL} above V_{MCV} to detect battery removal.

Initiating a Charge Action

A battery charge action is initiated with a battery insertion, application of V_{CC} to the bq2004, or a low-to-high transition on the $\overline{INH}$ pin. Battery insertion is recognized when the voltage at the BAT pin falls from above the internal V_{MCV} reference level to below that level. When V_{CC} is applied to the bq2004, a charge action begins after a brief power-on reset period. When $\overline{INH}$ transitions from low to high, a charge action begins after a brief reset period.

Temperature and Voltage Prequalification

A charge action is prequalified by the battery temperature and voltage. Before fast charging can begin, the battery temperature and voltage must fall within predetermined acceptable limits.

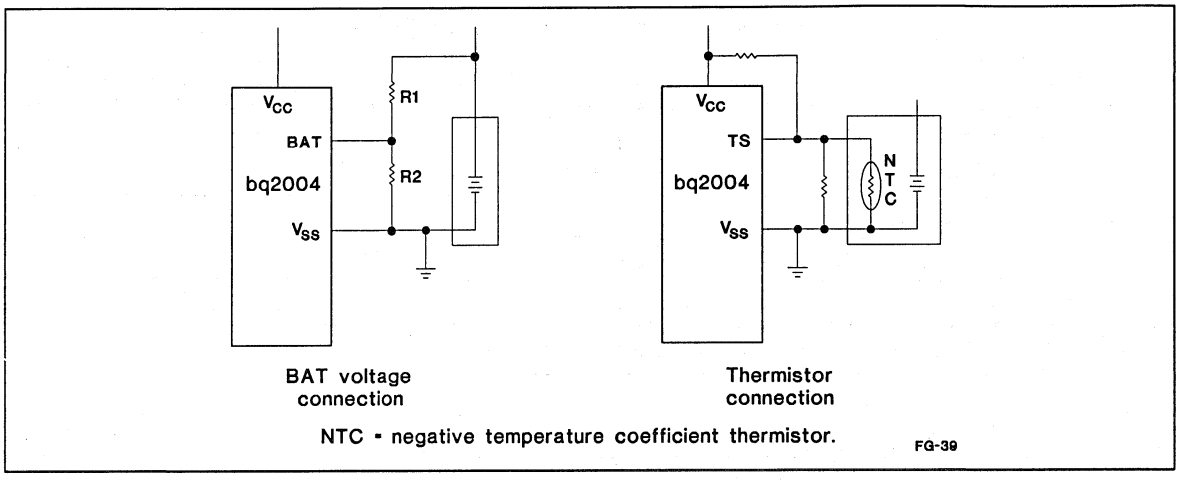


Figure 2. Voltage and Temperature Limit Measurement

V_{CELL} is compared to an internal low-voltage reference, V_{EDV} (0.4 * V_{CC}), which is the minimum acceptable battery voltage for fast charging. The V_{TEMP} (V_{TS} - V_{SNS}) voltage is compared to an internal hot-temperature fault reference, V_{HTF} ((¼ * V_{LTF}) + (¾ * V_{TCO})) and optionally to an internal low-temperature fault reference, V_{LTF} (0.4 * V_{CC}). These limits establish the acceptable battery and temperature sense voltage window for fast charge initiation. If the battery fails either of these two prequalifications for charge, the bq2004 enters a charge-pending mode, waiting for the battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cold, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2004 waits until the battery voltage is at an acceptable level before starting fast charge. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2004 to remain in the charge-pending state. The bq2004 continues to trickle charge (if enabled) the battery until the fast charge conditions are met.

Discharge-Before-Charge

The bq2004 supports discharge-before-charge on the battery, providing conditioning as well as capacity calibration. Once activated, the DIS pin goes active high until V_{CELL} falls below V_{EDV}, at which time fast charge qualification begins.

If $\overline{DCMD}$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with the application of power to the bq2004, by battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. A negative-going pulse on $\overline{DCMD}$ causes the bq2004 to initiate a discharge-before-charge action on the battery regardless of charging activity. The $\overline{DCMD}$ pin is internally pulled up to V_{CC}; therefore, not connecting this pin results in disabling the discharge-before-charge function. See Figure 3.

TM_1 and TM_2 Pins

The TM_1 and TM_2 pins are three-level input pins used to select the various charge, top-off, and trickle rates, maximum safety times, and -ΔV/PVD holdoff period. Table 3 describes the various states selected by the TM_1 and TM_2 pins.

Fast Charge

Once temperature and voltage prequalifications are met and any requested discharging of the battery is completed, fast charging begins and continues until termination by one or more of the five possible termination conditions:

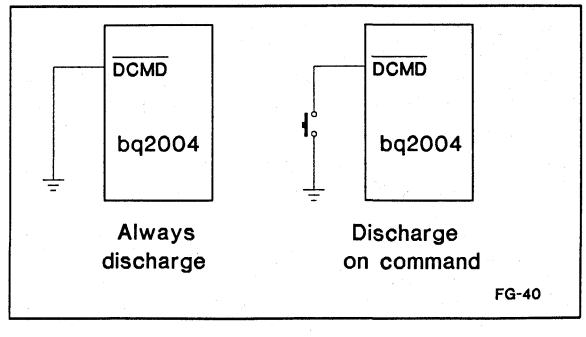


Figure 3. Discharge-Before-Charge

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV) or peak voltage detect (PVD)
- Maximum temperature
- Maximum charge time
- Maximum battery voltage

Voltage Termination Hold-off

At the start of fast charging, there is a hold-off time during which the -ΔV and PVD terminations are disabled (see Table 3). Once past the initial fast charge hold-off time, -ΔV or PVD termination is re-enabled. ΔT/Δt, maximum cell voltage (MCV), and maximum temperature (TCO) terminations are not affected by the hold-off period.

-ΔV or Peak Voltage Detect Termination

The bq2004 has two modes for voltage termination, depending on the state of the VSEL pin. VSEL high enables peak voltage detection; VSEL floating enables -ΔV detection; and VSEL low disables -ΔV and PVD terminations. -ΔV and PVD may be enabled or disabled at any time during the charge cycle. The bq2004 makes a termination decision every 34 seconds. For -ΔV, if V_{CELL} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated. This equates to a -ΔV termination of -6mV per cell typical.

The -ΔV test is valid only for:

$$0.4 * V_{CC} \leq V_{CELL} \leq 0.8 * V_{CC}$$

For peak voltage detect, the fast charge phase of the charge action is terminated when V_{CELL} is lower than the previously measured values by 0 to -3mV per cell.

ΔT/Δt Fast Charge Termination

The bq2004 makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 34 seconds. If V_{TEMP} is 16mV (typical) less than the voltage measured 68 seconds previously, the fast charge phase of the charge is terminated.

The ΔT/Δt test is valid only for:

$$0.2 * V_{CC} \leq V_{TEMP} \leq 0.4 * V_{CC}$$

Maximum Voltage, Time, and Temperature Safety Terminations

The bq2004 also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV). MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during fast charging. If either of these limits is exceeded, then fast charging or optional top-off charge is terminated. MCV is treated as a fault, so LED_1 and LED_2 are switched low with this condition.

Maximum time selection is programmed using the TM_1 and TM_2 pins (see Table 3). Time settings are available for corresponding charge rates ranging from C/4 to 4C.

Table 3. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM_1	TM_2	Fast Charge Safety Time (minutes)	PVD,-ΔV Hold-Off Time (seconds)	Top-Off	Pulse-Trickle Rate	Pulse-Trickle Period (Hz)
			Typical	Typical			
C/4	Low	Low	360	137	N	Disabled	Disabled
C/2	Float	Low	180	820	N	C/32	240
1C	High	Low	90	410	N	C/32	120
2C	Low	Float	45	200	N	C/32	60
4C	Float	Float	23	100	N	C/32	30
C/2	High	Float	180	820	Y	C/64	120
1C	Low	High	90	410	Y	C/64	60
2C	Float	High	45	200	Y	C/64	30
4C	High	High	23	100	Y	C/64	15

Note: T_A = 25°C, V_{CC} = 5.0V.

Temperature Monitoring

Temperature is represented as a voltage input on the bq2004 at the TS pin. Generally this voltage is developed from an NTC (negative temperature coefficient) thermistor referenced to the negative battery terminal. The bq2004 recognizes an internal voltage level of $V_{LTF} = 0.4 * V_{CC}$ as the low-temperature fault (LTF) level. If $V_{TEMP} \geq V_{LTF}$, charging is inhibited or terminated except for the peak voltage detection (VSEL = high) mode. In this mode, LTF is not used to qualify charge or terminate charge.

Similarly, the external reference voltage level presented at the TCO pin represents the high-temperature cut-off point at which fast charging is terminated. V_{TCO} should always be less than V_{LTF} to ensure proper device operation.

All temperature prequalifications and $\Delta T/\Delta t$ termination may be disabled by connecting TCO to V_{SS} and fixing the TS pin level to $0.2 * V_{CC}$. $\Delta T/\Delta t$ termination sensitivity is user-adjustable, depending on the values of the external resistor-divider network.

Top-Off Charge

An optional top-off charge phase is selected to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins (see Table 3). The charge control cycle is modified so that the MOD pin is activated for 260µs of every 2080µs. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to the fast charge safety time. Maximum time, temperature (TCO), and voltage (MCV) terminations are the only termination methods enabled during top-off. If the fast-charge phase of a charge terminates due to TCO, top-off charge pends until the temperature falls below HTF.

Pulse-Trickle Charge

Pulse-trickle charge is used to compensate for self discharge of the battery while idle in the charger, and to bring a depleted battery to a valid charge voltage prior to fast charge. The battery pulse-trickles at the end of fast charge and top-off, and prior to charge (see Table 1).

In the pulse-trickle state, MOD is active for 260µs of a period specified by the state of TM_1 and TM_2 pins. The resulting trickle rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Pulse-trickle and top-off can be disabled by tying TM_1 and TM_2 to V_{SS}.

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2004 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Charge Current Control

The bq2004 controls the charge current through the MOD output pin. The current control is designed to support implementation of a constant-current regulator. See Figure 4. Nominal regulated current is:

$$I_{REG} = 0.225V / R_{SNS}$$

When used in this configuration, the charge current is monitored at the SNS input by the voltage drop across a resistor, R_{SNS}. R_{SNS} may be chosen to provide a variety of charging currents.

The MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.2V typical), the MOD output is switched high to gate charge current. When the SNS voltage is greater than V_{SNSHI} (0.25V typical), the MOD output is switched low—shutting off current from the supply.

The MOD pin can also be used to gate an external charging current source. When an external current source is used, a sense resistor is not required, and the SNS pin is connected to V_{SS}. See Figure 5.

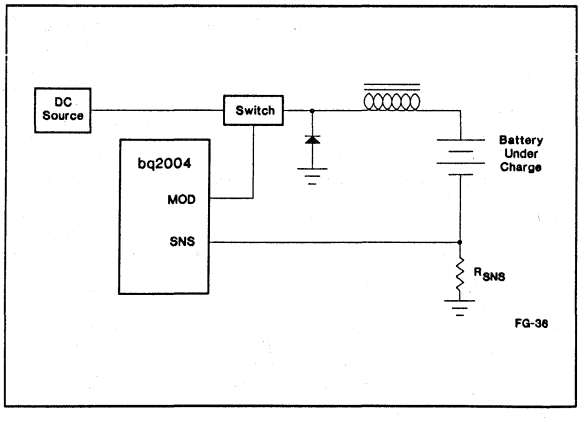


Figure 4. Constant-Current Switching Regulation

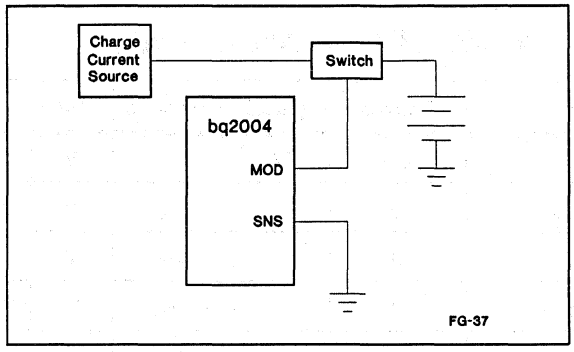


Figure 5. External Current Regulation

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±0.025	V	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	V_{SNSHI} – (0.01 * V_{CC})	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge[1]
V_{HTF}	High-temperature fault	(¼ * V_{LTF}) + (¾ * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.4 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits charge
V_{MCV}	Maximum cell voltage	0.8 * V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge

Note: $V_{CELL} = V_{BAT} - V_{SNS}$. $V_{TEMP} = V_{TS} - V_{SNS}$.

1. VSEL = high disables low-temperature fault charge qualification.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	Valid $\Delta T/\Delta t$ range
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2, DSEL, VSEL
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input low	-	-	0.3	V	TM_1, TM_2, DSEL, VSEL
V_{OH}	Logic output high	V_{CC} - 0.8	-	-	V	DIS, MOD, LED_1, LED_2, $I_{OH} \leq$ -10mA (see Figure 6)
V_{OL}	Logic output low	-	-	0.8	V	DIS, MOD, LED_1, LED_2, $I_{OL} \leq$ 10mA (see Figure 6)
I_{CC}	Supply current	-	1	3	mA	Outputs unloaded
I_{SB}	Standby current	-	-	1	µA	$\overline{INH} = V_{IL}$
I_{OH}	DIS, LED_1, LED_2, MOD source	-10	-	-	mA	@$V_{OH} = V_{CC}$ - 0.8V
I_{OL}	DIS, LED_1, LED_2, MOD sink	10	-	-	mA	@$V_{OL} = V_{SS}$ + 0.8V
I_L	Input leakage	-	-	±1	µA	$\overline{INH}$, BAT, V = V_{SS} to V_{CC}
	Input leakage	50	-	400	µA	$\overline{DCMD}$, V = V_{SS} to V_{CC}
I_{IL}	Logic input low source	-	-	70	µA	TM_1, TM_2, DSEL, VSEL, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, DSEL, VSEL, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	Tri-state	-2	-	2	µA	TM_1, TM_2, DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1	-	-	µs	
d_{FCV}	Fast charge safety time variation	0.84	1.0	1.16	-	V_{CC} = 4.75V to 5.25V; T_A = 0 to 60°C; see Table 3.
t_{REG}	MOD output regulation frequency	-	-	300	kHz	Typical regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	1	-	2	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV} during charge or top-off, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

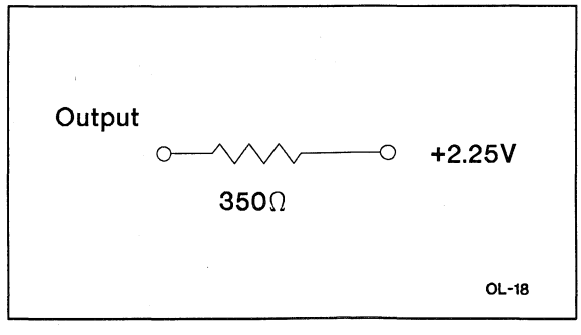
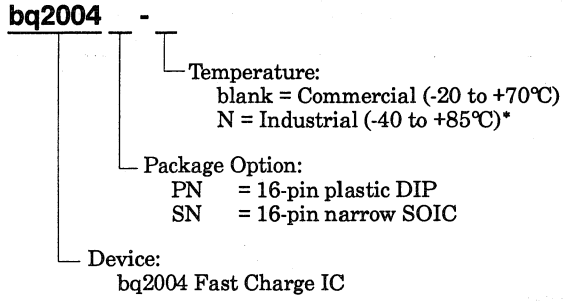


Figure 6. Output Load

Ordering Information



* Contact factory for availability.

BENCHMARQ

Preliminary **bq2004E**

Fast Charge IC

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Supports logic-level-controlled low-power mode (< 1µA standby current)
- Optional peak voltage detect (PVD) fast-charge termination
- Flexible current regulation:
  - Frequency-modulated switching current regulator
  - Gating control for use with external regulator
- 150-mil SOIC is ideal for integration into portable systems
- Pre-charge qualification for temperature and voltage faults
- Programmable LED outputs display battery and charge status
- Fast charge termination by Δ temperature/Δ time, -ΔV or peak voltage, and maximum temperature, time, and voltage

General Description

The bq2004E Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Flexible control of constant-current or current-limited charging supply allows the bq2004E to be the basis of a cost-effective system-integrated charger for batteries of two or more cells. High-efficiency switched constant-current regulation is accomplished using the bq2004E as a frequency-modulated controller. The bq2004E may alternatively be used with a transistor to gate an external charging current or in a cost-effective frequency-modulated linear regulator.

Switch-activated or automatic discharge-before-charge allows bq2004E-based chargers to support battery conditioning and capacity determination.

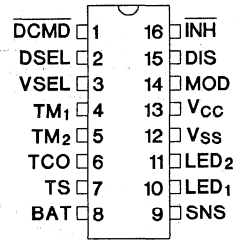
Fast charge may begin on application of V_{CC} to the bq2004E, replacement of the battery, or use of the $\overline{INH}$ pin. For safety, fast charge is inhibited until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV) or peak voltage detect
- Maximum temperature
- Maximum time
- Maximum voltage

Following fast charge, the bq2004E proceeds with a pulsed top-off charge (if enabled) and a pulsed trickle charge.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-47

Pin Names

$\overline{DCMD}$	Discharge command	SNS	Sense resistor input
DSEL	Display select	LED_1	Charge status output 1
VSEL	Voltage termination select	LED_2	Charge status output 2
TM_1	Timer mode select 1	V_{SS}	System ground
TM_2	Timer mode select 2	V_{CC}	5.0V ±10% power
TCO	Temperature cutoff	MOD	Charge current control
TS	Temperature sense	DIS	Discharge control output
BAT	Battery voltage	$\overline{INH}$	Charge inhibit input

Pin Descriptions

$\overline{DCMD}$ **Discharge-before-charge control input**

$\overline{DCMD}$ controls the discharge-before-charge function of the bq2004E. A negative-going pulse on $\overline{DCMD}$ initiates a discharge to EDV (0.4 * V_{CC}) followed by a charge if conditions allow. By tying $\overline{DCMD}$ to ground, automatic discharge-before-charge is enabled by the application of power, by battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. $\overline{DCMD}$ is pulled up internally.

DSEL **Display select input**

This three-level input controls the $LED_{1,2}$ charge status indication. See Table 2 for details.

VSEL **Voltage termination select input**

This three-level input controls the voltage-termination technique used by the bq2004E.

TM_1, TM_2 **Timer mode inputs ($TM_{1,2}$)**

TM_1 and TM_2 are three-level inputs that control the settings for the fast charge safety timer and "top-off"/trickle charge control. See Table 3 for details.

TCO **Temperature cut-off threshold input**

Minimum allowable battery temperature-sensor voltage. If the potential between TS and SNS is less than the voltage at the TCO input, then any fast charging or top-off charging is terminated.

TS **Temperature sense input**

Input for battery temperature monitoring negative temperature coefficient (NTC) thermistor. TS > V_{CC} - 0.5V disables the temperature sensoring.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor network. This provides the reference potentials for both the TS and BAT pins. If SNS is connected to Vss, then MOD switches high at the beginning of charge, and low at the end of charge. See Figure 1 and Table 1 for details.

BAT **Battery voltage input**

BAT is the battery voltage sense input. This potential is limited to between 0.4 * V_{CC} and 0.8 * V_{CC} and is generally developed by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

LED_1, LED_2 **Charge status outputs**

Push-pull outputs indicating charging status. See Figure 1 and Table 2 for details.

Vss **Ground**

V_{CC} **V_{CC} supply input**

5.0V, ±10% power input.

MOD **Charge current control output**

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow. See Figure 1 and Table 1 for details.

DIS **Discharge control output**

Push-pull output used to control an external transistor to discharge the battery before charging. DIS is active high.

$\overline{INH}$ **Charge inhibit input**

When low, the bq2004E suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a charge cycle is initiated. See page 8 for details.

Functional Description

Figure 1 illustrates charge control and display status during a bq2004E charge cycle. Table 1 outlines the various bq2004E operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2004E initiates a charge by the application of power on V_{CC}, by a battery replacement, or by a low-to-high transition on the $\overline{INH}$ pin. Control of the charge action is then determined by the inputs from $\overline{DCMD}$, VSEL, TS, BAT, and $TM_{1,2}$.

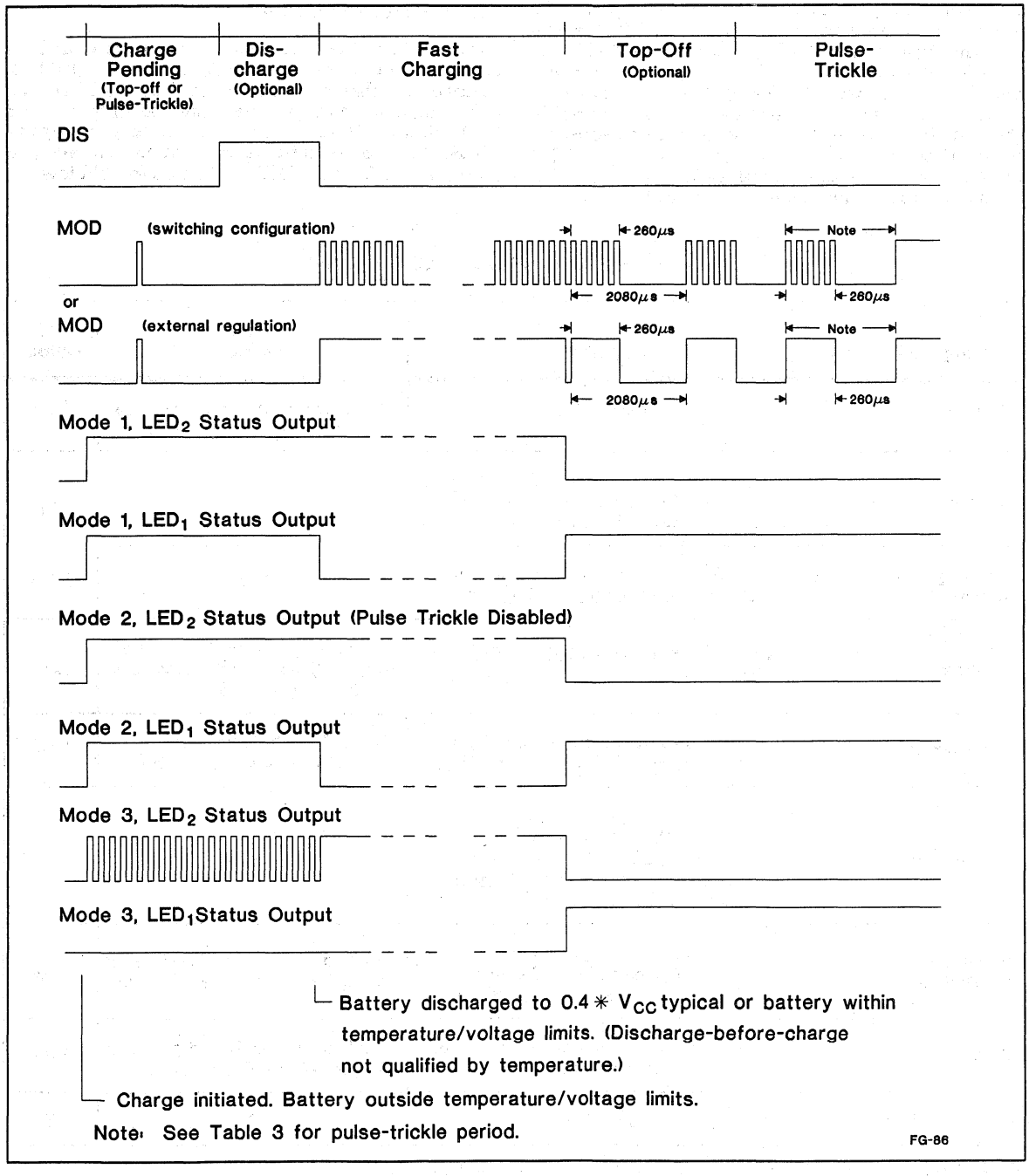


Figure 1. Example Charging Action Events

Following charge initiation, the bq2004E checks for acceptable battery temperature (between LTF—low-temperature fault and HTF—high-temperature fault) and battery voltage (between EDV—end-of-discharge voltage and MCV—maximum cell voltage). Fast charging begins when the voltage and temperature conditions are within these limits. Once the fast charging process begins, the bq2004E tests for the full-charge conditions: $\Delta T/\Delta t$ and/or $-\Delta V$ or peak voltage detect (PVD), with temperature, time, and voltage safety terminations.

Charge Status Indication

Table 1 outlines the various charge action states and the associated MOD and DIS output states. Table 2 describes the charge status indicated by the LED_1 and LED_2 outputs, which may be connected directly to an LED indicator. **In all cases, if the battery voltage at the BAT pin exceeds the maximum cell voltage (0.8 * V_{CC}), the LED_1 and LED_2 outputs are held low.**

Table 1. bq2004E Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output
Battery absent	$V_{CELL} \geq V_{MCV}$	Trickle charge activated per V_{SNS} for period specified in Table 3*	Low
Charge initiation	V_{CC} applied, V_{CELL} drops from $\geq V_{MCV}$ to $< V_{MCV}$ (battery insertion), or $\overline{INH}$ transitions low to high with battery inserted	-	–
Discharge-before-charge (optional)	$\overline{DCMD}$ high-to-low pulse or tied to V_{SS} on charge initiation; $V_{EDV} < V_{CELL} < V_{MCV}$	Low	High
Pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{HTF}$ or $V_{CELL} < V_{EDV}$	Activated per V_{SNS} for 260µs of every 2080 for top-off period; then trickle (see trickle state)	Low
Fast charging	Charge initiation occurred and $V_{HTF} < V_{TEMP} < V_{LTF}$ and $V_{EDV} \leq V_{CELL} < V_{MCV}$	Low if $V_{SNS} > 250mV$, nominal; high if $V_{SNS} < 200mV$, nominal	Low
Charge complete	$-\Delta V \geq 6mV$/cell or PVD ≥ 0 to 3mV/cell or $\Delta V_{TEMP}/\Delta T > 14mV$/minute or $V_{TEMP} < V_{TCO}$ or $V_{TEMP} > V_{LTF}$ or maximum time or maximum voltage	–	–
Top-off (optional; see Table 3)	Charge complete and top-off time not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} (see fast charging state) for 260µs of every 2080µs	Low
Trickle	Charge complete and top-off disabled or top-off complete	Trickle charge activated per V_{SNS} for period specified in Table 3 *	Low
Charge inhibit	$\overline{INH}$ low	Z	Z

Definitions: $V_{CELL} = V_{BAT} - V_{SNS}$; $V_{MCV} = 0.8 * V_{CC}$; $V_{EDV} = 0.4 * V_{CC}$;
$V_{TEMP} = V_{TS} - V_{SNS}$; $V_{LTF} = 0.4 * V_{CC}$; $V_{HTF} = ((1/3 * V_{LTF}) + (2/3 * V_{TCO}))$.
*DSEL = Z disables trickle.

Table 2. bq2004E LED Output Summary

Mode 1	Charge Action State	LED_1	LED_2
DSEL = Vss	Battery absent	Low	Low
	Fast charge pending or a discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 2	**Charge Action State (See note)**	**LED_1**	**LED_2**
DSEL = Floating	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 3	**Charge Action State**	**LED_1**	**LED_2**
DSEL = Vcc	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	Low	1/8 second high 1/8 second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

Note: Pulse trickle is inhibited in Mode 2.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum and minimum allowable values. The battery voltage sense input, BAT, for a battery pack should be divided to between 0.8 * Vcc and 0.4 * Vcc for proper operation. A resistor-divider ratio of:

$$\frac{R1}{R2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the respective SNS pin. See Figure 2.

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2004E.

The thermistor used for temperature measurement should have a negative temperature coefficient. The temperature sense voltage input at TS is developed using a resistor-thermistor network between Vcc and SNS. See Figure 2.

Battery Removal Detection

Battery removal is sensed by V_{CELL} (V_{BAT} - V_{SNS}) rising above V_{MCV} (0.8 * Vcc). An external resistor, R_{EXT}, between the battery positive lead and the charging supply input pulls V_{CELL} above V_{MCV} to detect battery removal.

Initiating a Charge Action

A battery charge action is initiated with a battery insertion, an application of Vcc to the bq2004E, or a low-to-high transition on the $\overline{INH}$ pin. Battery insertion is recognized when the voltage at the BAT pin falls from above the internal V_{MCV} reference level to below that level. When Vcc is applied to the bq2004E or $\overline{INH}$ transitions from low to high, a charge action begins after a brief power-on reset period.

Temperature and Voltage Prequalification

A charge action is prequalified by the battery temperature and voltage. Before fast charging can begin, the battery temperature and voltage must fall within predetermined acceptable limits.

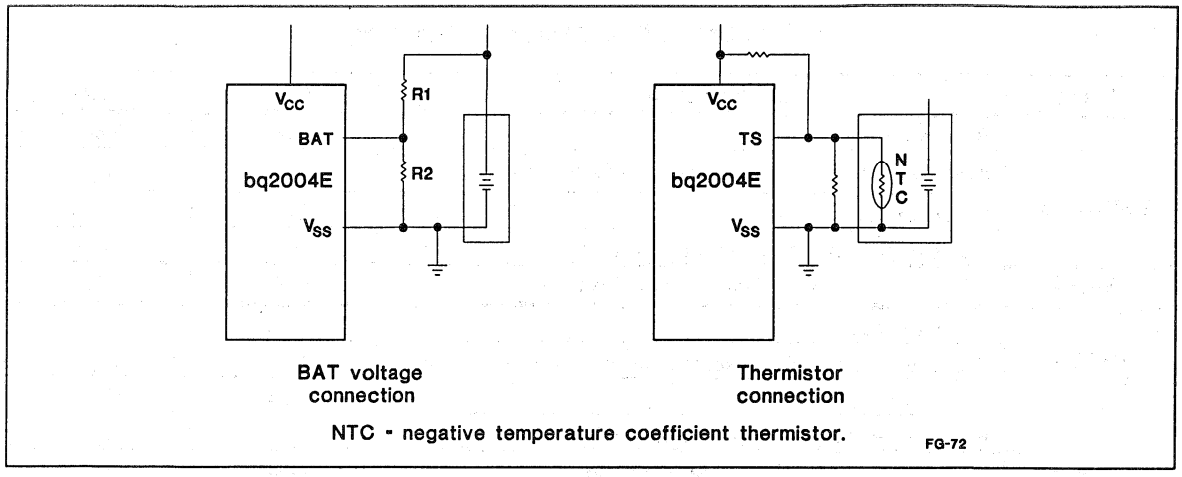


Figure 2. Voltage and Temperature Limit Measurement

V_{CELL} is compared to an internal low-voltage reference, V_{EDV} (0.4 * V_{CC}), which is the minimum acceptable battery voltage for fast charging. The V_{TEMP} (V_{TS} - V_{SNS}) voltage is compared to an internal hot-temperature fault reference, V_{HTF} ((⅓ * V_{LTF}) + (⅔ * V_{TCO})) and optionally to an internal low-temperature fault reference, V_{LTF} (0.4 * V_{CC}). These limits establish the acceptable battery and temperature sense voltage window for fast charge initiation. If the battery fails either of these two prequalifications for charge, the bq2004E enters a charge-pending mode, waiting for the battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cold, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2004E waits until the battery voltage is at an acceptable level before starting fast charge. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2004E to remain in the charge-pending state.

During the charge-pending mode, the bq2004E continues to pulse at ⅛ of the fast charge rate until the fast charge conditions are met or the top-off time-out period is exceeded. The bq2004E then trickle charges until the fast charge conditions are met.

Discharge-Before-Charge

The bq2004E supports discharge-before-charge on the battery, providing conditioning as well as capacity calibration. Once activated, the DIS pin goes active high until V_{CELL} falls below V_{EDV}, at which time fast charge qualification begins.

If $\overline{DCMD}$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with the application of power to the bq2004E or by battery replacement. A negative-going pulse on $\overline{DCMD}$ causes the bq2004E to initiate a discharge-before-charge action on the battery regardless of charging activity. The $\overline{DCMD}$ pin is internally pulled up to V_{CC}; therefore, not connecting this pin results in disabling the discharge-before-charge function. See Figure 3.

TM_1 and TM_2 Pins

The TM_1 and TM_2 pins are three-level input pins used to select the various charge, top-off, and trickle rates, maximum safety times, and -ΔV/PVD holdoff period. Table 3 describes the various states selected by the TM_1 and TM_2 pins.

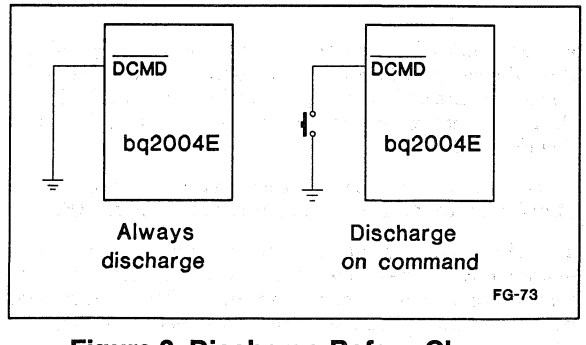


Figure 3. Discharge-Before-Charge

Fast Charge

Once temperature and voltage prequalifications are met and any requested discharging of the battery is completed, fast charging begins and continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV) or peak voltage detect (PVD)
- Maximum temperature
- Maximum charge time
- Maximum battery voltage

Voltage Termination Hold-off

At the start of fast charging, there is a hold-off time during which the -ΔV, PVD, and ΔT/Δt terminations are disabled (see Table 3). During hold-off, MOD is active for ⅛th of the charge rate. Once past the initial fast charge hold-off time, -ΔV, PVD, and ΔT/Δt terminations are re-enabled and MOD is active for fast charging per Table 1. Maximum cell voltage (MCV), and maximum temperature (TCO) terminations are not affected by the hold-off period. The hold-off time is not included in the Fast Charge Safety Time.

-ΔV or Peak Voltage Detect Termination

The bq2004E has two modes for voltage termination, depending on the state of the VSEL pin. VSEL high enables peak voltage detection; VSEL floating enables -ΔV detection; and VSEL low disables -ΔV and PVD terminations. -ΔV and PVD may be enabled or disabled at any time during the charge cycle. The bq2004E makes a termination decision every 17 seconds. For -ΔV, if V_{CELL} is lower than any previously measured value by 12mV typical, the fast charge phase of the charge action is terminated. This equates to a -ΔV termination of -6mV per cell typical.

The -ΔV test is valid only for:

$$0.4 * V_{CC} \le V_{CELL} \le 0.8 * V_{CC}$$

For peak voltage detect, the fast charge phase of the charge action is terminated when V_{CELL} is lower than the previously measured values by 0 to -3mV per cell.

ΔT/Δt Fast Charge Termination

The bq2004E makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 34 seconds. If V_{TEMP} is 16mV (typical) less than the voltage measured 68 seconds previously, the fast charge phase of the charge is terminated.

The ΔT/Δt test is valid only for:

$$0.2 * V_{CC} \le V_{TEMP} \le 0.4 * V_{CC}$$

Maximum Voltage, Time, and Temperature Safety Terminations

The bq2004E also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV). MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during fast charging. If either of these limits is exceeded, then fast charging or optional top-off charge is

Table 3. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM_1	TM_2	Fast Charge Safety Time (minutes)	PVD, -ΔV, and ΔT/Δt Hold-Off Time (seconds)	Top-Off	Pulse-Trickle Rate*	Pulse-Trickle Period (Hz)
			Typical	Typical			
C/4	Low	Low	325	137	N	Disabled	Disabled
C/2	Float	Low	154	546	N	C/512	15
1C	High	Low	77	273	N	C/512	7.5
2C	Low	Float	39	137	N	C/512	3.75
4C	Float	Float	19	68	N	C/512	1.88
C/2	High	Float	154	546	Y	C/512	15
1C	Low	High	77	273	Y	C/512	7.5
2C	Float	High	39	137	Y	C/512	3.75
4C	High	High	19	68	Y	C/512	1.88

Note: T_A = 25°C, V_{CC} = 5.0V.
*DSEL = Z disables pulse trickle

terminated. MCV is treated as a fault, so LED_1 and LED_2 are switched low with this condition.

Maximum time selection is programmed using the TM_1 and TM_2 pins (see Table 3). Time settings are available for corresponding charge rates ranging from C/4 to 4C.

Temperature Monitoring

Temperature is represented as a voltage input on the bq2004E at the TS pin. Generally this voltage is developed from an NTC (negative temperature coefficient) thermistor referenced to the negative battery terminal. The bq2004E recognizes an internal voltage level of V_{LTF} = 0.4 * V_{CC} as the low-temperature fault (LTF) level. If $V_{TEMP} \geq V_{LTF}$, charging is inhibited or terminated.

Similarly, the external reference voltage level presented at the TCO pin represents the high-temperature cut-off point at which fast charging is terminated. V_{TCO} should always be less than V_{LTF} to ensure proper device operation.

All temperature prequalifications and $\Delta T/\Delta t$ termination may be disabled by connecting TCO to V_{SS} and tying the TS pin to V_{CC}. $\Delta T/\Delta t$ termination sensitivity is user-adjustable, depending on the values of the external resistor-divider network.

Top-Off Charge

An optional top-off charge phase is selected to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins (see Table 3). The charge control cycle is modified so that the MOD pin is activated for 260µs of every 2080µs. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to 4/17 of the fast charge safety time (0.235 * safety time). Maximum time, temperature (TCO), and voltage (MCV) terminations are the only termination methods enabled during top-off. If the fast-charge phase of a charge terminates due to TCO, top-off charge pends until the temperature falls below high temperature fault (HTF).

Pulse-Trickle Charge

Pulse-trickle charge is used to compensate for self-discharge of the battery while idle in the charger. The battery pulse-trickles at the end of fast charge and top-off (see Table 1).

In the pulse-trickle state, MOD is active for 260µs of a period specified by the state of TM_1 and TM_2 pins. The resulting trickle rate is C/512. Pulse-trickle and top-off can be disabled by tying TM_1 and TM_2 to V_{SS}. Pulse trickle can also be disabled when DSEL = Z.

For pre-charge qualification, MOD is active for 260µs of every 2080µs, resulting in a rate 1/8th that of the fast charge rate. MOD continues to pulse at a 1/8 the rate for the top-off time-out period and then pulse trickles until the fast charge conditions are met. This is useful for bringing up the voltage on a battery after long storage periods.

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2004E suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Charge Current Control

The bq2004E controls the charge current through the MOD output pin. The current control is designed to support implementation of a constant-current regulator. See Figure 4. Nominal regulated current is:

$$I_{REG} = 0.225V / R_{SNS}$$

When used in this configuration, the charge current is monitored at the SNS input by the voltage drop across a resistor, R_{SNS}. R_{SNS} may be chosen to provide a variety of charging currents.

The MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.2V typical), the MOD output is switched high to gate charge current. When the SNS voltage is greater than V_{SNSHI} (0.25V typical), the MOD output is switched low—shutting off current from the supply.

The MOD pin can also be used to gate an external charging current source. When an external current source is used, a sense resistor is not required, and the SNS pin is connected to V_{SS}. See Figure 5.

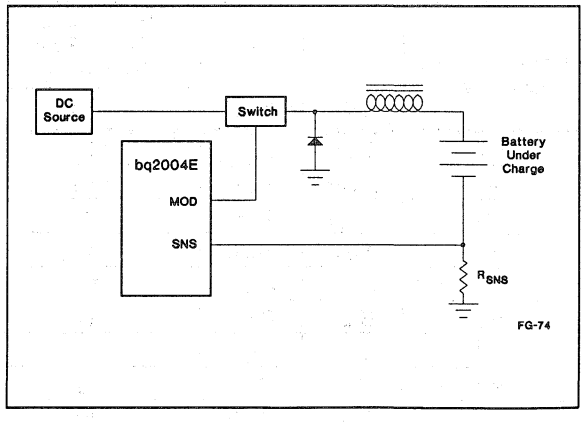


Figure 4. Constant-Current Switching Regulation

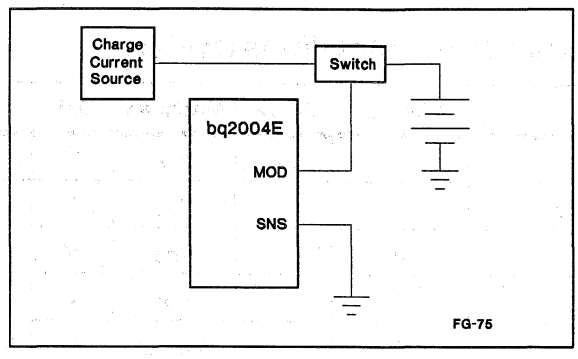


Figure 5. External Current Regulation

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±0.025	V	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	V_{SNSHI} – (0.01 * V_{CC})	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	(⅓ * V_{LTF}) + (⅔ * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.4 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits charge
V_{MCV}	Maximum cell voltage	0.8 * V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge

Note: $V_{CELL} = V_{BAT} - V_{SNS}$. $V_{TEMP} = V_{TS} - V_{SNS}$.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	$V_{BAT} - V_{SNS}$
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	$V_{TS} - V_{SNS}$
V_{TS}	Thermistor input	0	-	V_{CC} - 1.5	V	Valid temperature sensing
		V_{CC} - 0.5	-	V_{CC}		Disable temperature sensing
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	Valid $\Delta T/\Delta t$ range
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2, DSEL, VSEL
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input low	-	-	0.3	V	TM_1, TM_2, DSEL, VSEL
V_{OH}	Logic output high	V_{CC} - 0.8	-	-	V	DIS, MOD, LED_1, LED_2, $I_{OH} \leq$ -10mA (see Figure 6)
V_{OL}	Logic output low	-	-	0.8	V	DIS, MOD, LED_1, LED_2, $I_{OL} \leq$ 10mA (see Figure 6)
I_{CC}	Supply current	-	1	3	mA	Outputs unloaded
I_{SB}	Standby current	-	-	1	µA	$\overline{INH} = V_{IL}$
I_{OH}	DIS, $\overline{LED_1}$, $\overline{LED_2}$, $\overline{MOD}$ source	-10	-	-	mA	@$V_{OH} = V_{CC}$ - 0.8V
I_{OL}	DIS, LED_1, LED_2, MOD sink	10	-	-	mA	@$V_{OL} = V_{SS}$ + 0.8V
I_L	Input leakage	-	-	±1	µA	$\overline{INH}$, BAT, V = V_{SS} to V_{CC}
	Input leakage	50	-	400	µA	$\overline{DCMD}$, V = V_{SS} to V_{CC}
I_{IL}	Logic input low source	-	-	70	µA	TM_1, TM_2, DSEL, VSEL, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, DSEL, VSEL, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	Tri-state	-2	-	2	µA	TM_1, TM_2, DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ

2

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1	-	-	µs	
d_{FCV}	Fast charge safety time variation	0.84	1.0	1.16	-	V_{CC} = 4.75V to 5.25V; T_A = 0 to 60°C; see Table 3.
t_{REG}	MOD output regulation frequency	-	-	300	kHz	Typical regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	1	-	2	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV} during charge or top-off, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

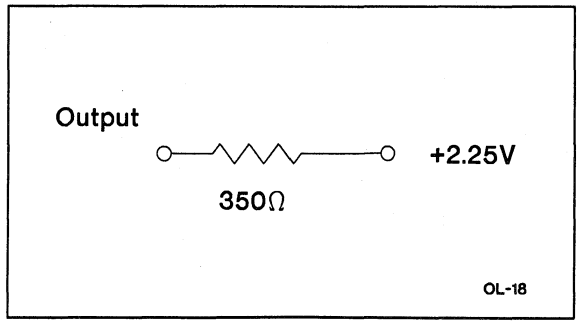
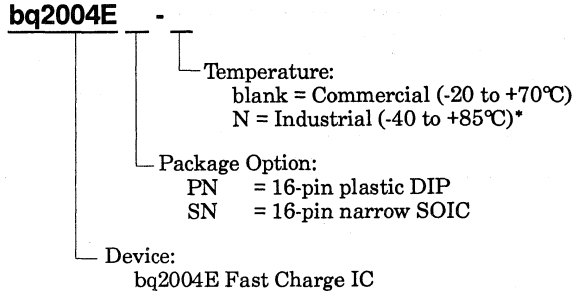


Figure 6. Output Load

Ordering Information



* Contact factory for availability.

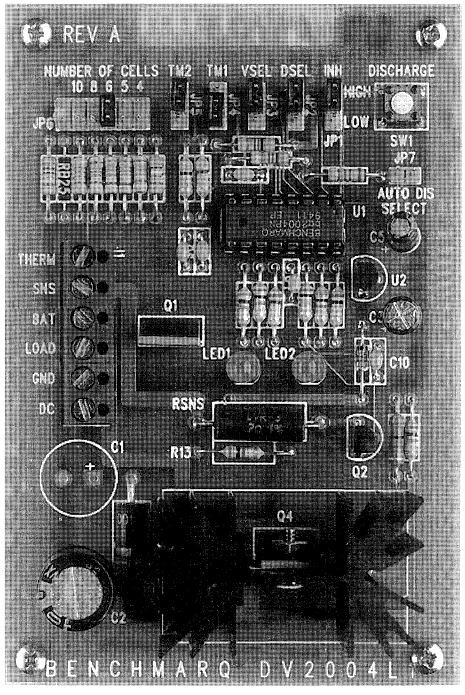
DV2004L1

Fast Charge Development System

Control of PNP Power Transistor

Features

- bq2004 fast charge control evaluation and development
- Charge current sourced from an on-board frequency-modulated linear regulator (up to 3.0 A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast charge termination by delta temperature/delta time (ΔT/Δt), negative delta voltage (-ΔV) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input



General Description

The DV2004L1 Development System provides a development environment for the bq2004 Fast Charge IC. The DV2004L1 incorporates a bq2004 and a frequency-modulated linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

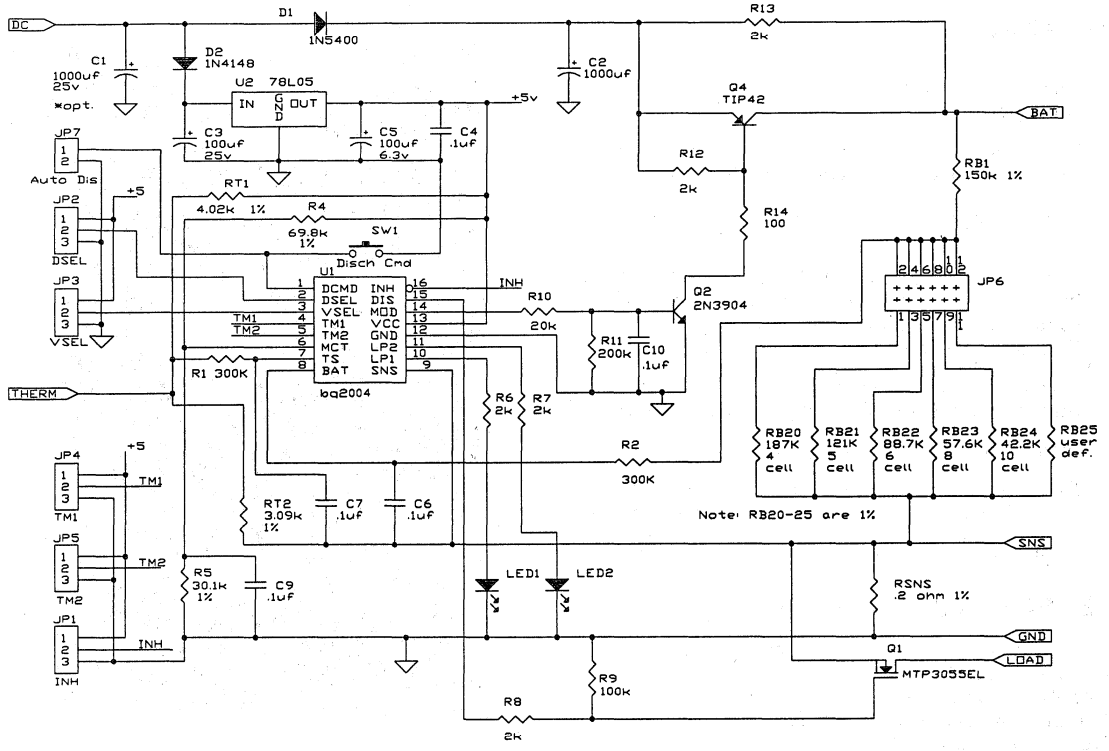
The fast charge is terminated by any of the following: ΔT/Δt, -ΔV or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004L1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.

Contents

1	DV2004L1 printed circuit board containing: a) bq2004 PDIP IC b) Frequency-modulated current regulator with heat sink c) All programming jumpers d) NTC thermistor
1	bq Charge Configuration diskette
1	Documentation kit including user's guide, schematics, and data sheets

DV2004L1 Board Schematic



Thermistor values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

BD-223

BENCHMARQ

DV2004L3

Fast Charge Development System

Control of Frequency-Modulated Linear Regulator

Features

- ➤ bq2004 fast charge control evaluation and development
- ➤ Charge current controlled with frequency-modulated linear design
- ➤ Fast charge of 2 to 12 NiCd and/or NiMH cells
- ➤ Fast charge termination by -ΔV, PVD, ΔT/Δt, maximum temperature, time, and voltage
- ➤ Discharge-before-charge option

General Description

The bq2004L3 Development System provides a cost-effective component-reduced development environment for the bq2004 Fast Charge IC. The DV2004L3 incorporates a frequency-modulated linear regulator for fast charge control of NiCd and/or NiMH cells.

The bq2004 MOD output drives a transistor that switches the bipolar transistor Q2. The switching frequency of the MOD output depands on the voltage of the SNS pin. The bq2004 switches MOD to maintain a nominal 0.220V across resistor R10. The charge current can easily be adjusted by modifying the value of R10.

Fast charge is terminated by any of the following: -ΔV or peak voltage detect (PVD), ΔT/Δt, maximum time, and maximum voltage. Jumper settings select the -ΔV enabled state, select the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries and completes the configuration sheet below.

Contents

1	DV2004L3 Development Board (includes 6W heat sink)
1	bq Charge Configuration Diskette
1	Documentation kit including user's guide, schematics, and data sheets

DV2004L3 Configuration—Complete Before Ordering

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

DC input voltage (V) _____

PVD enabled (yes/no) _____

-ΔV enabled (yes/no) _____

ΔT/Δt enabled (yes/no and desired rate) _____

Number of battery cells (2—12) _____

Charge current (A) (1.5A max.) _____

Battery capacity (mAh) _____

Battery type (NiCd and/or NiMH) _____

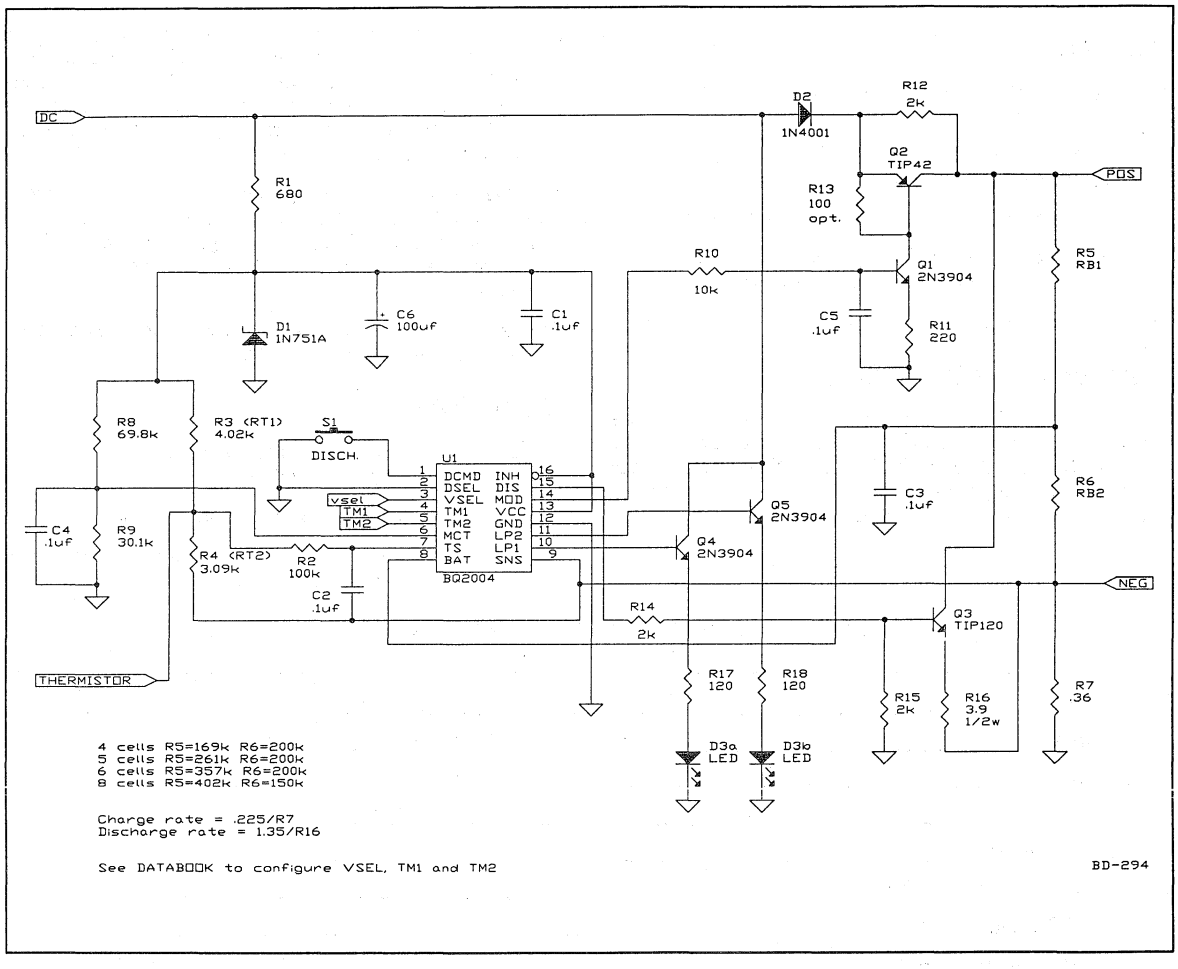
Top-off (yes/no) _____

Discharge-before-charge (yes/no) _____

Discharge current (mA) _____

Dec. 1994

DV2004L3 Board Schematic



BENCHMARQ

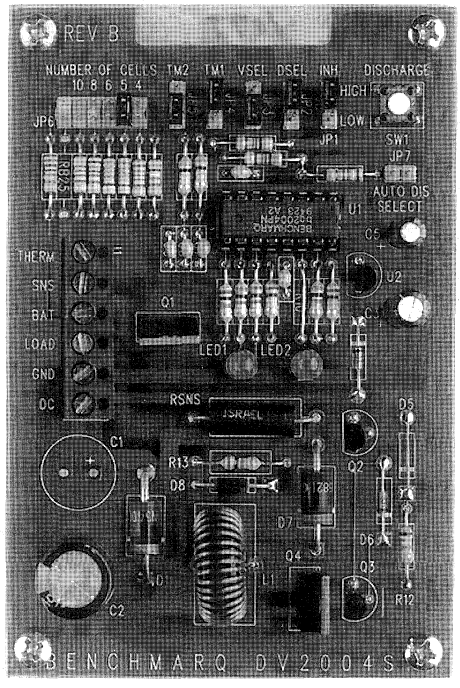
DV2004S1

Fast Charge Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2004 fast charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input



General Description

The DV2004S1 Development System provides a development environment for the bq2004 Fast Charge IC. The DV2004S1 incorporates a bq2004 and a buck-type switch-mode regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

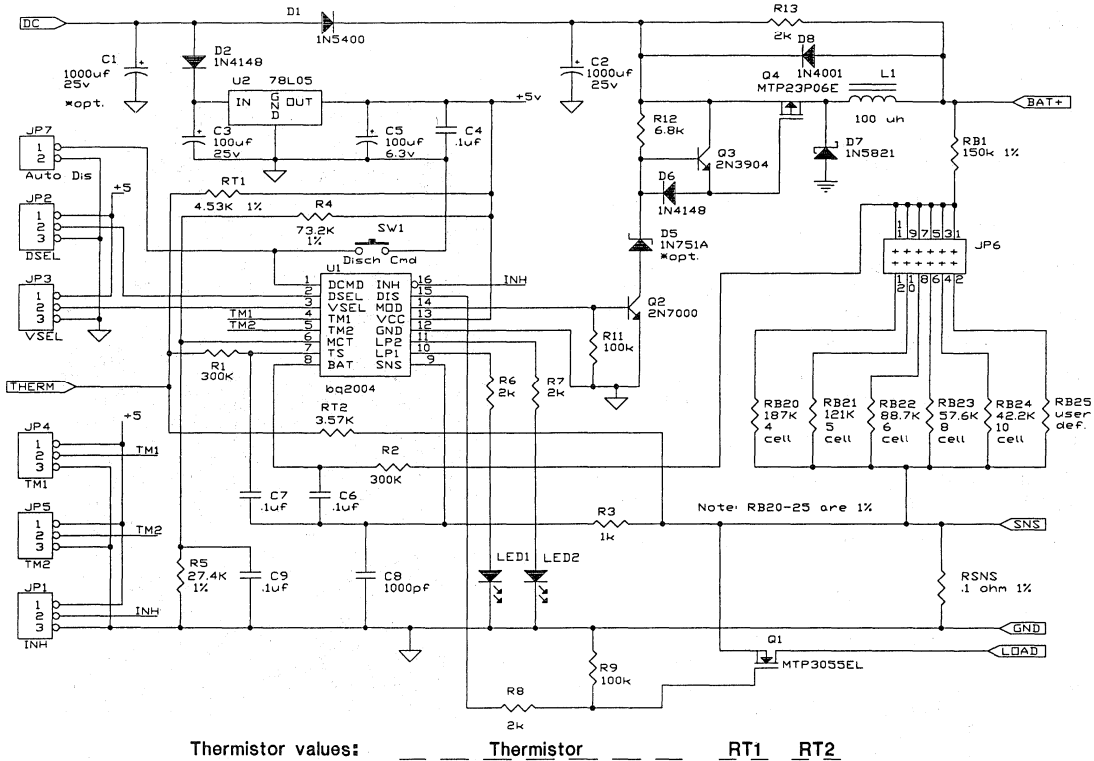
The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004S1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.

Contents

1	DV2004S1 printed circuit board containing: a) bq2004 PDIP IC b) Switch-mode current regulator c) All programming jumpers d) NTC thermistor
1	bq Charge Configuration diskette
1	Documentation kit including user's guide, schematics, and data sheets

DV2004S1 Board Schematic



Thermistor values:

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Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

BD-277

BENCHMARQ

bq2005

Dual-Battery Fast Charge IC

Features

- Fast charge control and conditioning for one or two NiMH or NiCd batteries
- Flexible current regulation:
  - Integrated switching charge current controller
  - Gating control for use with external regulation
- Sequential charging of two battery packs
- Discharge-before-charge for battery conditioning
- Fast charge termination by: $\Delta T/\Delta t$, $-\Delta V$, maximum time, maximum temperature, maximum voltage
- Selectable pulsed "top-off" and trickle charge
- Direct LED control outputs display battery and charge status
- 20-pin 300-mil PDIP or SOIC packages

General Description

The CMOS bq2005 Dual-Battery Fast Charge IC provides comprehensive fast charge control functions with high-speed switching power control circuitry for one or two independent battery-pack systems.

The bq2005 is the basis of a cost-effective solution for sequentially charging two battery packs using flexible control of constant-current or current-limited charging supply. The bq2005 can be used as a frequency-modulated controller operating up to 300KHz for switched regulation of the charging current. The bq2005 may alternatively be used with a linear regulator or transistor to gate an external supply.

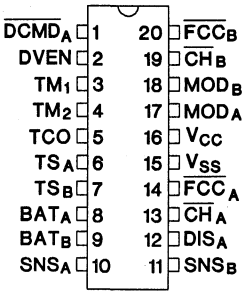
Switch-activated or automatic discharge-before-charge for one battery allows bq2005-based chargers to support battery conditioning, eliminating the voltage-depression effect found in some rechargeable battery chemistries.

Fast charge begins with the application of the charging supply or by replacement of the battery. For safety, charge is inhibited until the battery temperature and voltage are within configured limits. Temperature, voltage, and time are monitored throughout fast charge.

Charge is terminated by any of the following:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Negative delta voltage ($-\Delta V$)
- Maximum temperature
- Maximum time
- Maximum voltage

Pin Connections



20-Pin DIP or SOIC

PN-44

Pin Names

$\overline{DCMD}_A$	Discharge command input, battery A
DVEN	$-\Delta V$ enable
TM_1	Timer mode select 1
TM_2	Timer mode select 2
TCO	Temperature cut-off
TS_A, TS_B	Temperature sense input, battery A/B
BAT_A, BAT_B	Battery voltage input, battery A/B
DIS_A	Discharge control output, battery A
$\overline{CH}_A$, $\overline{CH}_B$	Charge status output, battery A/B
$\overline{FCC}_A$, $\overline{FCC}_B$	Fast charge complete output, battery A/B
V_{SS}	System ground
V_{CC}	5.0V ±10% power
MOD_A, MOD_B	Charge current control output, battery A/B
SNS_A, SNS_B	Charging current sense input, battery A/B

Pin Descriptions

$\overline{DCMD}_A$ Discharge-before-charge control input, battery A

$\overline{DCMD}_A$ controls the discharge-before-charge function of the bq2005. A negative-going pulse on $\overline{DCMD}_A$ initiates a discharge to EDV (0.475 * V_{CC}) followed by a charge if conditions allow. By tying $\overline{DCMD}_A$ to ground, automatic discharge-before-charge is enable either by the application of power or by battery replaced.

DVEN -ΔV enable input

This input controls the -ΔV charge termination test. If DVEN is high, the -ΔV termination method is enabled. If DVEN is low, -ΔV is disabled. DVEN may change state at any time.

TM_1, TM_2 Timer mode inputs ($TM_{1,2}$)

TM_1 and TM_2 are three-level inputs that control the settings for fast charge safety timer and "top-off"/trickle charge control. See Table 3 for details.

TCO Temperature cut-off threshold input

Maximum allowable battery temperature-sensor voltage. If the potential between TS_A and SNS_A or TS_B and SNS_B is less than the voltage at the TCO input, then any fast charging or "top off" charging is terminated for the respective battery.

TS_A, TS_B Temperature sense inputs, battery A/B ($TS_{A,B}$)[1]

Input for external battery temperature monitoring thermistor.

SNS_A, SNS_B Charging current sense inputs, battery A/B ($SNS_{A,B}$)[1]

$SNS_{A,B}$ controls the switching of $MOD_{A,B}$ based on an external sense resistor network. This provides the reference potentials for both the $TS_{A,B}$ and $BAT_{A,B}$ pins. If $SNS_{A,B}$ is connected to V_{SS}, then $MOD_{A,B}$ switches high at the beginning of charge, and low at the end of charge. See Figure 1 and Table 1 for details.

BAT_A, BAT_B Battery voltage inputs, battery A/B ($BAT_{A,B}$)[1]

BAT_A and BAT_B are the divided input voltages for battery A and battery B. This potential is limited to 0.95 * V_{CC} and 0.475 * V_{CC} and is generally developed by a high impedance resistor-divider network connected between the positive and the negative terminals of the battery.

DIS_A Discharge control output

Push-pull output used to control an external transistor to discharge battery A before charging. DIS_A is active high.

$\overline{CH}_A$, $\overline{CH}_B$ Charge status outputs, battery A/B ($\overline{CH}_{A,B}$)[1]

Open-drain output indicating charging status. See Figure 1 and Table 2 for details.

$\overline{FCC}_A$, $\overline{FCC}_B$ Fast charge complete outputs, battery A/B ($\overline{FCC}_{A,B}$)[1]

Open-drain output indicating fast charge complete. See Figure 1 and Table 2 for details.

MOD_A, MOD_B Charge current control outputs, battery A/B ($MOD_{A,B}$)[1]

$MOD_{A,B}$ is a push-pull output that is used to control the charging current to the battery. $MOD_{A,B}$ switches high to enable charging current to flow and low to inhibit charging current flow. See Figure 1 and Table 1 for details.

V_{CC} V_{CC} supply input

5.0V, ±10% power input.

V_{SS} Ground

[1] Notation used in text for generic pin reference.

Functional Description

Figure 1 illustrates charge control and display status during a bq2005 charge cycle. Table 1 outlines the various bq2005 operational states and their associated conditions, which are described in detail in the following sections.

Charge Action Control

The bq2005 initiates a charge by either the application of power on V_{CC} or by a battery replacement. A charge action is controlled by the inputs from $\overline{DCMD}_A$, DVEN, $TS_{A,B}$, $BAT_{A,B}$, and $TM_{1,2}$.

The bq2005 is a sequential charger, initiating a charge action on either battery A or B. If both battery A and battery B are present when V_{CC} is applied to the bq2005, the charge action begins with battery B if conditions are acceptable. The bq2005 controls the initiation of a charge action and checks for acceptable battery temperature (between LTF—low-temperature fault and HTF—high-temperature fault) and voltage (between EDV—end-of-discharge voltage and MCV—maximum cell voltage) prior to fast charging. The fast charging process begins, and the bq2005 tests for the full-charge conditions: $\Delta T/\Delta t$ and/or $-\Delta V$, with temperature, time, and voltage safety terminations.

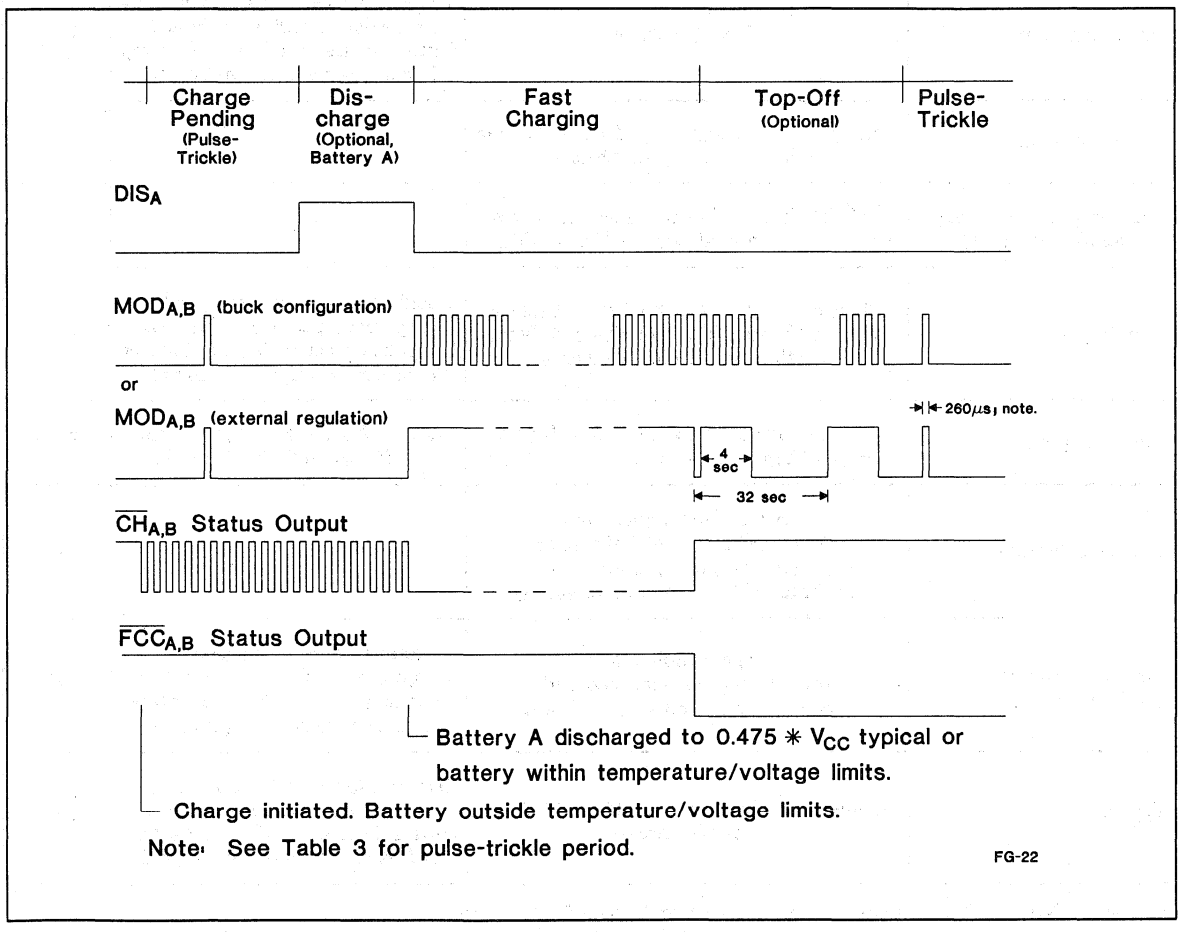


Figure 1. Example Charging Action Events

Charge Status Indication

Table 1 outlines the various charge action states and the associated $MOD_{A,B}$ and DIS_A output states. Table 2 describes the charge status indicated by the $\overline{CH}_{A,B}$ and $\overline{FCC}_{A,B}$ outputs, which may be connected directly to an LED indicator. **In all cases, if the battery voltage at the BAT_A and/or BAT_B pins exceeds the maximum cell voltage (0.95 * V_{CC}), the $\overline{CH}_{A,B}$ and $\overline{FCC}_{A,B}$ outputs are held high.**

Table 1. bq2005 Operational Summary

Charge Action State	Conditions	$MOD_{A,B}$ Output	DIS_A Output
Battery absent	$V_{CELL} \geq V_{MCV}$	Trickle charge activated per V_{SNS} for period specified in Table 3. Output is inactive if other battery is fast charging or topping off.	Low
Charge initiation	V_{CC} applied or V_{CELL} drops from $\geq V_{MCV}$ to $< V_{MCV}$ (battery insertion)	–	–
Discharge-before-charge (optional, battery A)	$\overline{DCMD}_A$ high-to-low pulse or tied to V_{SS} when V_{CC} is applied; $V_{EDV} < V_{CELL} < V_{MCV}$	MOD_A low	High
Pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{HTF}$ or $V_{CELL} < V_{EDV}$, or other battery fast charging	Trickle charge activated per V_{SNS} for period specified in Table 3. Output is inactive if other battery is fast charging or topping off.	Low
Fast charging	Charge initiation occurred and $V_{HTF} < V_{TEMP} < V_{LTF}$ and $V_{EDV} \leq V_{CELL} < V_{MCV}$	Low if $V_{SNS} > 250mV$, nominal; high if $V_{SNS} < 200mV$, nominal	Low
Charge complete	$-\Delta V \geq 13mV$ typical or $\Delta V_{TEMP}/\Delta T > 14mV$/minute or $V_{TEMP} < V_{TCO}$ or $V_{TEMP} > V_{LTF}$ or maximum time or maximum voltage	–	–
Top-off (optional; see Table 3)	Charge complete and top-off time not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} (see fast charging state) for 4 of every 32 sec. Output is inactive if other battery is fast charging or topping off.	Low
Trickle	Charge complete and top-off disabled or top-off complete	Trickle charge activated per V_{SNS} for period specified in Table 3. Output is inactive if other battery is fast charging or topping off.	Low

Notes: $V_{CELL} = V_{BAT} - V_{SNS}$, $V_{MCV} = 0.95 * V_{CC}$, $V_{EDV} = 0.475 * V_{CC}$.
$V_{TEMP} = V_{TS} - V_{SNS}$, $V_{LTF} = 0.4 * V_{CC}$, $V_{HTF} = ((1/4 * V_{LTF}) + (3/4 * V_{TCO}))$.

Table 2. bq2005 LED Output Summary

Charge Action State	Note	$\overline{CH}_A$, $\overline{CH}_B$	$\overline{FCC}_A$, $\overline{FCC}_B$
Battery absent	Battery not inserted	High	High
Charge initiated and pending or battery A discharge-before-charge	Fast charge conditions are not valid, or other battery is fast charging	1/8 sec high, 1/8 sec low	High
Fast charging	-	Low	High
Charge complete, top-off, and/or trickle	-	High	Low

Note: $\overline{CH}_A$ and $\overline{FCC}_A$ are related outputs, but are independent of the states of $\overline{CH}_B$ and $\overline{FCC}_B$, which are also related outputs.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum and minimum allowable values. The battery voltage sense input, $BAT_{A,B}$, for a battery pack must be divided to between 0.95 * V_{CC} and 0.475 * V_{CC} for proper operation. A resistor-divider ratio of:

$$\frac{R1}{R2} = \frac{N}{2.375} - 1$$

is recommended to maintain the battery voltage within the valid range, where R1 is the resistor connected to the positive battery terminal, and R2 is the resistor connected to the respective $SNS_{A,B}$ pins. See Figure 2.

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2005 if V_{CC} is removed with batteries inserted.

The bq2005 requires that the thermistors used for temperature measurements have a negative temperature coefficient. The temperature sense voltage inputs at $TS_{A,B}$ are developed using a resistor-thermistor network between V_{CC} and $SNS_{A,B}$. See Figure 2.

Battery Removal Detection

An external resistor, R_{EXT}, between the battery positive lead and the charging supply input is necessary to allow the bq2005 to detect battery insertion.

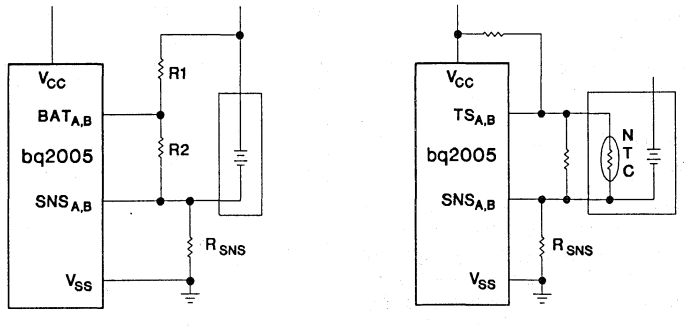


Figure 2. Voltage and Temperature Limit Measurement

Initiating a Charge Action

A battery charge action is initiated with either battery insertion or application of V_{CC} to the bq2005. Battery insertion is recognized when the voltage at either of the $BAT_{A,B}$ pins falls from above the internal V_{MCV} reference level to below that level. When V_{CC} is applied to the bq2005, a charge action begins after a brief power-on reset period.

Temperature and Voltage Prequalification

A charge action is prequalified by the battery temperature and voltage. Before fast charging can begin, the battery temperature and voltage must fall within predetermined acceptable limits.

V_{CELL} is compared to an internal low-voltage reference, V_{EDV}, which is the minimum acceptable battery voltage for fast charging. V_{TEMP} voltage is compared to an internal low-temperature fault reference, V_{LTF}, and the internal hot-temperature fault reference, V_{HTF}. These limits establish the acceptable battery and temperature sense voltage window for fast charge initiation. If the battery fails either of these two prequalifications for charge, the bq2005 enters a charge-pending mode, waiting for the battery voltage and temperature to become acceptable.

In the case of a battery that is too warm or too cold, the charge action starts when the battery temperature becomes acceptable. In the case of deeply discharged batteries (voltage too low), the bq2005 waits until the battery voltage is at an acceptable level before starting fast charge. In the case of a faulty battery, V_{BAT} may never reach an acceptable voltage level, causing the bq2005 to remain in the charge-pending state. The bq2005 continues to trickle charge (if enabled) the battery until the fast charge condition becomes acceptable.

Discharge-Before-Charge

The bq2005 supports discharge-before-charge on battery A, providing battery conditioning as well as capacity calibration. Once activated, the DIS_A pin goes active high until V_{CELL} falls below V_{EDV}, at which time the battery starts fast charge.

If $\overline{DCMD}_A$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with either the application of power to the bq2005 or by battery replaced. A negative-going pulse on $\overline{DCMD}_A$ causes the bq2005 to initiate a discharge-before-charge action on BAT_A regardless of its current charging activity. The $\overline{DCMD}_A$ pin is internally pulled up to V_{CC}; therefore, not connecting this pin results in disabling the discharge-before-charge function. See Figure 3.

Fast charging, top-off, and trickle charge of battery B are not affected during the discharge of battery A.

Fast Charge: TM_1 and TM_2 Pins

When fast charge begins on either of the batteries, the other battery remains in a pending state until the first battery terminates fast charge. At this time, fast charging begins on the second battery. When fast charge of the second battery terminates, optional top-off sequentially proceeds if enabled (program pins TM_1 and TM_2). A pulse-trickle begins on both batteries at the end of top-off or fast charge. Fast charge and optional top-off of battery B always take precedence over battery A when both batteries are present.

The TM_1 and TM_2 pins are three-level input pins used to select the various charge and top-off rates, maximum safety times, and -ΔV hold-off period. Table 3 describes the various states selected by the TM_1 and TM_2 pins.

Once temperature and voltage prequalifications are met and any requested discharging of the battery is completed, fast charging begins and continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV)
- Maximum temperature
- Maximum charge time
- Maximum battery voltage

Voltage Termination Hold-off

At the start of fast charging, there is a hold-off time during which the -ΔV termination is disabled (see Table 3). Once past the initial fast charge hold-off time, -ΔV termination is re-enabled. ΔT/Δt, maximum cell voltage (MCV), and maximum temperature (TCO) terminations are not affected by the hold-off period.

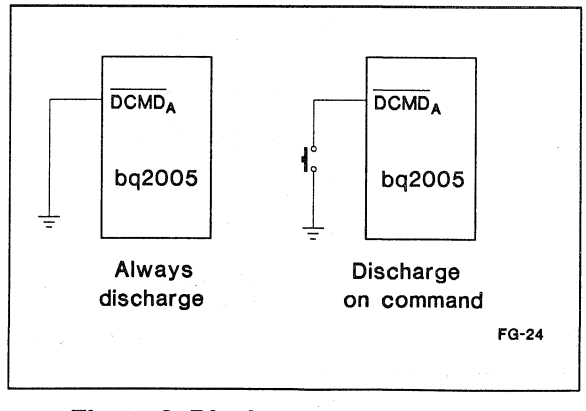


Figure 3. Discharge-Before-Charge

-ΔV Termination

The bq2005 makes a termination decision based on negative delta voltage every 32 seconds. If V_{CELL} is lower than any previously measured value by 13mV typical, the fast charge phase of the charge action is terminated. This equates to a -ΔV termination of -6mV per cell typical. The -ΔV test is valid only for:

$$0.475 * V_{CC} \leq V_{CELL} \leq 0.95 * V_{CC}$$

-ΔV detection may be enabled or disabled at any time using the DVEN pin.

ΔT/Δt Fast Charge Termination

The bq2005 makes a termination decision based on delta temperature/delta time (ΔT/Δt) every 32 seconds. If V_{TEMP} is 16mV (typical) less than the voltage measured 64 seconds previously, the fast charge phase of the charge is terminated.

The ΔT/Δt test is valid only for:

$$0.2 * V_{CC} \leq V_{TEMP} \leq 0.4 * V_{CC}$$

Maximum Voltage, Maximum Time, and Maximum Temperature Safety Terminations

The bq2005 also terminates fast charge for maximum temperature (TCO), maximum time, and maximum voltage (MCV). MCV and TCO reference levels provide the maximum limits for battery voltage and temperature during fast charging. If either of these limits is exceeded, both fast charging and optional top-off charge are terminated. MCV is treated as a fault, so $\overline{FCC}_{A,B}$ and $\overline{CH}_{A,B}$ become inactive with this condition.

Maximum time selection is programmed using the TM_1 and TM_2 pins (see Table 3). Time settings are available for corresponding charge rates ranging from C/4 to 4C.

Temperature Monitoring

Temperature is represented as a voltage input on the bq2005 at the TS_A and TS_B pins. Generally this voltage is developed from an NTC (negative temperature coefficient) thermistor referenced to the negative battery terminal. The bq2005 recognizes an internal voltage level of $V_{LTF} = 0.4 * V_{CC}$ as the low-temperature fault (LTF) level. If $V_{TEMP} \geq V_{LTF}$, charging is inhibited or terminated.

Table 3. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast Charge Rate	TM_1	TM_2	Fast Charge Safety Time (minutes)	-ΔV Hold-Off Time (seconds)	Top-Off	Pulse-Trickle Rate	Pulse-Trickle Period (Hz)
			Typical	Typical			
C/4	Low	Low	360	137	N	Disabled	Disabled
C/2	Float	Low	180	820	N	C/32	240
1C	High	Low	90	410	N	C/32	120
2C	Low	Float	45	200	N	C/32	60
4C	Float	Float	23	100	N	C/32	30
C/2	High	Float	180	820	Y	C/64	120
1C	Low	High	90	410	Y	C/64	60
2C	Float	High	45	200	Y	C/64	30
4C	High	High	23	100	Y	C/64	15

Note: $T_A = 25°C$, $V_{CC} = 5.0V$.

Similarly, the external reference voltage level presented at the TCO pin represents the high-temperature cut-off point at which fast charging is terminated. V_{TCO} should always be less than V_{LTF} to ensure proper device operation.

All temperature prequalifications and $\Delta T/\Delta t$ termination may be disabled by connecting TCO to V_{SS} and fixing the $TS_{A,B}$ pin level to 0.2 * V_{CC}. $\Delta T/\Delta t$ termination sensitivity is user-adjustable, depending on the values of the external resistor-divider network.

Top-Off Charge

An optional top-off charge phase is selected to follow fast charge termination for charge rates from C/2 to 4C. This option is selected through the TM_1/TM_2 programming pins (see Table 3).

If selected, the bq2005 "tops off" the battery at the pulsed rate. The charge control cycle is modified so that $MOD_{A,B}$ pins are activated for only 4 of every 32 seconds. This results in a rate 1/8th that of fast charging. Top-off charge proceeds for a time equal to the fast charge safety time. Temperature (TCO) and voltage (MCV) terminations are the only termination methods enabled during "top-off." Any fast charge initiation immediately terminates a top-off charge in progress.

Pulse-Trickle Charge

Pulse-trickle charge is used to compensate for self discharge of the battery while idle in the charger, and to bring a depleted battery to a valid charge voltage prior to fast charge. Both batteries pulse-trickle at the end of fast charge and top-off, and prior to charge (see Table 1).

In the pulse-trickle state, MOD_A and MOD_B are separately active for 260µs of a period specified by the state of TM_1 and TM_2 pins. The resulting trickle rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Pulse-trickle and top-off can be disabled by tying TM_1 and TM_2 to V_{SS}. Fast charge or top-off of either battery suspends pulse-trickle.

Charge Current Control

The bq2005 controls charge current through the $MOD_{A,B}$ output pins. The current control is designed to support implementation of a constant-current switching regulator. See Figure 4. Nominal regulated current is:

$$I_{REG} = 0.225V / R_{SNS}$$

When used in this configuration, the charge current is monitored at the $SNS_{A,B}$ input by the voltage drop across a resistor, R_{SNS}. R_{SNS} may be chosen to provide a variety of charging currents and may differ between slots A and B.

The $MOD_{A,B}$ pins are switched high or low depending on the voltage input to the $SNS_{A,B}$ pins. If the voltage at the $SNS_{A,B}$ pins is less than V_{SNSLO} (0.2V typical), the MOD outputs are switched high to gate charge current through the inductor to the battery. When the SNS voltage is greater than V_{SNSHI} (0.25V typical), the MOD outputs are switched low—shutting off current from the supply.

The $MOD_{A,B}$ pins can also be used to gate an external charging current source. When an external current source is used, a sense resistor is not required, and the $SNS_{A,B}$ pins are connected to V_{SS}. See Figure 5.

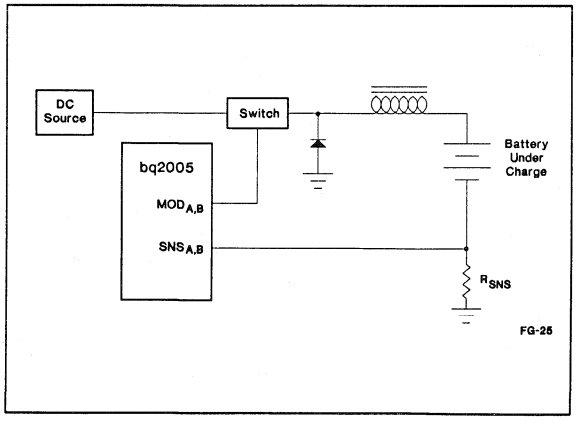


Figure 4. Constant-Current Switching Regulation

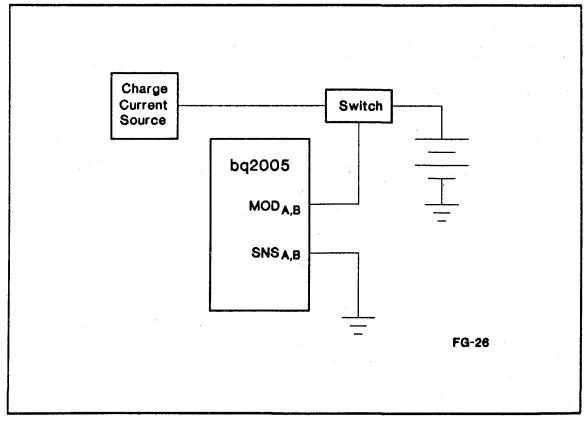


Figure 5. External Current Regulation

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (TA = TOPR; VCC ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = Low	0.05 * V_{CC}	±0.025	V	
V_{SNSLO}	Low threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = High	V_{SNSHI} – (0.01 * V_{CC})	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	(¼ * V_{LTF}) + (¾ * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.475 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits charge
V_{MCV}	Maximum cell voltage	0.95 * V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge

Note: $V_{CELL} = V_{BAT} - V_{SNS}$.

$V_{TEMP} = V_{TS} - V_{SNS}$.

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}_A$, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}_A$, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS_A, $MOD_{A,B}$, $I_{OH} \leq$ -5mA (see Figure 6)
V_{OL}	Logic output low	-	-	0.5	V	DIS_A, $\overline{FCC}_{A,B}$, $\overline{CH}_{A,B}$, $MOD_{A,B}$, $I_{OL} \leq$ 5mA (see Figure 6)
I_{CC}	Supply current	-	1.0	3.0	mA	Outputs unloaded
I_{OH}	DIS_A, $MOD_{A,B}$ source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	DIS_A, $\overline{FCC}_{A,B}$, $MOD_{A,B}$, $\overline{CH}_{A,B}$ sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_L	Input leakage	-	-	±1	µA	DVEN, V = V_{SS} to V_{CC}
		-	-	-400	µA	$\overline{DCMD}_A$, V = V_{SS}
I_{IL}	Logic input low source	-	-	70.0	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70.0	-	-	µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0	-	2.0	µA	TM_1, TM_2 should be left disconnected (floating) for Z logic input state
I_{BAT}	Input current to $BAT_{A,B}$ when battery is removed	-	-	-20	µA	V_{CC} = 5.0V; T_A = 25°C; input should be limited to this current when input exceeds V_{CC}.
V_{THERM}	$\Delta T/\Delta t$ detection threshold from $TS_{A,B}$	-	16 ± 4	-	mV	V_{CC} = 5.0V, T_A= 25°C
-ΔV	Negative delta voltage detection	-	13 ± 4	-	mV	V_{CC} = 5.0V, T_A= 25°C

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$R_{BATA,B}$	Battery A/B input impedance	50	-	-	MΩ
$R_{TSA,B}$	$TS_{A,B}$ input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
$R_{SNSA,B}$	$SNS_{A,B}$ input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD_A}$ pulse command	1	-	-	µs	Pulse start for charge or discharge-before-charge
d_{FCV}	Fast charge safety time variation	0.84	1.0	1.16	-	V_{CC} = 4.5V to 5.5V; see Table 3.
t_{REG}	MOD output regulation frequency	-	-	300	kHz	Typical regulation capability; V_{CC} = 5.0V
t_{MCV}	$V_{CELL} \geq V_{MCV}$ valid period	-	-	1	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV}, then a transition of $V_{CELL} < V_{MCV}$ is recognized as battery replaced. Otherwise, $V_{CELL} < V_{MCV}$ is ignored.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

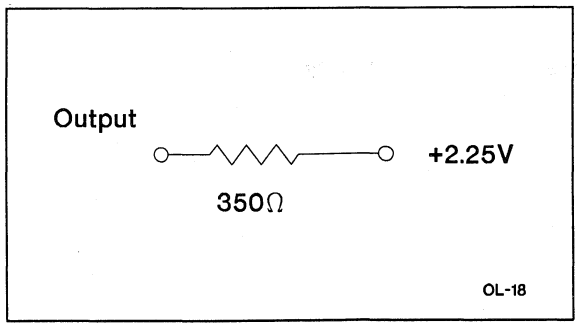


Figure 6. Output Load

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2-142	Input leakage (I_L)	Was ± 400µA; $\overline{DCMD}_A$, V = V_{SS} to V_{CC}; is -400µA; $\overline{DCMD}_A$, V = V_{SS}.
2	2-142	Input current to $BAT_{A,B}$ when battery is removed (I_{BAT})	Was -1.0mA maximum; is -20µA maximum.

Note: Change 1 = July 1993 B "Preliminary" changes from May 1993 A draft data sheet.
Change 2 = Nov. 1993 C "Final" changes from July 1993 B "Preliminary."

Ordering Information

bq2005 -

- Temperature:
  - blank = Commercial (-20 to +70°C)
  - N = Industrial (-40 to +85°C)*
- Package Option:
  - PN = 20-pin narrow plastic DIP
  - S = 20-pin SOIC
- Device:
  - bq2005 Dual-Battery Fast Charge IC

* Contact factory for availability.

DV2005L1

Fast Charge Development System

Control of PNP Power Transistor

Features

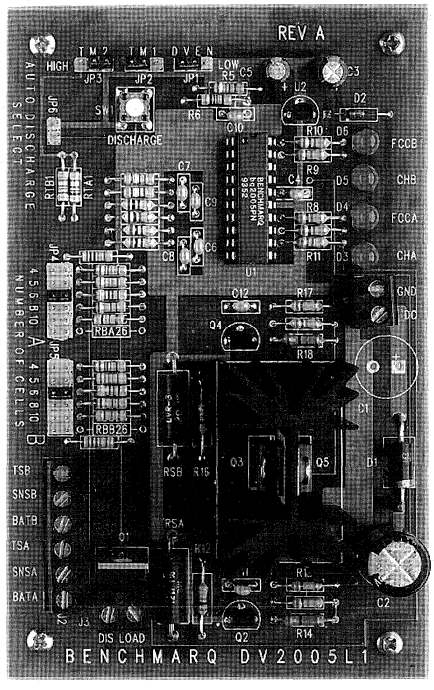
- bq2005 fast charge control evaluation and development
- Charge current sourced from two on-board frequency-modulated linear regulators (up to 3.0 A)
- Fast charge control and conditioning for one or two NiMH and/or NiCd batteries containing 4 to 10 NiCd or NiMH cells; user-configurable for applications that use other numbers of cells
- Sequential charging of two battery packs
- Fast charge termination by $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, time, and voltage
- $-\Delta V$ enable, hold-off, top-off,trickle rate, maximum charge time, and number of cells are jumper-configurable
- Charging status displayed on LEDs (two for each battery)
- Discharge-before-charge control with push-button switch for battery A
- Selectable pulsed "top-off" charge and trickle charge

General Description

The DV2005L1 Linear Development System provides a development environment for the bq2005 Dual-Battery Fast Charge IC. The DV2005L1 incorporates a bq2005 and two frequency-modulated linear regulators to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, and maximum voltage. Jumper settings select the $-\Delta V$ enabled state, select the hold-off, top-off, trickle, and maximum time limits.

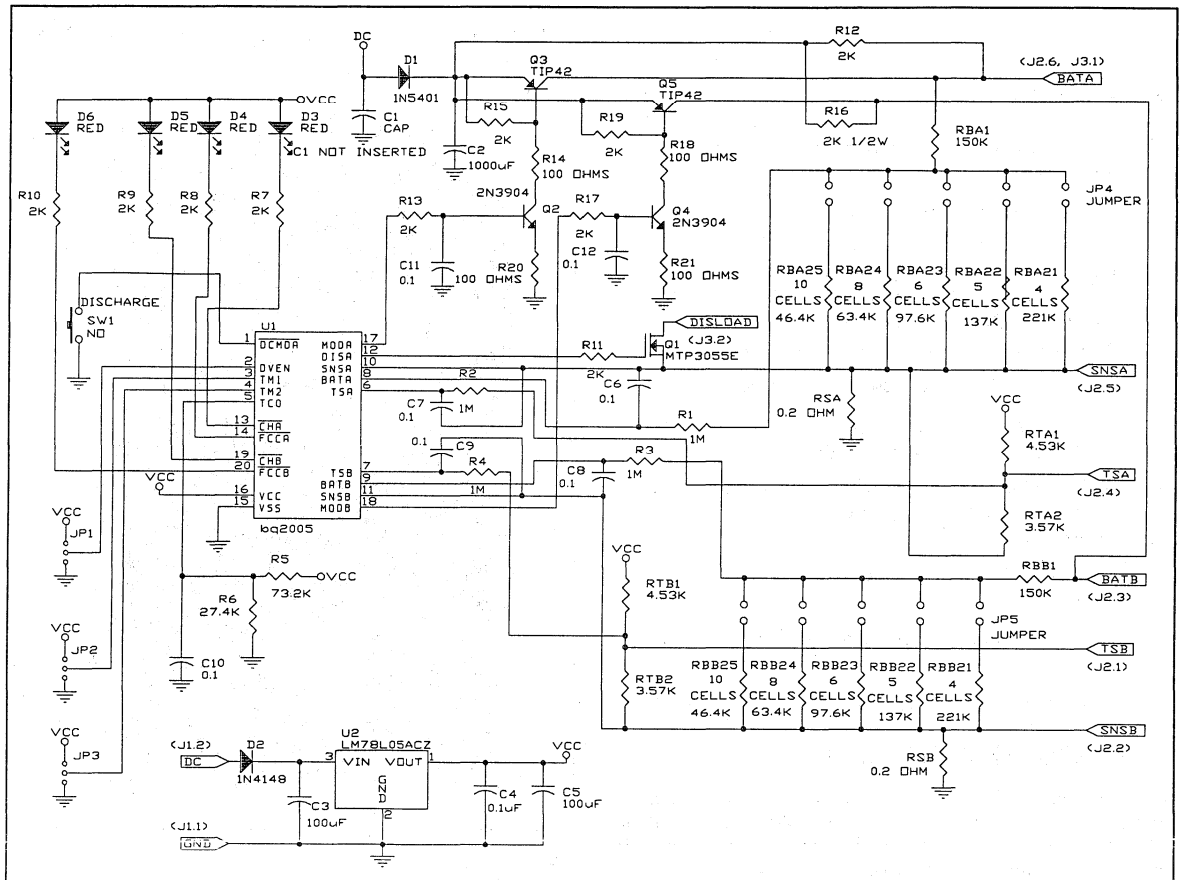
The user provides a power supply and batteries. The user configures the DV2005L1 for the number of cells, $-\Delta V$ charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.



Contents

1	DV2005L1 printed circuit board containing: a) bq2005 PDIP IC b) Dual frequency-modulated linear current regulator with common heat sink c) All programming jumpers d) 2 NTC thermistors
1	bq Charge Configuration diskette
1	Documentation kit including user's guide, schematics, and data sheets

DV2005L1 Board Schematic



Thermistor values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

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BENCHMARQ

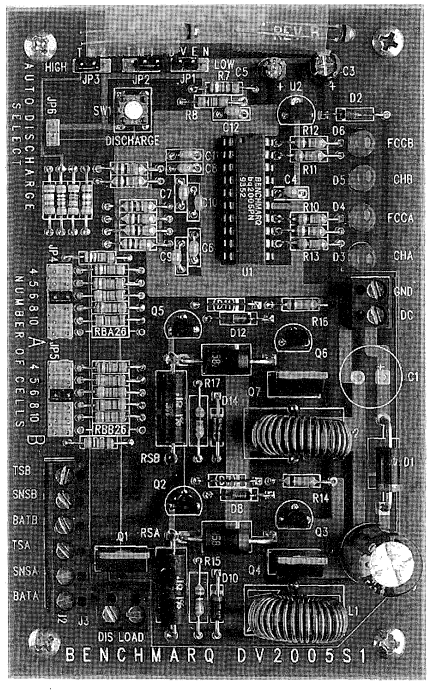
DV2005S1

Fast Charge Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2005 fast charge control evaluation and development
- Charge current sourced from two on-board switch-mode regulators (up to 3.0 A)
- Fast charge control and conditioning for one or two NiMH and/or NiCd batteries containing 4 to 10 NiCd or NiMH cells; user-configurable for applications that use other numbers of cells
- Sequential charging of two battery packs
- Fast charge termination by ΔT/Δt, -ΔV, maximum temperature, time, and voltage
- -ΔV enable, hold-off, top-off,trickle rate, maximum charge time, and number of cells are jumper-configurable
- Charging status displayed on LEDs (two for each battery)
- Discharge-before-charge control with push-button switch for battery A
- Integrated switching charge current controller to 300KHz
- Selectable pulsed "top-off" charge and trickle charge



General Description

The DV2005S1 Switching Development System provides a development environment for the bq2005 Dual-Battery Fast Charge IC. The DV2005S1 incorporates a bq2005 and two buck-type switch-mode regulators to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: ΔT/Δt, -ΔV, maximum temperature, maximum time, and maximum voltage. Jumper settings select the -ΔV enabled state, select the hold-off, top-off, trickle, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2005S1 for the number of cells, -ΔV charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands discharge-before-charge with a push-button switch.

Connection Descriptions

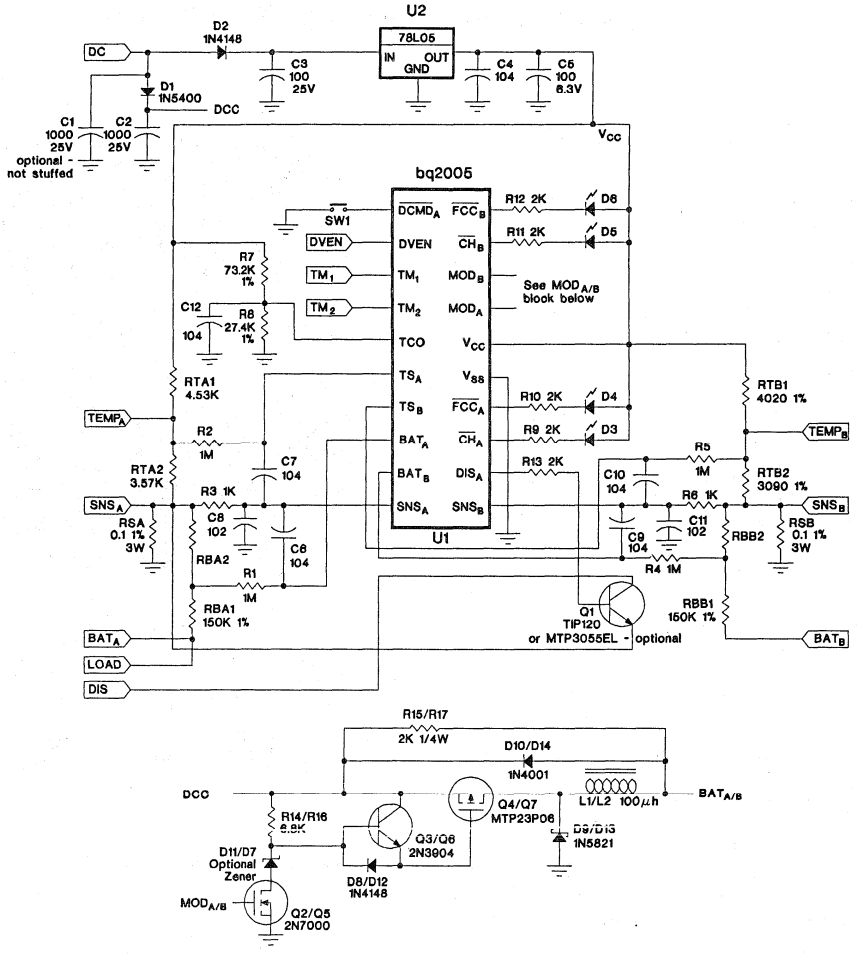
1 DV2005S1 printed circuit board containing:

a) bq2005 PDIP IC
b) Dual switch-mode current regulator
c) All programming jumpers
d) 2 NTC thermistors

1 bq Charge Configuration diskette

1 Documentation kit including user's guide, schematics, and data sheets

DV2005S1 Board Schematic



Thermistor values:

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Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.53K	3.57K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

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Rev. B Board

BENCHMARQ

Using the bq2005 to Control Fast Charge

Introduction

This application note describes the use and functions of the bq2005 controlling a current source to fast charge NiCd or NiMH batteries. The bq2005 may also serve as the modulator for a switching-mode constant-current regulator to provide an efficient charge current source. Examples illustrate the ease with which the bq2005 is incorporated into applications.

The bq2005 is targeted for applications requiring state-of-the-art dual-battery fast-charging at minimal cost. It provides sophisticated full-charge detection techniques such as ΔT/Δt (delta temperature/delta time) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2005 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

A significant advantage of the bq2005 over other fast-charge solutions is the use of ΔT/Δt and/or -ΔV as the primary decisions for fast-charge termination. ΔT/Δt detection is one of the most sensitive and reliable methods for fast-charge termination when charging NiMH and NiCd batteries. Near full charge, the temperature rise begins to accelerate. The ΔT/Δt decision typically precedes the peak voltage, allowing for minimal overcharge stress. The ΔT/Δt method also tolerates varying rates of charge, which may be desirable when charging during system operation.

Compared to the ΔT method, which uses two sensors to monitor battery temperature and ambient temperature, the ΔT/Δt method uses a single thermistor to monitor the rate of temperature increase. This approach is more sound in cases when the initial battery temperature may be significantly different from the ambient temperature. This ΔT/Δt termination decision can easily be disabled.

An input from a battery voltage divider enables the bq2005 to detect -ΔV, which is a very reliable charge terminator for NiCd batteries and most NiMH batteries, depending on the application. -ΔV detection in the bq2005 may be temporarily disabled during periods when the charge current fluctuates greatly or during the beginning of a fast charge to eliminate false peaks. -ΔV termination is logic-level selectable without affecting other termination choices.

To help ensure safety for the battery and system, fast charging may also be terminated at a high-temperature cutoff threshold (TCO), a safety time period, or a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2005 disables -ΔV detection during a short "hold-off" period at the start of fast charge. This hold-off period is configured as described in the bq2005 data sheet.

The bq2005 may be configured to have two or three charge stages. In a two-stage configuration, the fast-charge stage controlled by the bq2005 is preceded and followed by a pulse-trickle charge at a rate controlled by the programming pins of the bq2005. In a three-stage configuration, the fast charge is followed by a top-off charge stage at ⅛ the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, a trickle charge at a pulsed rate equivalent to C/64 is supplied to the battery to compensate for self-discharge

Basic Charge-Control Operation

Three detailed applications follow this section. One provides direct control of a linear regulator, and the other two provide switch-mode current rgulation.

Gating Current

Figure 1 shows an example of external source gating. With SNS tied to V_{SS}, the bq2005 enables charge current to the battery by asserting MOD at the start of charge and maintaining this state until charge is terminated. In this example, R1, Q2, R4, R5, R6, and Q1 form the switching circuit. MOD drives Q2 into conduction—saturating Q1.

The current-handling capability of this circuit depends on the components selected to perform the switching and current-regulation functions. Table 1 shows some suggested component combinations for corresponding currents.

The voltage-boost circuit shown in Figure 1 is necessary to keep the voltage on either BAT_A or BAT_B above MCV while the other battery is charging (assumes only one battery is inserted). This implementation is limited to 15V DC. Please contact Benchmarq's Applications Group for assistance with other input voltage configurations, or for alternative methods.

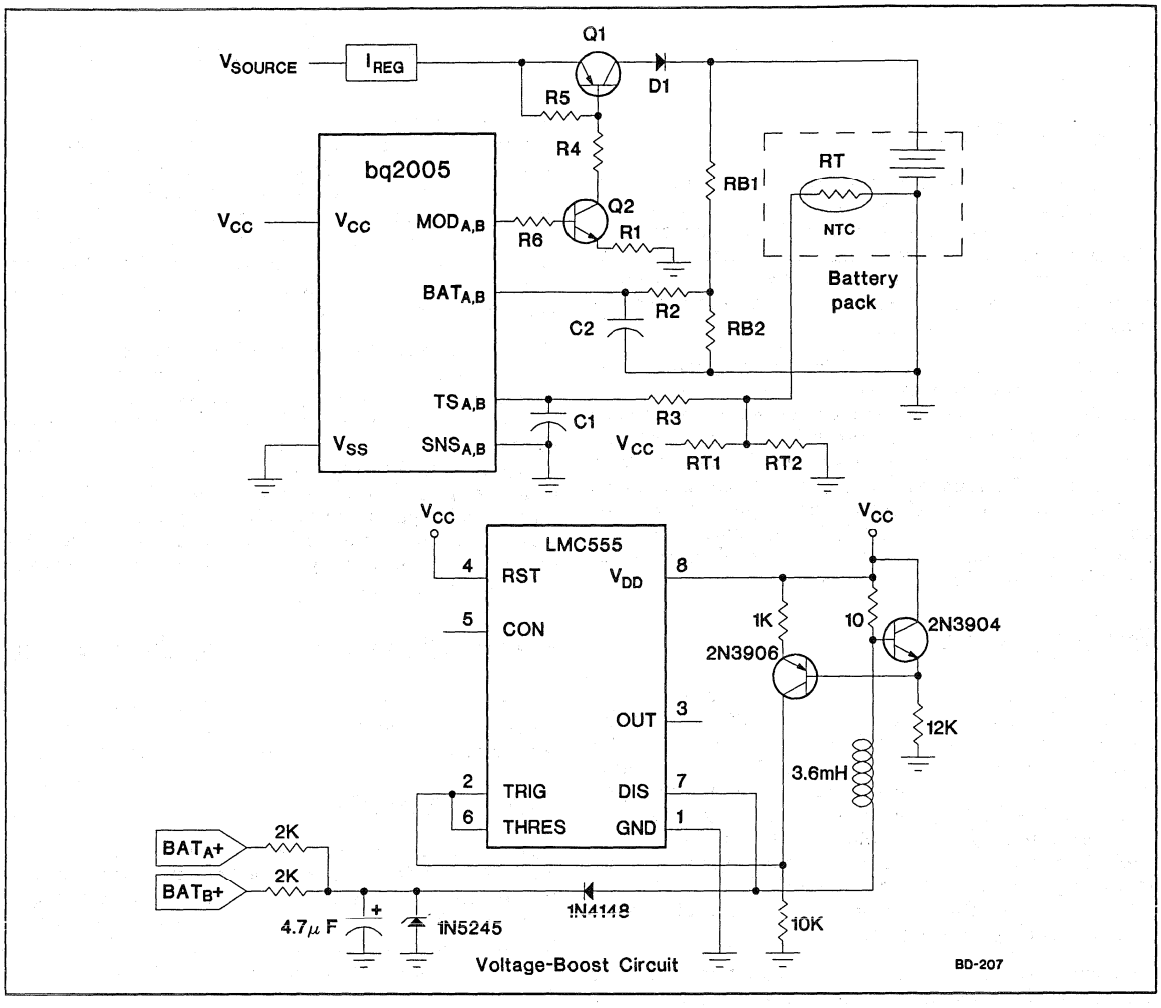


Figure 1. Gated External Source (Bipolar Switch Option)

Table 1. Suggested Component Combinations

I_{IN}	Q1	Q2	R1	R4	R5	R6
0.5A	MPS750	2N3904	150Ω ¼W	–	1KΩ	–
1A	MPS750	2N3904	68Ω ½W	100Ω ½W	1KΩ	–
2A	TIP42	2N3904	43Ω ½W	51Ω ½W	200Ω	–
3A	TIP42	2N3904	27Ω 1W	27Ω 1W	200Ω	–
5A	IRFR9010	2N3904	100Ω ¼W	–	1KΩ	33KΩ
8A	IRF9Z22	2N3904	100Ω ¼W	–	1KΩ	33KΩ

Charge Initiation

Charge may be initiated by applying power to the IC or by battery insertion. Charge initiation by application of power to the IC works as follows: When V_{CC} is applied, the bq2005 is held in reset for approximately one and one-half seconds. At the end of the reset period, a charge cycle initiates as soon as conditions allow. If both batteries are present, fast-charging battery B takes precedence over charging battery A. If battery A is inserted while fast charge is pending on battery B, the bq2005 trickle charges both batteries, and then fast charges battery B after conditions allow. If battery B is inserted while fast charge is pending on battery A, the bq2005 trickle charges both batteries, and then fast charges battery B when conditions allow.

Charge initiation on battery replacement relies on the $BAT_{A,B}$ pin voltage being greater than MCV in the absence of a battery, and falling below MCV when the battery is connected. To ensure this condition, resistor R7 in Figure 1 is sized to elevate the empty battery location voltage such that MCV is exceeded.

When the battery is replaced, the voltage on $BAT_{A,B}$ should fall below MCV, at which time a charge cycle initiates as soon as conditions allow.

Table 2, Charge Action Truth Table, describes the bq2005 charge actions under a variety of battery and charge states.

Discharge-Before-Charge, Battery A

It may occasionally be desirable to discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 2 illustrates the implementation of this function. If $\overline{DCMD}_A$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with battery replaced on application of power to the bq2005. A negative strobe signal on $\overline{DCMD}_A$ also initiates discharge-before-charge. **This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS_A to a high state until the voltage sensed on BAT_A falls below V_{EDV} (0.475 * V_{CC}).** Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

The discharge-before-charge function is ignored or terminated when $V_{BAT} - V_{SNS} > V_{MCV}$ (battery removed). If the discharge-before-charge function is not desired, $\overline{DCMD}_A$ should be tied to V_{CC} or left floating. $\overline{DCMD}_A$ is internally pulled up to V_{CC}.

Table 2. Charge Action Truth Table

V_{CC}	BAT_A	BAT_B	Charge Action
0→5V	V	V	Fast charge B, pend A
0→5V	V	N	Fast charge A
0→5V	N	V	Fast charge B
5V	↑	F	Fast charge B, pend A
5V	↑	L	Trickle A and B, fast charge B and pend A when conditions allow
5V	L	↑	Trickle A and B, fast charge B and pend A when conditions allow
5V	F	↑	Fast charge A, pend B
5V	D	L	Trickle A, trickle B
5V	L	D	Trickle A, trickle B
5V	D	V	Fast charge B, pend top-off A
5V	V	D	Fast charge A, pend top-off B
5V	D	D	Top off B, trickle A, then top off A, trickle B
5V	D	↑	Abort top-off A
5V	↑	D	Abort top-off B
5V	T	L	Trickle A, trickle B
5V	L	T	Trickle A, trickle B
5V	T	V	Fast charge B, pend trickle A
5V	V	T	Fast charge A, pend trickle B
5V	T	T	Trickle A, trickle B

V = Battery inserted and valid charge conditions:
$V_{DIV} = V_{BAT} - V_{SNS}$
$0.475 * V_{CC} \le V_{DIV} \le 0.95 * V_{CC}$
$0.4 * V_{CC} \ge V_{TS} \ge V_{HTF}$

L = Battery inserted and outside temperature limit or below V_{EDV}.

N = Battery removed: $V_{DIV} > 0.95 * V_{CC}$

F = Fast charge

D = Top-off

T = Trickle

↑ = Battery insertion: V_{DIV} transitioning from ≥ $0.95 * V_{CC}$ to $V_{DIV} \le 0.95 * V_{CC}$

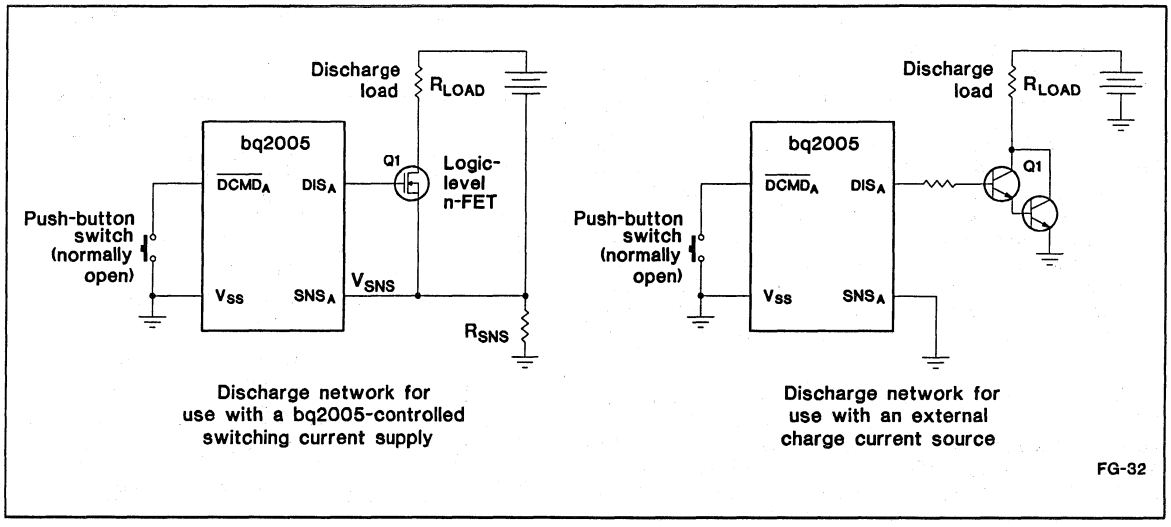


Figure 2. Battery Conditioning Network

Configuring the $BAT_{A,B}$ Inputs

The bq2005 uses the battery voltage sense input on the $BAT_{A,B}$ pins to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, and facilitate negative delta voltage (-ΔV) detection.

V_{BAT} may be derived from a simple passive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range, which is between V_{MCV} and V_{EDV} ($0.475 * V_{CC} \leq V_{DIV} \leq 0.95 * V_{CC}$).

For NiCd and NiMH batteries, the battery terminal voltage is divided down to this potential per the following equation:

$$\frac{RB1}{RB2} = \frac{N}{2.375} - 1$$

where N = number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative $SNS_{A,B}$ pins.

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the $BAT_{A,B}$ pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from $BAT_{A,B}$ between 20KΩ and 1MΩ is acceptable over the bq2005 operating range. Total impedance between the battery terminal and V_{SS} should typically be about 300KΩ to 1MΩ . See Table 3.

Note: Because V_{SNS} may be above V_{SS} in bq2005 switching regulation applications, the actual internal comparison uses $V_{BAT} - V_{SNS}$, or V_{DIV}. This internal value V_{DIV} maintains a representative comparison voltage independent of any current through R_{SNS}.

Table 3. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1	RB2
3	137 KΩ	523 KΩ
4	357 KΩ	523 KΩ
5	309 KΩ	280 KΩ
6	301 KΩ	196 KΩ
7	316 KΩ	162 KΩ
8	649 KΩ	274 KΩ
9	383 KΩ	137 KΩ
10	442 KΩ	137 KΩ
12	412 KΩ	102 KΩ
14	499KΩ	102 KΩ
16	649 KΩ	113 KΩ

MCV

Battery over-voltage protection is accomplished by comparing V_{DIV} to the internal MCV reference. If V_{DIV} becomes greater than V_{MCV}, then charging, top-off, and trickle charge terminate, and $\overline{CH}_{A,B}$ and $\overline{FCC}_{A,B}$ outputs are high impedance.

A typical MCV value equates to 2.0V per cell. To detect the presence of a battery, the DC supply voltage must be greater than 2.0 * N, where N is the number of battery cells. Battery packs with fewer than three cells require an external amplifier to use the bq2005 (see Figure 3).

Temperature Sensing and the TCO Pin

The bq2005 uses the temperature sense input on the $TS_{A,B}$ pins to qualify charge initiation and termination. A negative temperature coefficient (RNTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 4. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT. If this temperature sensor is to be used for charge control, it should be in direct contact with the cells.

2

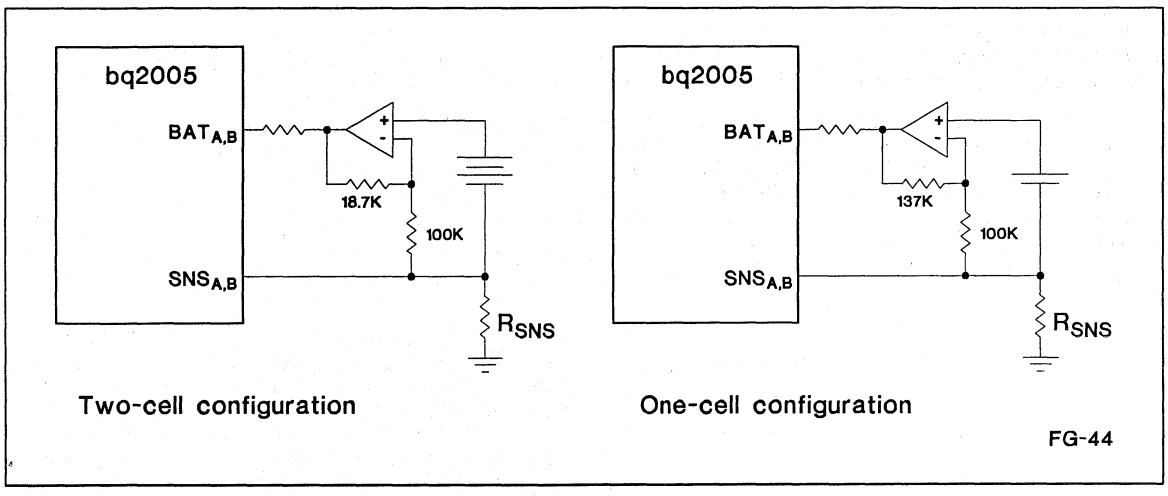


Figure 3. Battery Cell Voltage Amplifier for <3 Cells

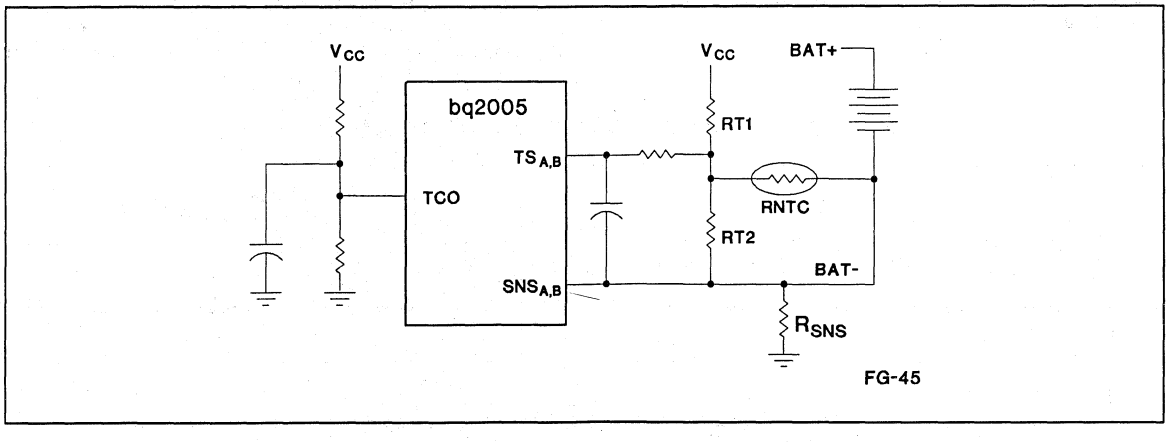


Figure 4. Temperature Sense Inputs

Temperature-decision thresholds are defined as LTF (low-temperature fault), HTF (hot-temperature fault), and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-HTF range. In this case, $\overline{CH}_{A,B}$ is alternating high and low at a 4Hz rate, and charging does not initiate until the battery temperatures enter this range.

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2005 interprets the reference points V_{LTF}, V_{HTF}, and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at 2/5 V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 5. Note that since the voltage on pin $TS_{A,B}$ - decreases as temperature increases, v_{TCO} should always be less than 2/5 V_{CC}. V_{HTF} is set internally 3/4 of the way from V_{LTF} to V_{TCO}. The resistive dividers shown in Figure 4 may be used to generate the desired V_{TCO}.

$\Delta T/\Delta t$ detection adds an additional constraint on the selection of temperature sense components. Detection occurs when the voltage $TS_{A,B} - SNS_{A,B}$ declines at a rate between 0.0024 V_{CC} and 0.0040 V_{CC} per 68 seconds, with a nominal 5V V_{CC} producing a nominal detection rate of 14mV/min (16mV/68sec). For example, assuming a 1°C/min desired average $\Delta T/\Delta t$ detection rate ($T_{\Delta T}$), and minimum and maximum charge temperatures of 0° and 40°C, respectively, V_{TCO} equals:

$$V_{TCO} = (2 * V_{CC}/5) - (0.0028 * V_{CC} * (T_{TCO} - T_{LTF}))$$

$$= 2 - (0.014 * (40 - 0))$$

$$= 1.44V$$

Table 4 shows the temperature control values that apply for the application example assuming the Philips thermistor. Appendix A explains the derivation of such component values.

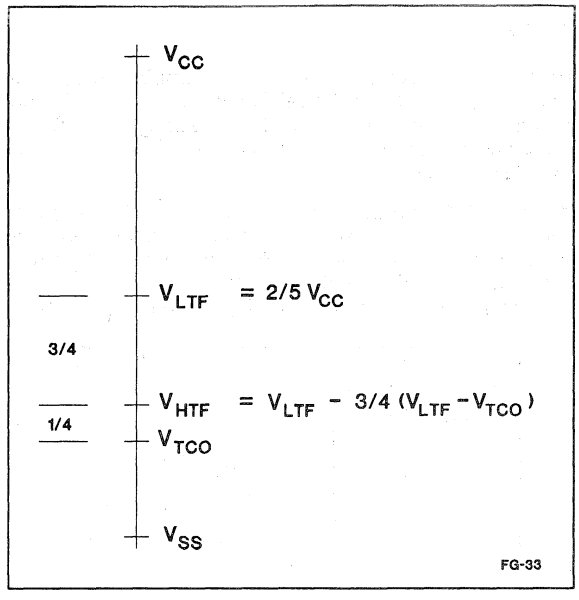


Figure 5. Temperature Reference Points

New $\Delta T/\Delta t$ samples are processed every 34 seconds. To minimize the risk of premature termination, the design should be configured assuming a minimum charge cutoff rate of 0.0024 * V_{CC}, or 10.6mV per minute (at 25°C; V_{CC} = 5V). This is the lowest signal that may be recognized as meeting the decision threshold. Repeating samples cause a decision quickly as the voltage ramps between this minimum threshold and the nominal 14mV per minute. The system is self-compensating in that the thermistor provides increasingly overstated negative voltage change with increasing temperature, making the measurement more sensitive at higher temperatures. The last three columns of Table 4 are an example of this relationship.

Table 4. Example Values, Temperature Sense Network

LTF (°C)	HTF (°C)	TCO (°C)	V_{TCO} (V)	RT1 (KΩ)	RT2 (KΩ)	$T_{\Delta T}$ (°C/min)	Minimum-to-Nominal $\Delta T/\Delta t$ Rate (°C/min)		
							@ 25°C	@ 35°C	@ 45°C
10	44.4	50	1.303	5110	4120	1.00	0.75–1.00	0.63–0.83	0.56–0.74

Notes:
1. V_{SR} = 0V.
2. Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin $TS_{A,B}$ to 0.2 * V_{CC}.

Vcc Supply

The Vcc supply provides both power and voltage reference to the bq2005. This reference directly affects the internal time-base voltage measurements.

The time-base is trimmed during manufacturing to within 5 percent of the typical value with Vcc = 5V. The oscillator varies directly with Vcc. If, for example, a 5% regulator supplies Vcc, the time-base could be in error by as much as 10%.

For applications requiring even more cost-cutting measures, using a Zener diode-resistor combination as the bq2005 power supply sacrifices very little accuracy and performance. To minimize +5V loading, LEDs are cascode-driven as shown in Figure 6.

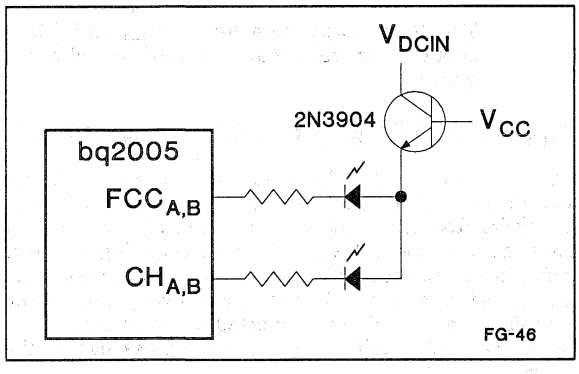


Figure 6. Cascode-Driven LEDs

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2005 Vcc supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the proper charge operation and the rated current, V_{DC} must be greater than the number of cells * 2V + V_{LOSS} in the charging path.

Battery Removal Detection

An external 2K resistor in Figure 1 is sized to pull $BAT_{A,B}$ above MCV with the removal of the battery. The resistance of R7 should be selected to pull the battery sense pin above MCV and yet keep input current on $BAT_{A,B}$ less than 20μA.

Top-Off Charge

The top-off charge option allows for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off is needed for NiMH batteries, which accept charge poorly at charge states above 85%. Top-off occurs at a 1/8 pulsed rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. Top-off terminates if TCO or MCV is exceeded or if charge or discharge is initiated on the other battery. Top-off has a lower priority than charge; it pends until both batteries have been charged and then charges the batteries in sequence—first battery B and then battery A.

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use. Top-off is also not necessary for NiCd batteries.

Negative Delta Voltage Fast-Charge Detection

-ΔV full-charge detection may operate in parallel with ΔT/Δt detection. If temperature control is disabled by design, then -ΔV should be enabled (DVEN tied to Vcc). If -ΔV is enabled, a constant-current charging source is required. Otherwise a drop in current may cause a false -ΔV determination. DVEN may change state at any time.

Mode Selection Pins TM_1 and TM_2

These two pins are used to select the safety time-out (five selections, 23 to 360 minutes) and optional top-off charge (four selections, 23 to 180 minutes, equal to the safety time selection).

The safety time-out should be selected to be longer than any reasonably expected charge time. The nominal charge time (Ah capacity/charge rate) should be increased to allow for both charge inefficiency and the fact that many batteries hold more than the rated charge. A safety time-out 1.3–1.5 times the nominal time is normally adequate (i.e., 90 minutes for a 1C charge). The safety time-out may be far in excess of the nominal charge time if temperature termination is enabled.

Note: If the charge rate varies (such as fast charging during system operation using ΔT/Δt termination), then the safety time-out selection should allow for the slowest charges that may occur. The 180- or 360-minute selection may be appropriate.

In addition to selecting the safety timer period and top-off enabled/disabled, TM_1 and TM_2 select the appropriate pulse trickle period. C/32 is recommended for NiCd cells, while C/64 is recommended for NiMH batteries. Top-off and pulsed trickle can be disabled by tying TM_1 and TM_2 low, selecting a six-hour charge time-out. TM_1 and TM_2 may be changed at any time during a charge cycle to select different conditions; however, changing them during charge may result in an indeterminate time-out period. TM_1 and TM_2 are held constant throughout the entire charge cycle.

System-Controlled Charge Inhibition

System control of battery charging is best accomplished by driving the temperature and voltage sense pins high, terminating or inhibiting charge. Driving $\overline{INH}$ voltage to V_{SS} results in a transition at the $BAT_{A/B}$ sense pin, terminating any fast charge, top-off, or trickle in process. When $\overline{INH}$ transitions to V_{CC}, charging is reinitiated if a battery is present and within temperature and voltage limits. See Figure 7.

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by 1V to 2V. For maximum efficiency, a polyswitch may be used in combination with a suitably sized Schottky diode reversed across the electronics.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2005 is important when the bq2005 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept isolated from the bq2005 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the V_{CC} pin.

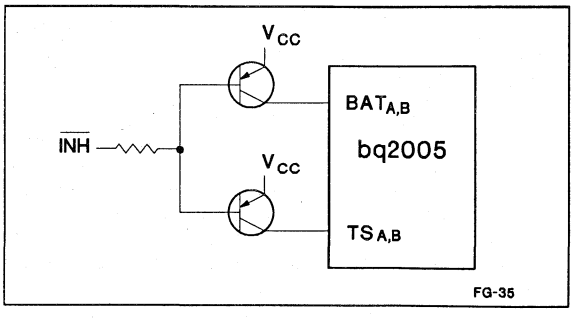


Figure 7. Inhibit Battery Charging Circuit

4. 0.1µF capacitors and resistors forming R-C filters connected to pins $BAT_{A,B}$, $TS_{A,B}$, and TCO should be as close as possible to their associated pins.
5. Because the bq2005 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the $\overline{DCMD_A}$ input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2005-modulated switching applications:
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the $SNS_{A,B}$ pins.
   - The 0.1µF capacitors for $BAT_{A,B}$ and $TS_{A,B}$ should be routed directly to $SNS_{A,B}$ and not to ground.

Application Example 1: Linear Regulator

In the frequency-modulated example of Figure 8, the bq2005 is used to implement a linear regulator/charge controller that can charge 4, 5, 6, 8, or 10 NiCd or NiMH cells (selected by JP4 and JP5) by controlling the base drive to a series pass PNP transistor. The current must be limited to stay within the power dissipation of the transistor in free air or connected to an appropriately sized heat sink. Table 5 contains the parts list for the board.

Charge is initiated on battery replacement or power-up. Jumper JP1 controls -ΔV detection: selecting V_{CC} enables -ΔV and GND disables it. Switch SW1 controls discharge of battery A. HTF = 48°C, TCO = 48°C, and LTF = 10°C for the component values listed in Table 6 for RTB1, RBT2, R5, and R6 with a Philips thermistor (Part No. 2322-640-63103) with ΔT/Δt termination set for 1°C/minute at 30°C.

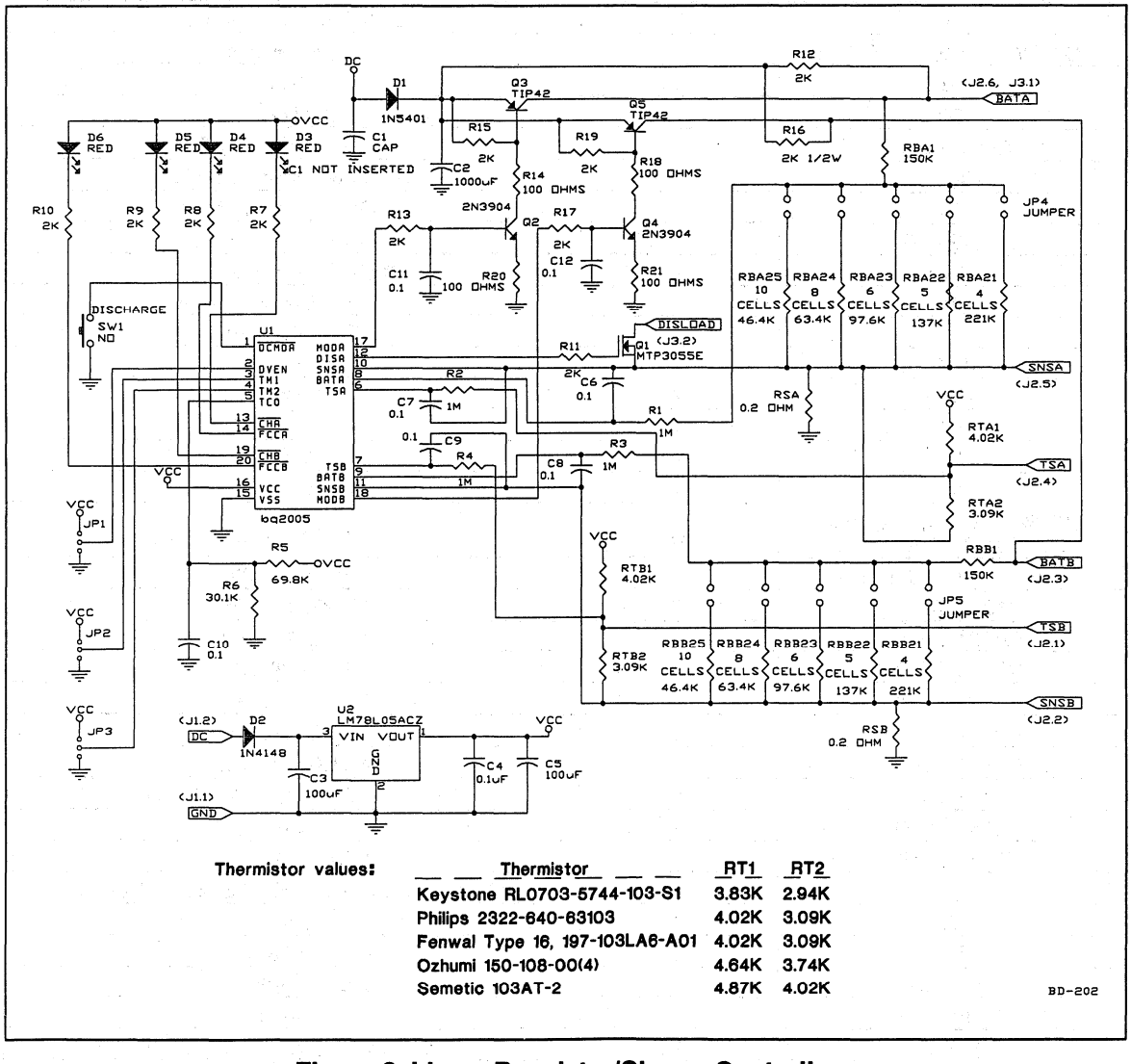
Safety time-out is selected by programming TM1 and TM2 with jumpers JP2 and JP3, respectively. To customize the design for a specific application, ensure that the power components are rated for the stresses they must handle. Charge current is a function of $RS_{A,B}$ and an internal bq2005 threshold:

$$I_{CHARGE} \approx \frac{0.225V}{RS_{A,B}}$$

The source power supply must provide sufficient voltage differential to the battery to account for losses in polarity protection diodes or resistive drops.

The selection of component values for R13, R17, C11, and C12 in this example affects the switching frequency of MOD and the delay to full current sense at the sense

pins of the bq2005. Although the effects on fast charge and top-off are minimal because the delay is small compared to the total time, the effect on pulse trickle charge is significant. Transistors Q2 and Q4 may not turn on in some cases, which may be advantageous if no trickle charge is desired.



Thermistor values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

BD-202

Figure 8. Linear Regulator/Charge Controller

Table 5. Linear Regulator/Charge Controller Board Parts List

Component Name	Quantity	Component Description
C1, C2	1	1000µF 25V aluminum (C1 is optional—not stuffed)
C3	1	100µF 25V aluminum
C5	1	100µF 6.3V aluminum
C4, C6, C7, C8, C9, C10, C11, C12	8	0.1µF ceramic
D1	1	1N5400
D2	1	1N4148
D3, D4, D5, D6	4	HMLP-D150 HP LED
J1, J3	2	2-position terminal block
J2	1	6-position terminal block
JP1, JP2, JP3	3	3-pin single-row header
JP4, JP5	2	12-pin dual-row header
JP6	1	2-pin single-row header
Q1	1	MTP3055EL FET
Q2, Q4	2	2N3904
Q3, Q5	2	TIP42
R1, R2, R3, R4	4	1MΩ 5% ¼W
R5	1	69.8KΩ 1% ¼W
R6	1	30.1KΩ 1% ¼W
R7, R8, R9, R10, R11, R12, R13, R15, R16, R17, R19	11	2KΩ 5% ¼W
R14, R18, R20, R21	2	100Ω 5% ¼W
RBA1, RBB1	2	150KΩ 1% ¼W
RBA21, RBB21	2	221KΩ 1% ¼W
RBA22, RBB22	2	137KΩ 1% ¼W
RBA23, RBB23	2	97.6KΩ 1% ¼W
RBA24, RBB24	2	63.4KΩ 1% ¼W
RBA25, RBB25	2	46.4KΩ 1% ¼W
RSA, RSB	2	0.2Ω 1% 3W wirewound Dale LVR3
RTA1, RTB1	2	4.02KΩ 1% ¼W
RTA2, RTB2	2	3.09KΩ 1% ¼W
S1	1	SPST momentary switch, Panasonic P8008S
U1	1	bq2005
U2	1	LM78L05ACZ
Heatsink	1	Thermalloy 6298B
Mounting kit	2	TO-220
Socket	1	20-pin solder tail ICO-203-58-T
PCB	1	DV2005L1
Screws	4	6-32 thread x ¼inch
Legs	4	Stand-off ½inch 6-32 thread

Application Example 2: Single-Magnetics Low-Cost Dual-Switching Charger

Figure 9 illustrates a low-cost dual-sequential switching charger using a small, low Q inductor to speed up the bipolar transistor commutation. Table 6 contains the parts list for the board. Bipolar transistors Q2 and Q5 are used to multiplex the energy stored in L1 by the charger's charge cycles.

Transistor Q3 is used to switch energy into L1 from the power source. Low-Q inductor L2 helps to turn Q3 off to limit its power dissipation. This circuit has the advantage of using bipolar transistors with saturation voltages far below the IR drops of comparably sized p-channel MOSFETs. This also results in significant cost savings. Designers must use care in selecting Q3 for suitability as a switching transistor. The Zetex Super-E line is ideal for applications up to 3A.

Layout guidelines are described on page 8. Possible layout concerns include:

- Diode D2 is installed to catch inductor energy in the event of battery removal during charge.
- Battery voltage differentials are applied to the base-emitter junctions of transistors Q5 and Q2 in the reverse direction. (Although the bq2005 will not charge a shorted battery, the design should ensure that Q5 and Q2 are protected if the battery could be shorted during charge.)

Q3 must be a high-speed switching transistor with suitably high V_{CE} rating for the application. The ZTX789A has a breakdown rating of 25V and a continuous current rating of 3A. This transistor's high gain enables it to saturate to a very low V_{CE} (< 0.25V) at 2A. The "on-time" power dissipation makes up most of the component power loss, but the switching loss must be added to give a complete picture of the transistor's required power dissipation.

A good switching transistor is gauged by its transition frequency (F_T) rating. A transistor with an F_T rating of >50MHz is a superior switching transistor for a switch-mode application, whereas a transistor with an F_T of 10MHz may be usable. In this example, the ZTX789A has an F_T of 100MHz. Manufacturers sometimes cite turnoff time as a sum of storage and fall time; some cite these values independently. The turnoff time is important for frequency selection, but the fall time is critical to determine power dissipation.

The influence of fall time on power dissipation can be estimated using the following formula:

$$P_{SW} = F \times T_F \times V_{IN} \times \frac{I_P}{6}$$

where:

P_{SW} = Power loss when switching

F = Switching frequency

T_F = Fall time

V_{IN} = Maximum input voltage

I_P = Peak switching current

Component power dissipation is the sum of P_{SW} and P_{ON}, which is estimated from the following formula:

$$P_{ON} = \frac{V_{BAT}}{V_{IN}} \times V_{CESAT} \times I_{AV}$$

where:

P_{ON} = Power dissipation when the transistor is on

V_{BAT} = Battery voltage

V_{IN} = Input voltage

V_{CESAT} = Maximum transistor saturation voltage

I_{AV} = Average battery charge current

The Zetex E-line package can dissipate the heat resulting from this design in free air.

Other switching transistors that may be useful in applications up to 3A are the MJE210 and the D45H series transistors. Q2 and Q5 are selected for high HFE and low V_{CESAT}.

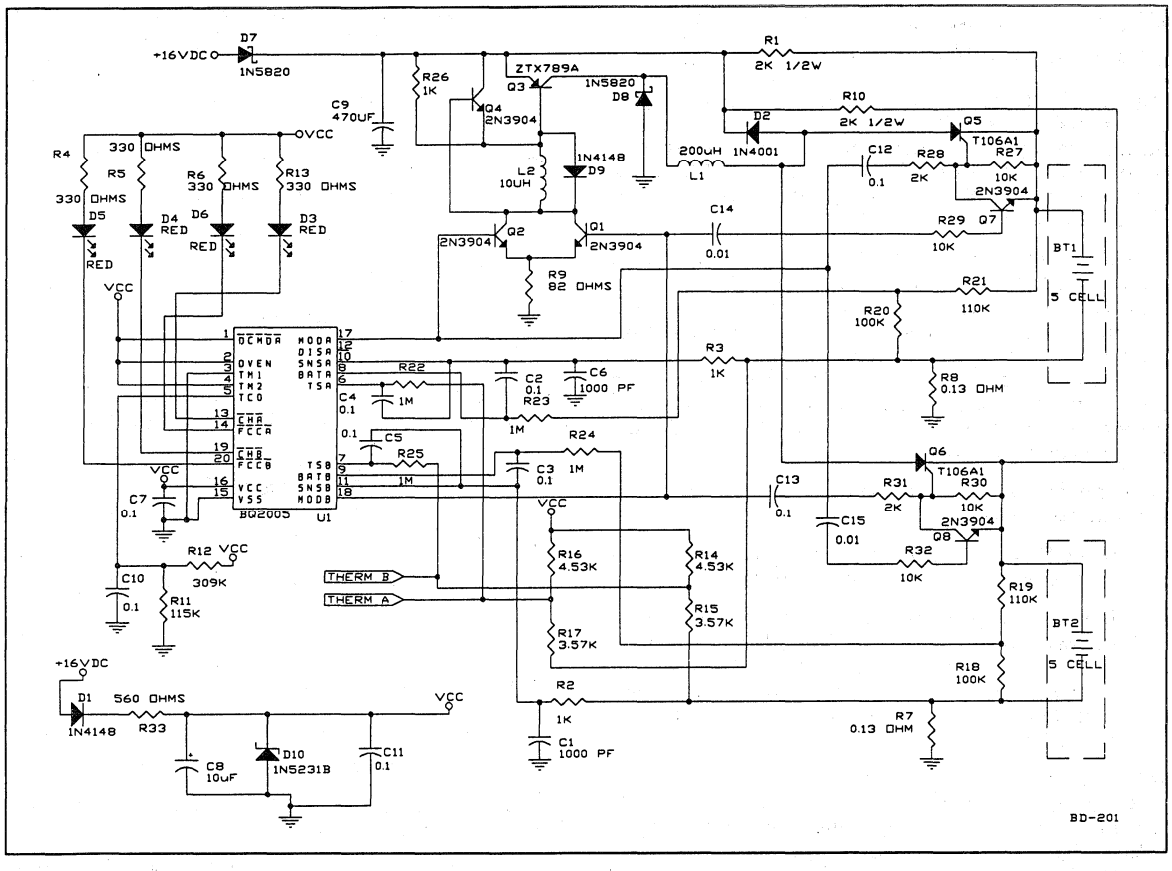


Figure 9. Single-Magnetics Low-Cost Dual-Switching Charger

Table 6. Single-Magnetics Low-Cost Dual-Switching Parts List

Component Name	Quantity	Component Description
C1, C6	2	1000pF 50V ceramic
C2, C3, C4, C5, C7, C10, C11, C12, C13	9	0.1µF 50V ceramic
C14, C15	2	0.01µF 50V ceramic
C8	1	10µF 35V aluminum
C9	1	470µF 35V aluminum
D1, D9	2	1N4148
D2	1	1N4001
D3, D4, D5, D6	4	HMLP-D150 red HP LED
D7, D8	2	1N5820 Schottky
D10	1	1N5231B Zener
L1	1	200µH toroid inductor
L2	1	10µH J.W. Miller 78F100J
Q1, Q2, Q4, Q7, Q8	5	2N3904
Q3	1	ZTX789A, Zetex high gain, med. power
Q5, Q6	2	T106A1, Teccor 4A SCR
R1, R10, R28, R31	4	2KΩ 5% ¼W carbon film
R2, R3, R26	3	1KΩ 5% ¼W carbon film
R4, R5, R6, R13	4	330Ω 5% ¼W carbon film
R7, R8	2	0.13Ω 5% 1W metal oxide
R9	1	82Ω 5% ¼W carbon film
R11	1	115KΩ 1% ¼W metal film
R12	1	309Ω 1% ¼W metal film
R14, R16	2	4.53KΩ 1% ¼W metal film
R15, R17	2	3.57KΩ 1% ¼W metal film
R18, R20	2	100KΩ 5% ¼W carbon film
R19, R21	2	110KΩ 5% ¼W carbon film
R22, R23, R24, R25	4	1MKΩ 5% ¼W carbon film
R27, R29, R30, R32	4	10KΩ 5% ¼W carbon film
R33	1	560Ω 5% ¼W carbon film
U1	1	bq2005

Application Example 3: P-Channel MOSFET Buck-Topology Switch-Mode Charger

In this example, the bq2005 is used to implement a switching regulator/charge controller that can charge 4 to 10 NiCd or NiMH cells with current regulated up to 3A.

Figure 10 is a standard configuration for a pFET switch-mode charger. MOD drives a small signal DMOS FET, Q2/Q5. When MOD is high, Q2/Q5 is on, turning on Q4/Q7 via the path through D8/D12 and D11/D7.

L1/L2 inductor current ramps up linearly while MOD is high. L1/L2 current is in series with the battery and RSA or RSB. The inductor current ramps up linearly until V_{SNS} reaches 0.250V, at which time MOD goes low and Q4/Q7 turns off. A flux reversal occurs in L1/L2, causing D9/D13 to conduct. Charge is now being transferred from L1/L2 into the battery. The L1/L2 current ramps down linearly until V_{SNS} reaches 0.20V. At this point the cycle repeats with MOD going high.

For input voltages that are higher than the rated Q4/Q7 safe operating gate voltage, Zener diode D7/D11 can be placed in series with the drain lead of Q2/Q5. The Zener voltage should be sized to allow full Q4/Q7 enhancement while Q2/Q5 is conducting. See Table 7.

Capacitor C2 is used to provide a low-impedance for the Q2/Q5 source lead. Without C2 in place, Q2/Q5 can be connected to an overly inductive voltage supply. D1 is a blocking diode that keeps the battery from discharging via U2 during removal of the DC power source input.

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection can be enabled (DVEN high), and discharge control is through $\overline{DCMD}$ (SW1 low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; ΔT/Δt at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and resistor R15/R17 are determined by the designer. RSA/RSB is selected such that I_{CHG} * RSA/RSB = 0.225V.

The values of RB1 and RB2 to complete this schematic may be selected from Table 3.

Note: Temperature control and qualification may be disabled by tying the TCO pin to V_{SS} and fixing the voltage on the $TS_{A,B}$ pins to 0.1 * V_{CC}.

Table 8 lists suggested components for different-rate chargers. Table 9 lists other components shown in Figure 10.

Table 7. Lookup Table for D7/D11 Selection

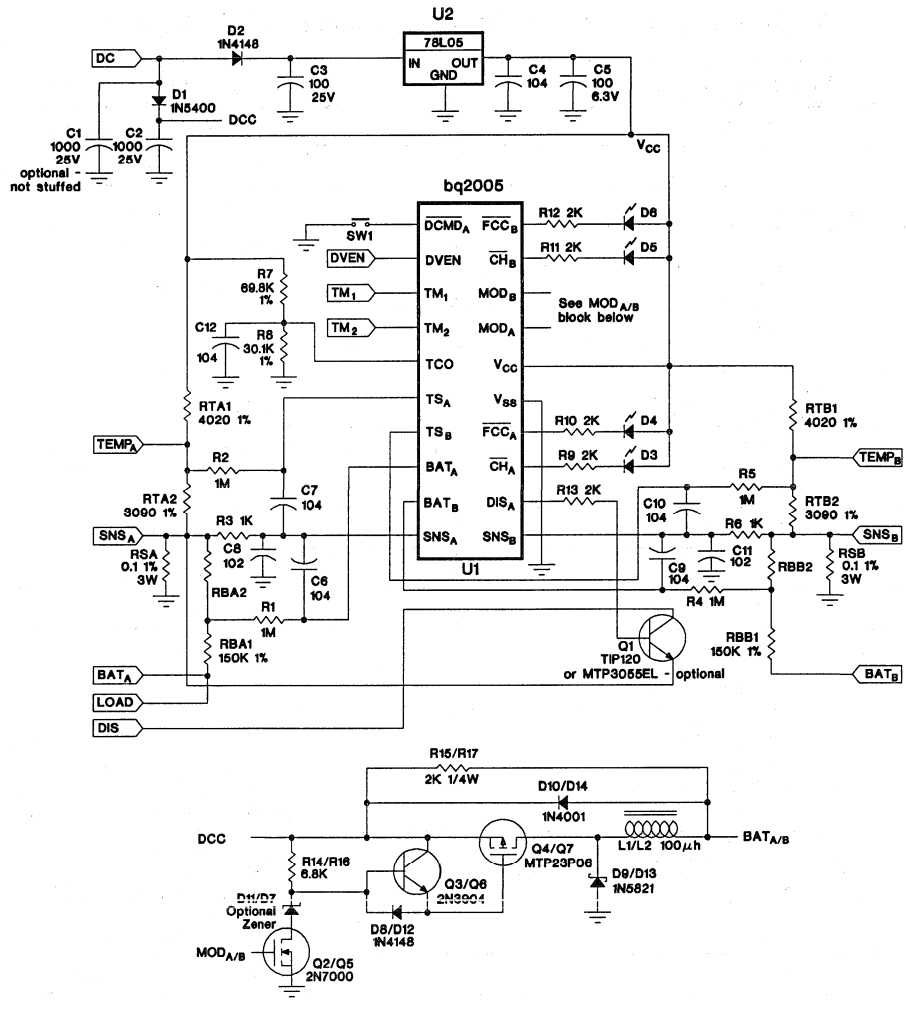
+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Table 8. Suggested Components—P-Channel MOSFET Charger

Suggested Max. Charging Current	Q4/Q7	D9/ D13	D10/ D14	L1/L2
1A	IRF9Z14	1N4001	1N5818	30 turns, #26 AWG, wound on Magnetics, Inc., P/N 77040 core; nominal inductance 59µH; GFS Mfg., Inc., P/N 92-2156-1
2A	IRF9Z24	1N5821	1N5821	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
3A	IRF9Z34	1N5821	1N5821	
Source	International Rectifier	Motorola	Motorola	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 9. Other Components—P-Channel MOSFET Charger

Component Name	Component Description
C1, C2	1000µF 5V electrolytic
C3	100µF 25V electrolytic
C4, C6, C7, C9, C10, C12	0.1µF ceramic
C5	100µF 6.3V electrolytic
C8, C11	1000pF ceramic
D1	1N5400
D2, D8, D12	1N4148
D3, D4, D5, D6	HLMP 4700 red LED
D7/D11	Optional Zener; see Table 9
D9/D13	1N5821
D10/D14	1N4001
Q1	TIP120 or MTP3055EL
Q2, Q5	2N7000
Q3, Q6	2N3904
Q4/Q7	MTP23P06
R1, R2, R4, R5	1MΩ 5% ¼W or ⅛W
R3, R6	1KΩ 5% ¼W
R7, R8	User-defined 1% ¼W or ⅛W
R9, R10, R11, R12, R13	2KΩ 5% ¼W or ⅛W
R14/R16	6.8KΩ 5% ¼W or ⅛W
RSA, RSB	0.1Ω 1% 3W
RBA1, RBB1	150KΩ 1% ¼W or ⅛W
RBA2, RBB2	User-defined 1% ¼W or ⅛W
RTA1, RTB1	User-defined 1% ¼W or ⅛W
RTA2, RTB2, R15, R17	User-defined 1% ¼W or ⅛W
L1/L2	See Table 10
U1	bq2005
U2	LM78L05ACZ



Thermistor values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

BD-184

Notes: All 104 capacitors are 0.1µF ceramic.
All 102 capacitors are 0.001µF ceramic.

Figure 10. P-Channel MOSFET Switching-Mode Charger

Appendix A
Determining Temperature-Control Component Values

The bq2005 uses a negative temperature coefficient (NTC) thermistor to determine temperature. The ΔT/Δt sensitivity can be adjusted using different resistor values (RT1 and RT2 in Figure 1 and the application example) and a different high-temperature cutoff voltage. Table A-1 lists various thermistor manufacturers, with the appropriate part numbers.

Follow these steps to determine temperature-control component values (see Figure 6):

1a. The low-temperature fault (LTF) limit for charging must be established. LTF for charging is determined by the battery specification and the charge rate used. A typical value for the low-temperature limit is 10°C.

b. V_{LTF} is set within the bq2005 at 0.4 * V_{CC}.

2a. The high-temperature cutoff (TCO) for charging must be established. TCO for charging is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical values range from 40°C to 50°C, although values outside this range may be applicable.

b. The average ΔT/Δt sensitivity from LTF to TCO ($T_{\Delta T}$, expressed as °C/minute) for termination must be established. As mentioned in this application note, the bq2005 provides a typical ΔT/Δt charge termination of 14 mV per minute. The $T_{\Delta T}$ value is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical nominal values for $T_{\Delta T}$ range from 0.75°C/min to 1.5°C/min.

Relative to the average value $T_{\Delta T}$, the minimum-to-maximum range of ΔT/Δt at a specific temperature depends on two parameters:

- The measurement resolution of the bq2005, which contributes a ± 25% error.
- The non-linearity of the thermistor between LTF and TCO. As the temperature nears LTF, the expected ΔT/Δt is less than $T_{\Delta T}$ (less sensitive), and as the temperature nears TCO, the expected ΔT/Δt is more than $T_{\Delta T}$ (more sensitive).

The ΔT/Δt range should be considered in determining the nominal $T_{\Delta T}$. Nominal $T_{\Delta T}$ should be selected so that its minimum value represents an acceptable (non-premature) termination threshold. Thus a first bq2005 sample does not cause a premature termination. Multiple sampling ensures that the termination occurs well before the $T_{\Delta T}$ max.

c. The high-temperature cutoff voltage, V_{TCO}, must be established. This V_{TCO} limit is determined by the $T_{\Delta T}$ and may be calculated by:

$$V_{TCO} = [\ (2 * V_{CC}/5) - (0.0028 * V_{CC} * (TCO - LTF))\ ] / T_{\Delta T}$$

V_{TCO} is provided at the TCO pin by a resistor-divider network as shown in Figures 8 and 9: $V_{TCO} = V_{CC} * R1/(R1 + R2)$.

4. Select the thermistor to be used. If it is not from Table A-1, the thermistor sensitivity at 25°C should be at least -4% and the ΔR steps between 30°C and 50°C should be comparable to or greater than those in Table A-1 to obtain the appropriate accuracy. Lower values affect the linearity of the ΔT/Δt.

5. Determine the thermistor resistance at LTF and TCO (R_{LTF} and R_{TCO}, respectively). This may be done using the thermistor temperature versus resistance conversion table provided with the thermistor specification. These tables are usually in 5°C increments.

6. The values for RT1 and RT2 may be calculated by:

$$T1 = R_{LTF} * (1 - (2/V_{CC}))/(2/V_{CC})$$

$$T2 = R_{TCO} * (1 - (V_{TCO}/(V_{CC} - V_{SNS})))/(V_{TCO}/(V_{CC} - V_{SNS}))$$

$$RT2 = ((T2 * R_{LTF}) - (T1 * R_{TCO}))/(T1 - T2)$$

$$RT1 = (RT2 * T1)/(R_{LTF} + RT2)$$

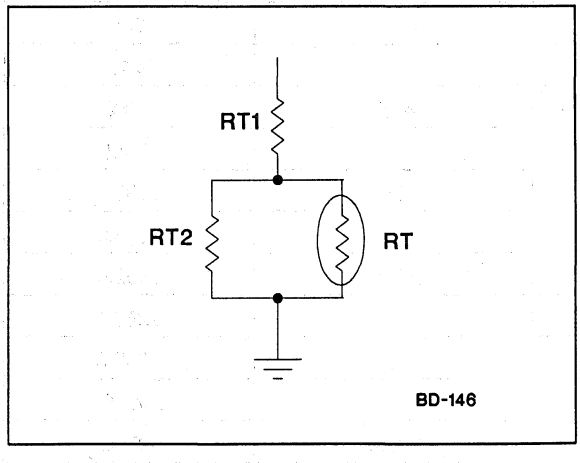


Figure A-1. Resistor Network

Table A-1. 10K NTC Thermistor Types and Resistance Values

Temperature (°C)	Nominal Resistance (Ω) at Temperature			
	Keystone Carbon Co. RL0703-5744-103-S1 (Tel: 814/781-1591)	Philips Components 2322-640-63103 (Tel: 407/743-2112)	Fenwal Electronics Type 16; 197-103LA6-A01 (Tel: 508/478-6000)	Thermometrics C100Y103J (Tel: 908/287-2870)
-30	188172	173900	177000	-
-25	138043	128500	-	-
-20	102263	95890	97070	-
-15	76461	72230	-	-
-10	57672	54890	55330	-
-5	43864	42070	-	-
0	33630	32510	32650	29588
5	25988	25310	-	23515
10	20243	19860	19900	18813
15	15889	15690	-	15148
20	12562	12490	12490	12271
25	10000	10000	10000	10000
30	8013	8060	8057	8195
35	6461	6536	-	6752
40	5241	5331	5327	5593
45	4276	4373	-	4656
50	3507	3606	3603	3894
55	2894	2989	-	3273
60	2400	2490	2488	2762
65	2001	2085	-	2342
70	1677	1753	1752	1993.7
75	1412	1481	-	1704.0
80	1194	1256	1258	1462.0
85	1014	1070	-	1259.1
90	865.2	915.5	917.7	1088.3
95	741.0	786.1	-	943.9
100	636.9	677.5	680.0	821.4

Fast Charge IC

Features

- ➤ Fast charging and conditioning of NiCd and NiMH batteries
  - Precise charging independent of battery pack number of cells
  - Discharge-before-charge on demand
  - Pulse trickle charge conditioning
  - Battery undervoltage and overvoltage protection
- ➤ Built-in 10-step voltage-based charge status monitoring
  - Charge status display options include seven-segment monotonic bargraph and fully decoded BCD digit
  - Display interface options for direct drive of LCD or LED segments
  - Charger state status indicators for pending, discharge, charge, completion, and fault
  - Audible alarm for charge completion and fault conditions
- ➤ Charge control flexibility
  - Fast or Standard speed charging
  - Top-off mode for NiMH
  - Charge rates from 0/8 to 2C (30 minutes to 8 hours)
- ➤ Charge termination by:
  - Negative delta voltage (-ΔV)
  - Peak voltage detect (PVD)
  - Maximum voltage
  - Maximum time
  - Maximum temperature
- ➤ High-efficiency switch-mode design
  - Ideal for small heat-sensitive enclosures
- ➤ 24-pin, 300-mil SOIC or DIP

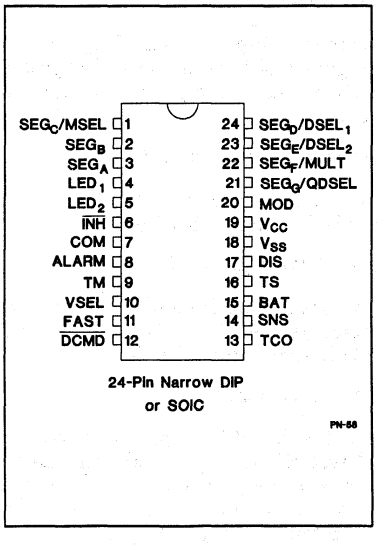
General Description

The bq2007 is a highly integrated monolithic CMOS IC designed to provide the intelligent battery charging and charge status monitoring required for stand-alone charge systems.

The bq2007 offers flexibility by providing a wide variety of charge status display formats. The bq2007 internal charge status monitor can be configured to support up to a seven-segment bargraph or a single BCD digit display. The bargraph display indicates up to seven monotonic steps, whereas the BCD digit counts in ten steps of 10% increments. The bq2007 output drivers can direct-drive either LCD or LED interface levels.

Charge action begins by either application of the charging supply or replacement of the battery pack. For safety, charging is inhibited until prequalification of battery temperature and voltage is within configured charge limits.

Pin Connections



Pin Names

SEGC/ MSEL	Display output segment C/ driver mode select
SEGB	Display output segment B
SEGA	Display output segment A
LED1	Charge status output 1
LED2	Charge status output 2
$\overline{INH}$	Charge inhibit input
COM	Common LED/LCD output
ALARM	Audio alarm output
TM	Timer mode select
VSEL	Voltage termination select
FAST	Fast charge rate select
$\overline{DCMD}$	Discharge command
TCO	Temperature cutoff
SNS	Sense resistor input
BAT	Battery voltage
TS	Temperature sense
DIS	Discharge control
VSS	System ground
VCC	5.0V ±10% power
MOD	Modulation control
SEGG/ QDSEL	Display output segment G/ charge status display select
SEGF/ MULT	Display output segment F/ multi-cell pack select
SEGE/ DSEL2	Display output segment E/ display select 2
SEGD/ DSEL1	Display output segment D/ display select 1

The acceptable battery temperature range is set by an internal low-temperature threshold and an external high-temperature cutoff threshold. The absolute temperature is monitored as a voltage on the TS pin with the external thermistor network shown in Figure 2.

The bq2007 provides for undervoltage battery protection from high-current charging if the battery voltage is less than the normal end-of-discharge value. In the case of a deeply discharged battery, the bq2007 enters the charge-pending state and attempts trickle-current conditioning of the battery until the voltage increases. Should the battery voltage fail to increase above the discharge value during the undervoltage time-out period, a fault condition is indicated.

Discharge-before-charge may be selected to automatically discharge the battery pack on battery insertion or with a push-button switch. Discharge-before-charge on demand provides conditioning services that are useful to correct or prevent the NiCd voltage depression, or "memory" effect, and also provide a zero capacity reference for accurate capacity monitoring.

After prequalification and any required discharge-before-charge operations, charge action begins until one of the full-charge termination conditions is detected. The bq2007 terminates charging by any of the following methods:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum absolute temperature
- Maximum battery voltage
- Maximum charge time-out

The bq2007 may be programmed for negative delta voltage (-ΔV) or peak voltage detect (PVD) charge termination algorithms. The VSEL input pin selects -ΔV or PVD termination to match the charge rate and battery characteristics.

To provide maximum safety for battery and system, charging terminates based on maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), and maximum time-out (MTO). The TCO threshold is the maximum battery temperature limit for charging. TCO terminates charge action when the temperature sense input voltage on the TS pin drops below the TCO pin voltage threshold. MCV provides battery overvoltage protection by detecting when the battery cell voltage (V_{CELL}) exceeds the V_{MCV} value and terminates fast charge, standard charge, or top-off charge. The maximum time-out (MTO) termination occurs when the charger safety timer has completed during the active charge state.

The bq2007 indicates charge state status with an audio alarm output option and two dedicated output pins with programmable display options. The $DSEL_{1-2}$ inputs can select one of the three display modes for the LED_{1-2} outputs.

Charger status is indicated for:

- Charge pending
- Charge in progress
- Charge complete
- Fault condition

Pin Descriptions

SEG_{A-G} Display output segments A–G

State-of-charge monitoring outputs. QDSEL input selects the bargraph or BCD digit display mode. See Table 3.

MSEL Display driver mode select

Soft-programmed input selects LED or LCD driver configuration at initialization. When MSEL is pulled up to V_{CC}, outputs SEG_{A-G} are LED interface levels; when MSEL is pulled down to V_{SS}, outputs SEG_{A-G} are LCD levels.

$DSEL_1$, $DSEL_2$ Display mode select 1-2

Soft-programmed inputs control the LED_{1-2} charger status display modes at initialization. See Table 2.

MULT Fixed-cell pack select

Soft-programmed input is pulled up to V_{CC} when charging multi-cell packs and is pulled down to V_{SS} for charging packs with a fixed number of cells.

QDSEL State-of-charge display select

The QDSEL input controls the SEG_{A-G} state-of-charge display modes. See Table 3.

LED_{1-2} Charger status outputs 1-2

Charger status output drivers for direct drive of LED displays. Display modes are selected by the DSEL input. See Table 2.

$\overline{INH}$ Charge inhibit input

When low, the bq2007 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a charge cycle is initiated. See page 10 for details.

COM **Common LCD/LED output**

Common output for LCD/LED display SEG_{A-G}. Output is high-impedance during initialization to allow reading of soft-programmed inputs $DSEL_1$, $DSEL_2$, MSEL, MULT, and QDSEL.

ALARM **Audio output**

Audio alarm output.

TM **Timer mode select**

TM is a three-level input that controls the settings for charge control functions. See Table 4.

VSEL **Voltage termination select**

This input switches the voltage detect sensitivity. See Table 5.

FAST **Fast charge rate select**

The FAST input switches between Fast and Standard charge rates. See Table 5.

$\overline{DCMD}$ **Discharge command**

The $\overline{DCMD}$ input controls the discharge-before-charge function. A negative-going pulse initiates a discharge action. If $\overline{DCMD}$ is connected to V_{SS}, automatic discharge-before-charge is enabled. See Figure 3.

TCO **Temperature cut-off threshold input**

Minimum allowable battery temperature-sensor voltage. If the potential between TS and SNS is less than the voltage at the TCO input, then any fast charging or top-off charging is terminated.

SNS **Sense resistor input**

SNS controls the switching of MOD output based on an external sense resistor. This provides the lower reference potential for the BAT pin.

BAT **Battery voltage input**

Battery voltage sense input for the battery pack being charged. This resistor divider network is connected between the positive and the negative terminals of the battery. See Figure 1.

TS **Temperature sense input**

Input for battery temperature monitoring negative temperature coefficient (NTC) thermistor.

DIS **Discharge control**

DIS is a push-pull output that controls an external transistor to discharge the battery before charging.

V_{SS} **Ground**

V_{CC} **V_{CC} supply input**

MOD **Current-switching control output**

Push/pull output that controls the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

Functional Description

Figure 1 illustrates charge control and display status during a bq2007 charge cycle. Table 1 summarizes the bq2007 operational features. The charge action states and control outputs are given for possible input conditions.

Charge Action Control

The bq2007 charge action is controlled by input pins $\overline{DCMD}$, VSEL, FAST, and TM. When charge action is initiated, the bq2007 enters the charge-pending state, checks for acceptable battery voltage and temperature, and performs any required discharge-before-charge operations. $\overline{DCMD}$ controls the discharge-before-charge function, and VSEL, FAST, and TM select the charger configuration. See Tables 4 and 5.

During charging, the bq2007 continuously tests for charge termination conditions: negative delta voltage, peak voltage detection, maximum time-out, battery overvoltage, and high-temperature cutoff. When the charge state is terminated, a trickle charge continues to compensate for self-discharge and maintain the fully charged condition.

Charge Status Indication

Table 2 summarizes the bq2007 charge status display indications. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED_2.

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system. LED_2 indicates the precharge

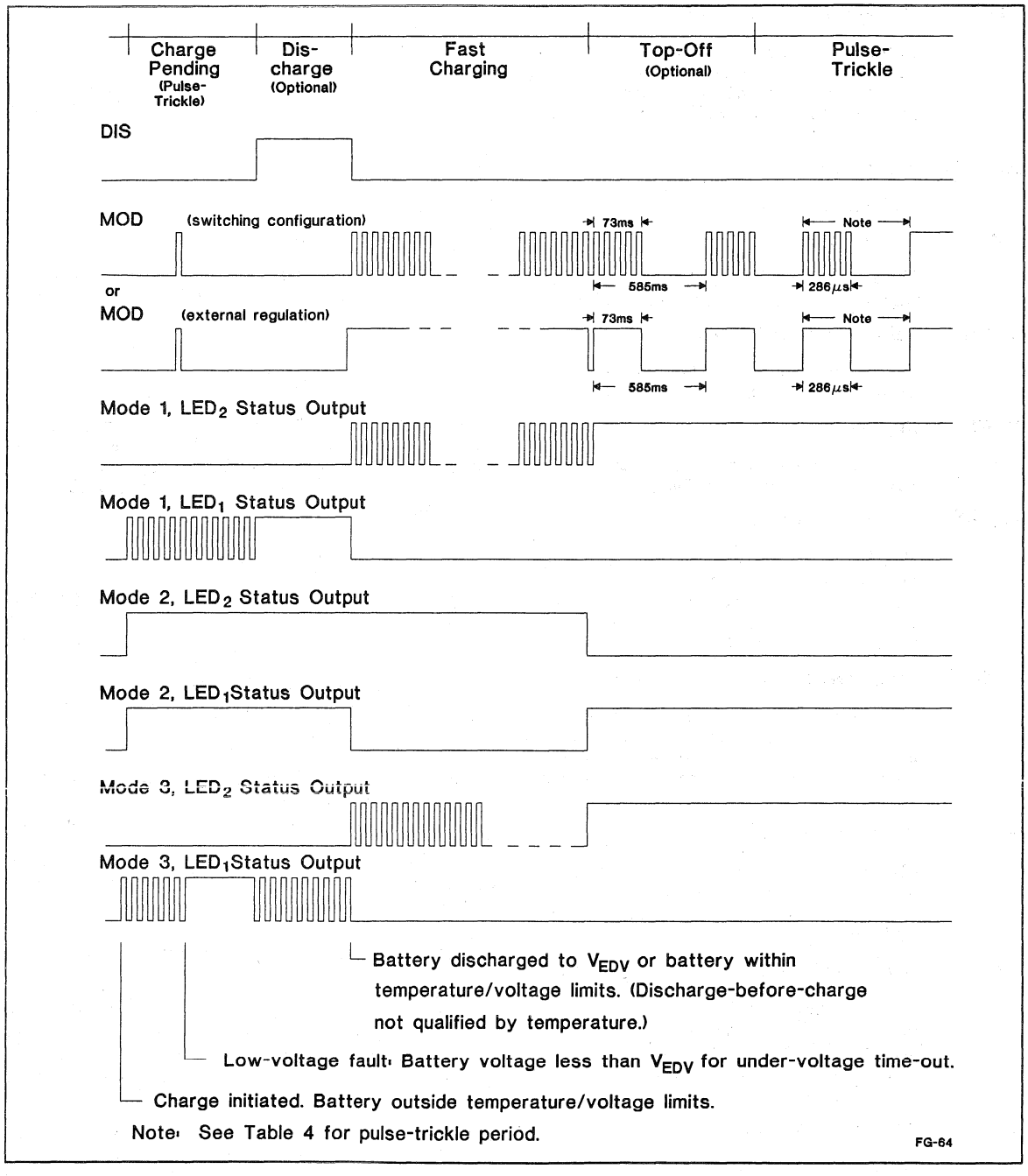


Figure 1. Example Charging Action Events

status (i.e., charge pending and discharge) and LED_1 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode is for implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} allows for fault status information to be displayed.

Audio Output Alarm

The bq2007 audio alarm output generates an audio tone to indicate a charge completion or fault condition. The audio alarm output is a symmetrical duty-cycle AC signal that is compatible with standard piezoelectric alarm elements. A valid battery insertion is indicated by a single high-tone beep of ½-second typical duration. The charge completion and fault conditions are indicated by a 9.5- to 15-second high-tone sequence of ½-second typical duration at a 2-second typical repetition rate.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT soft-programmed input pin.

When MULT is pulled down to V_{SS}, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to 1/64 to 1/32 of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

Table 1. bq2007 Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output
Battery absent	V_{CC} applied and $V_{CELL} \geq V_{MCV}$	Trickle charge per Table 4	Low
Charge initiation	V_{CC} applied or V_{CELL} drops from $\geq V_{MCV}$ to $< V_{MCV}$	-	Low
Discharge-before-charge	$\overline{DCMD}$ high-to-low transition or to V_{SS} on charge initiation and $V_{EDV} < V_{CELL} < V_{MCV}$	Low	High
Charge pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{TCO}$ or $V_{CELL} < V_{EDV}$	Trickle charge per Table 4	Low
Fast charging	Charge pending complete and FAST = V_{CC}	Low if $V_{SNS} > 250mV$; high if $V_{SNS} < 200mV$	Low
Standard charging	Charge pending complete and FAST = V_{SS}	Low if $V_{SNS} > 250mV$; high if $V_{SNS} < 200mV$	Low
Charge complete	$-\Delta V$ termination or $V_{TEMP} < V_{TCO}$ or PVD ≥ 0 to -3mV/cell or maximum time-out or $V_{CELL} > V_{MCV}$	-	-
Top-off pending	VSEL = V_{CC}, charge complete and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{TCO}$ or $V_{CELL} < V_{EDV}$	Trickle charge per Table 4	Low
Top-off charging	VSEL = V_{CC} and charge complete and time-out not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} for 73ms of every 585ms	Low
Trickle charging	Charge complete and top-off disabled or top-off complete or pending	Trickle charge per Table 4	Low
Fault	Charge pending state and charge pending time-out (t_{PEND}) complete	Trickle charge per Table 4	Low

Definitions: $V_{CELL} = V_{BAT} - V_{SNS}$; $V_{MCV} = 0.8 * V_{CC}$; $V_{EDV} = 0.262 * V_{CC}$ or $0.4 * V_{CC}$; $V_{TEMP} = V_{TS} - V_{SNS}$; $V_{LTF} = 0.5 * V_{CC}$.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays 1/32 of the charge safety timer as a percentage of full charge. This method is recommended over the voltage-based method when charging fixed-cell packs where the battery terminal voltages can vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged. When using the timer-based method, discharge-before-charge is recommended.

During discharge and when MULT is pulled down to V_{SS}, the charge status monitor indicates a percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. When V_{BAT} is greater than V_{80}, V_{60}, V_{40}, or V_{20}, the BCD digit format displays the 90%, 70%, 50%, and 30% respective charge indications. The discharge thresholds V_{80}, V_{60}, V_{40}, or V_{20} in bargraph format are indicated by the 90%, 60%, 40%, or 30% respective charge indications.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor BCD format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 3. The display modes are a seven-segment monotonic bargraph or a seven-segment BCD single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single BCD digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment charge status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments.

The BCD display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a BCD zero count at charge initiation to a BCD nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Table 3.

Table 2. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Display Driver Modes

The bq2007 is designed to interface with LCD or LED type displays. The LED signal levels are driven when the MSEL soft-programmed input is pulled to V_{CC} at initialization. The output pin COM is the common anode connection for LED SEG_{A-G}.

The LCD interface mode is enabled when the MSEL soft-programmed input pin is pulled to V_{SS} at initialization. An internal oscillator generates all the timing signals required for the LCD interface. The output pin COM is the common connection for static direct-driving of the LCD display backplane and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins is driven with the correct-phase AC signal to activate the LCD segment. In bargraph or BCD mode, output pins SEG_{A-G} interface to LED or LCD segments.

Battery Voltage and Temperature Measurement

The battery voltage and temperature are monitored within set minimum and maximum limits. When MULT is pulled up to V_{CC}, battery voltage is sensed at the BAT pin by a resistive voltage divider that divides the terminal voltage between 0.262 * V_{CC} (V_{EDV}) and 0.8 * V_{CC} (V_{MCV}). The bq2007 charges multi-cell battery packs from a minimum of N cells, to a maximum of 1.5 * N cells. The battery voltage divider is set to the minimum cell battery pack (N) by the BAT pin voltage divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1.33}\right) - 1$$

When MULT is pulled down to V_{SS}, tighter charge voltage limits and voltage-based charge status display are selected. This is recommended for charging packs with a fixed number of cells where the battery voltage divider range is between 0.4 * V_{CC} (V_{EDV}) and 0.8 * V_{CC}

Table 3. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

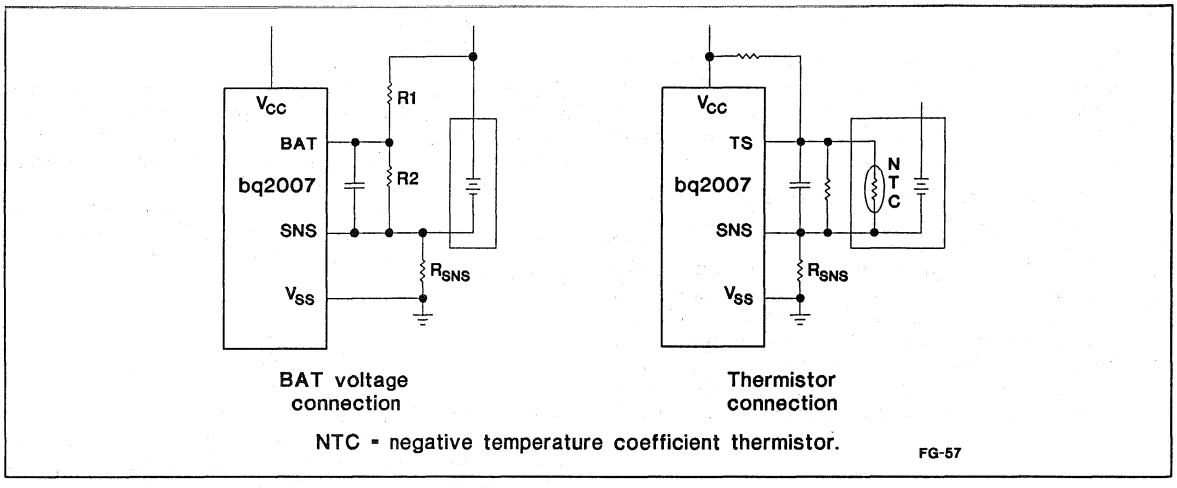


Figure 2. Voltage and Temperature Limit Measurement

(V_{MCV}). The bq2007 charges fixed-cell battery packs of N cells. The battery voltage divider is set by the divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{2}\right) - 1$$

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2007.

When battery temperature is monitored for maximum and minimum allowable limits, the bq2007 requires that the thermistor used for temperature measurement have a negative temperature coefficient. See Figure 2.

Temperature and Voltage Prequalifications

For charging to be initiated, the battery temperature must fall within predetermined acceptable limits. The voltage on the TS pin (V_{TS}) is compared to an internal low-temperature fault threshold (V_{LTF}) of (0.5 * V_{CC}) and the high temperature cutoff voltage (V_{TCO}) on the TCO pin. For charging to be initiated, V_{TS} must be less than V_{LTF} and greater than V_{TCO}. Since V_{TS} decreases as temperature increases, the TCO threshold should be selected to be lower than 0.5 * V_{CC} for proper operation. If the battery temperature is outside these limits, the bq2007 holds the charge-pending state with a pulse trickle current until the temperature is within limits. Temperature prequalification and termination is disabled if V_{TS} is greater than 0.8 * V_{CC}. See Figure 2.

The bq2007 provides undervoltage battery protection by trickle-current conditioning of a battery that is below the low-voltage threshold (V_{EDV}). The battery voltage (V_{CELL}) is compared to the low-voltage threshold (V_{EDV}) and charge will be inhibited if $V_{CELL} < V_{EDV}$. The condition trickle current and fault time-out are a percentage of the fast charge rate and maximum time-out (MTO).

Initiating Charge Action and Discharge-Before-Charge

A charge action is initiated under control of: (1) battery insertion or (2) power applied. Battery insertion is detected when the voltage at the BAT pin falls from above V_{MCV} to below V_{MCV}. Power applied is detected by the rising edge of V_{CC} when a battery is inserted.

Discharge-before-charge is initiated automatically on application of power or battery insertion when $\overline{DCMD}$ is connected to V_{SS}. Discharge-on-demand is initiated by a

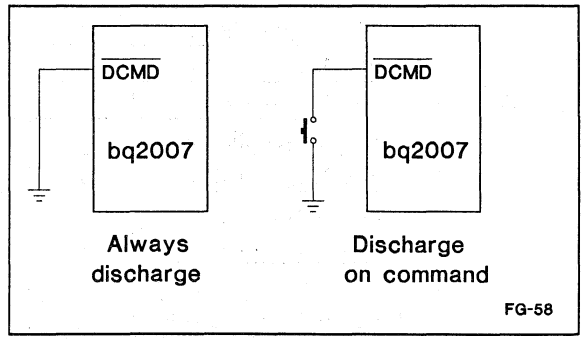


Figure 3. Discharge-Before-Charge

Table 4. bq2007 Charge Action Control Summary

FAST Input State	TM Input State	Time-out Period (min)	MOD Duty Cycle	Hold-off period (sec)	Trickle Rep Rate -ΔV C/32	Trickle Rep Rate PVD C/64
Vss	Float	640 (C/8)	25%	2400	219Hz	109Hz
Vss	Vss	320 (C/4)	25%	1200	109Hz	55Hz
Vss	Vcc	160 (C/2)	25%	600	55Hz	27Hz
Vcc	Float	160 (C/2)	100%	600	219Hz	109Hz
Vcc	Vss	80 (C)	100%	300	109Hz	55Hz
Vcc	Vcc	40 (2C)	100%	150	55Hz	27Hz

negative-going pulse on the $\overline{DCMD}$ pin regardless of charging activity. The $\overline{DCMD}$ pin is internally pulled up to Vcc; therefore, not connecting this pin results in disabling the discharge-before-charge function. See Figure 3. When the discharge begins, the DIS output goes high to activate an external transistor that connects a load to the battery. The bq2007 terminates discharge-before-charge by detecting when the battery cell voltage is less than or equal to the end-of-discharge voltage (V_{EDV}).

Charge State Actions

Once the required discharge is completed and temperature and voltage prequalifications are met, the charge state is initiated. The charge state is configured by the VSEL, FAST, and TM input pins. The FAST input selects between Fast and Standard charge rates. The Standard charge rate is ¼ of the Fast charge rate, which is accomplished by disabling the regulator for a period of 286µs of every 1144µs (25% duty cycle). In addition to throttling back the charge current, time-out and hold-off safety time are increased accordingly. See Table 4.

The VSEL input selects the voltage termination method. The termination mode sets the top-off state and trickle charge current rates. The TM input selects the Fast charge rate, the Standard rate, and the corresponding charge times. Once charging begins at the Fast or Standard rate, it continues until terminated by any of the following conditions:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum temperature cutoff (TCO)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

Voltage Termination Hold-off

To prevent early termination due to an initial false peak battery voltage, the -ΔV and PVD terminations are disabled during a short "hold-off" period at the start of charge. During the hold-off period when fast charge is selected (FAST = 1), the bq2007 will top off charge to prevent excessive overcharging of a fully charged battery. Once past the initial charge hold-off time, the termination is enabled. TCO and MCV terminations are not affected by the hold-off time.

-ΔV or PVD Termination

Table 5 summarizes the two modes for full-charge voltage termination detection. When VSEL = Vss, negative delta voltage detection occurs when the voltage seen on the BAT pin falls 12mV typical per cell below the maximum sampled value. VSEL = Vcc selects peak voltage detect termination and the top-off charge state. PVD termination occurs when the BAT pin voltage falls between 4mV and 6mV per cell below the maximum sampled value. When charging a battery pack with a fixed number of cells, the battery voltage divider can be set to sense two cells; thus the -ΔV and PVD termination thresholds are -6mV and 0 to -3mV, respectively. The valid battery voltage range on V_{BAT} for -ΔV or PVD termination is from 0.262 * Vcc to 0.8 * Vcc.

Table 5. VSEL Configuration

VSEL	Detection Method	Top-Off	Pulse Trickle Rate
Vss	-ΔV	Disabled	C/32
Vcc	PVD	Enabled	C/64

Maximum Temperature, Maximum Voltage, and Maximum Time Safety Terminations

The bq2007 also terminates charge action for maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), and maximum time-out (MTO). Temperature is monitored as a voltage on the TS pin (V_{TS}), which is compared to an internal high-temperature cutoff threshold of V_{TCO}. The TCO reference level provides the maximum limit for battery temperature during charging. MCV termination occurs when $V_{CELL} > V_{MCV}$. The maximum time-out (MTO) termination is when the charger safety timer countdown has completed during the active charge state. If the MTO, MCV, or TCO limit is exceeded during Fast charge, Standard charge, or top-off states, charge action is terminated.

Top-Off and Pulse Trickle Charging

The bq2007 provides a post-detection timed charge capability called top-off to accommodate battery chemistries that may have a tendency to terminate charge prior to achieving full capacity. When VSEL = V_{CC}, the top-off state is selected; charging continues after Fast charge termination for a period equal to the time-out value. In top-off mode, the Fast charge control cycle is modified so that MOD is activated for a pulse output of 73ms of every 585ms. This results in a rate 1/8 that of the Fast charge rate. Top-off charge is terminated by maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), or maximum time-out termination.

Pulse trickle is used to compensate for self-discharge while the battery is idle and to condition a depleted low-voltage battery to a valid voltage prior to high-current charging. The battery is pulse trickle charged when Fast, Standard, or top-off charge is not active. The MOD output is active for a period of 286µs of a period specified in Table 4. This results in a trickle rate of C/64 for PVD and C/32 when -ΔV is enabled.

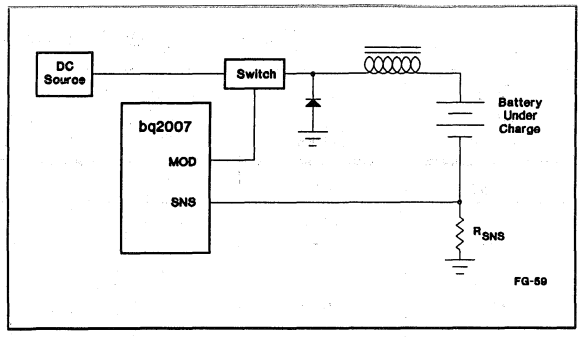


Figure 4. Constant-Current Switching Regulation

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2007 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Charge Current Control

The bq2007 controls charge current through the MOD output pin. In a frequency-modulated buck regulator configuration, the control loop senses the voltage at the SNS pin and regulates to maintain it between 0.04 * V_{CC} and 0.05 * V_{CC}. The nominal regulated current is I_{REG} = 0.225V/R_{SNS}. See Figure 4.

MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.04 * V_{CC} nominal), the MOD output is switched high to gate charge current through the inductor to the battery. When the SNS voltage is greater than V_{SNSHI} (0.05 * V_{CC} nominal), the MOD output is switched low-shutting off charge current from the supply. The MOD pin can be used to gate an external charging current source. When an external current source is used, no sense resistor is required, and the SNS pin is connected to V_{SS}.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ± 10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±25	mV	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	V_{SNSHI} - (0.01 * V_{CC})	±10	mV	
V_{LTF}	TS pin low-temperature threshold	0.5 * V_{CC}	±30	mV	SNS = 0V
V_{HTF}	TS pin high-temperature threshold	V_{TCO}	±30	mV	SNS = 0V
V_{EDV}	End-of-discharge voltage MULT is pulled up to V_{CC}	0.262 * V_{CC}	±30	mV	SNS = 0V
	End-of-discharge voltage MULT is pulled down to V_{SS}	0.4 * V_{CC}	±30	mV	SNS = 0V
V_{MCV}	BAT pin maximum cell voltage threshold	0.8 * V_{CC}	±30	mV	SNS = 0V
V_{20}	20% state-of-charge voltage threshold at the BAT pin	187/320 * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{40}	40% state-of-charge voltage threshold at the BAT pin	191/320 * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{60}	60% state-of-charge voltage threshold at the BAT pin	195/320 * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{80}	80% state-of-charge voltage threshold at the BAT pin	203/320 * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{20}	20% state-of-charge voltage threshold at the BAT pin	158/320 * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1
V_{40}	40% state-of-charge voltage threshold at the BAT pin	163/320 * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1
V_{60}	60% state-of-charge voltage threshold at the BAT pin	167/320 * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1
V_{80}	80% state-of-charge voltage threshold at the BAT pin	171/320 * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	10%
V_{BAT}	Voltage on BAT pin	0	-	V_{CC}	V	
V_{TS}	Voltage on TS pin	0	-	V_{CC}	V	Thermistor input
V_{TCO}	Temperature cutoff on TCO	0	-	0.5 * V_{CC}	V	Note 2
V_{CELL}	Battery voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{TEMP}	Voltage potential on TS	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}$, FAST, VSEL, $\overline{INH}$
	Tri-level input high	V_{CC} - 0.3	-	-	V	TM
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}$, FAST, VSEL, $\overline{INH}$
	Tri-level input low	-	-	0.3	V	TM
V_{OH}	Logic output high	V_{CC} - 0.8	-	-	V	DIS, LED_{1-2}, SEG_{A-G} @ I_{OH} = -10mA; MOD @ I_{OH} = -5mA
V_{OL}	Logic output low	-	-	0.8	V	DIS, LED_{1-2}, SEG_{A-G} @ I_{OL} = 10mA; MOD @ I_{OL} = 5mA
V_{OHCOM}	COM output	V_{CC} - 0.8	-	-	V	@ I_{OHCOM} = -40mA
I_{OHCOM}	COM source	-40	-	-	mA	@ V_{OHCOM} = V_{CC} - 0.8V
I_{CC}	Supply current	-	1	2.5	mA	No output load
I_{OH}	DIS, LED_{1-2}, SEG_{A-G} source	-10	-	-	mA	@V_{OH} = V_{CC} - 0.8V
I_{OH}	MOD	-5	-	-	mA	@V_{OH} = V_{CC} - 0.8V
I_{OL}	DIS, LED_{1-2}, SEG_{A-G} sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_{OL}	MOD	5	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_{IZ}	Tri-state inputs floating for Z state	-2.0	-	2.0	µA	TM
I_L	Input leakage	-	-	±1	µA	$\overline{INH}$, VSEL, V = V_{SS} to V_{CC}
	Input leakage	50	-	400	µA	$\overline{DCMD}$, FAST, V = V_{SS} to V_{CC}
I_{IL}	Logic input low current	-	-	70	µA	TM, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high current	-70	-	-	µA	TM, V = V_{CC} - 0.3V to V_{CC}

Notes:
1. V_{CELL} - V_{BAT} - V_{SNS}, V_{TEMP} - V_{TS} - V_{SNS}.
2. Invalid operating condition for $V_{TCO} \geq 0.5 * V_{CC}$.

Impedance

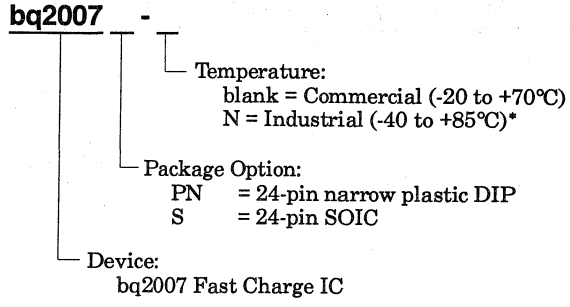
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_I	DC input impedance: pins TS, BAT, SNS, TCO	50	-	-	MΩ	
R_{PROG}	Soft-programmed pull-up resistor	150	-	200	KΩ	MSEL, $DSEL_1$, $DSEL_2$, MULT, QDSEL; resistor value ± 10% tolerance
R_{FLT}	Float state external resistor	-	5	-	MΩ	TM

Timing (TA = 0 to +70°C; VCC ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Deviation of fast charge safety time-out	0.84	1.0	1.16	-	At V_{CC} = ±10%, T_A = 0 to 60°C; see Table 3
t_{REG}	MOD output regulation frequency	-	-	300	kHz	Typical regulation range; V_{CC} = 5.0V
t_{PEND}	Charge pending time-out	-	25	-	%	Ratio of fast charge time-out; see Table 4.
F_{COM}	Common LCD backplane frequency	-	73	-	Hz	LCD segment frame rate
F_{ALARM}	Alarm frequency output	-	3500	-	kHz	High tone
t_{PW}	Pulse width for $\overline{DCMD}$ pulse command acknowledge	1	-	-	µs	Signal valid time
t_{MCV}	Valid period for $V_{CELL} > V_{MCV}$	0.5	-	1	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV} during charge or top-off, then a transition is recognized as a battery replacement.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Ordering Information



* Contact factory for availability.

BENCHMARQ

DV2007S1

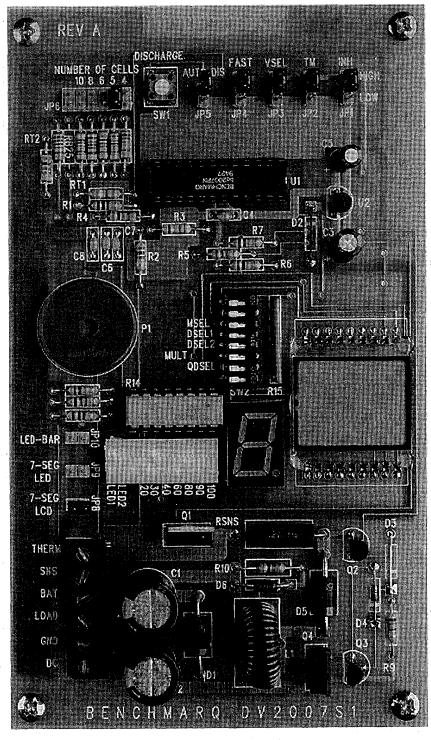
Fast Charge Development System

Control of On-Board Switch-Mode Regulator

2

Features

- bq2007 fast charge control evaluation and development
- Battery charge status display modes and driver interfaces are jumper configurable
  - On-board seven-step LED bargraph or ten-step BCD digit display
  - Charge status monitoring interface option
  - On-board charge status indication LEDs
- Fast charge termination by -ΔV, peak voltage detect (PVD), maximum temperature, time, and voltage
- Jumper-selectable for 4, 5, 6, 8, or 10 NiCd or NiMH cell pack charging
- Jumper-selectable standard or fast charge rates from 1 to 4 hours
- Discharge-before-charge push-button or automatic control



General Description

The bq2007 Fast Charge IC is a single-chip CMOS IC that performs charge control, charge status, and charge status display in a 24-pin DIP package. The DV2007S1 Development System offers a quick method to evaluate the bq2007 functional features and to validate selected parameters prior to design implementation. The board contain all the connections required to fully exercise the bq2007 features.

Fast charge is terminated by any of the following: -ΔV, peak voltage detect (PVD), maximum temperature, maximum time, and maximum voltage. Jumper settings select the voltage termination mode, driver mode selection (LED or LCD), display modes, time limits, and charge rate.

The user provides a DC power supply and batteries. A discharge-before-charge option is also provided by a push-button switch.

Contents

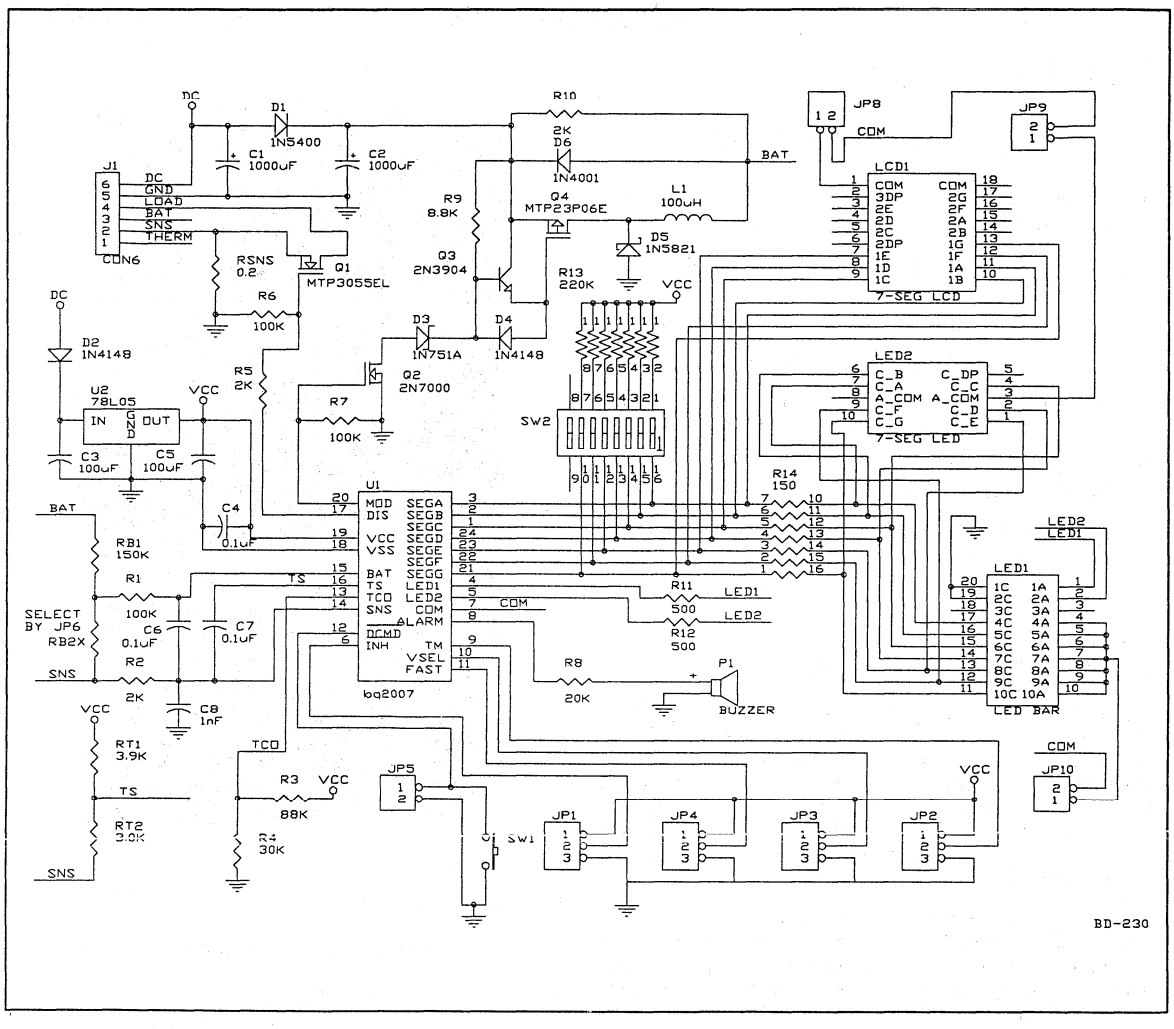
1 DV2007S1 printed circuit board containing:

a) bq2007 PDIP IC
b) Switch-mode current regulator
c) All programming jumpers
d) LCD and LED display hardware
e) NTC thermistor

1 bq Charge Configuration diskette

1 Documentation kit including user's guide, schematics, and data sheets

DV2007S1 Board Schematic



BENCHMARQ

Using the bq2007

Display Mode Options

Introduction

The bq2007 Fast Charge IC provides flexibility with a wide variety of charge status monitor display mode formats. The bq2007 internal charge status monitor can be configured to support up to a seven-segment bargraph or a single BCD digit display. The bargraph display indicates up to seven monotonic steps, whereas the BCD digit indicates ten steps of 10% increments. The bq2007 output drivers can direct-drive either LCD or LED interface levels.

Display Driver Modes

The bq2007 is designed to interface directly with LCD or LED type displays. The display driver mode is selected with the soft-programmed input MSEL and is independent of the state-of-charge monitor format or indications. The LED signal levels are driven when the MSEL soft-programmed input is pulled to V_{CC} at initialization. The output pin COM is the common-anode connection for LED SEG_{A-G}. See Figure 1.

The LCD interface mode is enabled when the MSEL soft-programmed input is pulled to V_{SS} at initialization. An internal oscillator generates all timing signals required for the LCD interface. Output pin COM is the common connection for static direct-driving of the LCD display backplane and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins are driven with the correct-phase AC signal to activate the LCD segment. See Figure 1.

Charge Status Indication

Table 1 summarizes the bq2007 charge status display indications. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED_2.

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system, where LED_1 indicates the precharge status (i.e., charge pending and discharge) and LED_2 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode allows the implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} mode allows for fault status information. See Figure 2.

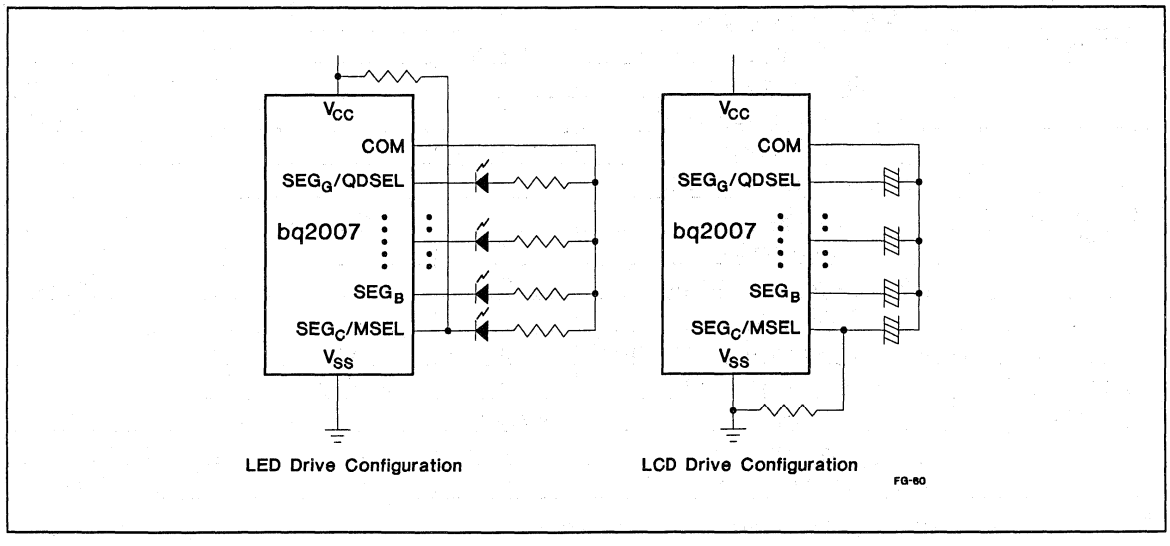


Figure 1. Display Driver Configurations

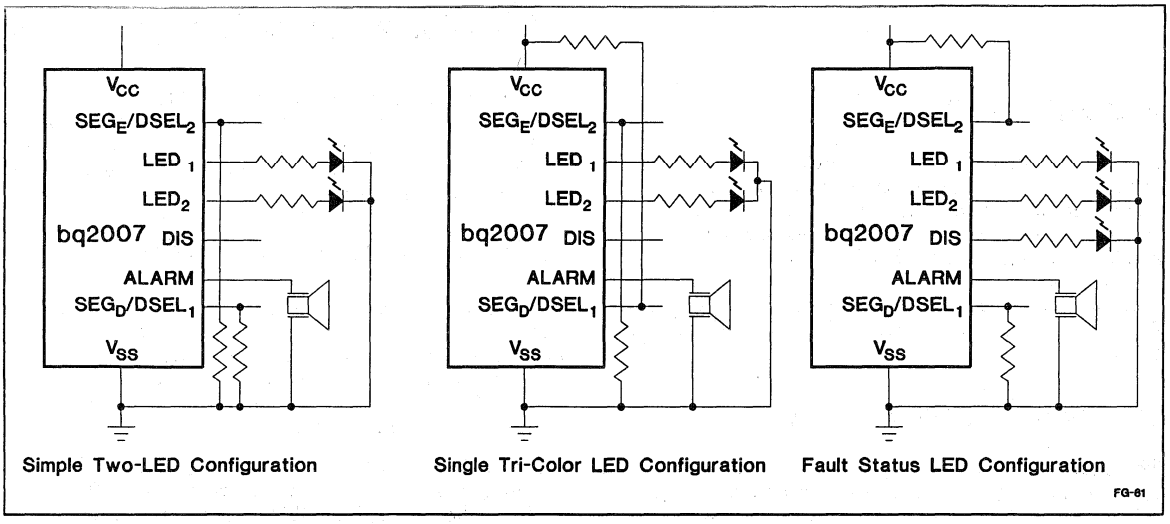


Figure 2. Charge Status Display Configurations

Table 1. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Audio Output Alarm

The bq2007 audio alarm output generates an audio tone to indicate a charge completion or fault condition. The audio alarm output is a symmetrical duty-cycle AC signal that is compatible with standard piezoelectric alarm elements. A valid battery insertion is indicated by a single 3.5kHz beep of ½-second typical duration. The charge completion and fault conditions are indicated by a 9.5- to 15-second high-tone sequence of ½-second typical duration at a 2-second typical repetition rate.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT soft-programmed input pin.

When MULT is pulled down to V_{SS}, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to 1/64 to 1/32 of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays 1/32 of the charge safety timer as a percentage of the full-charge time. This method is recommended over the voltage-based method when charging packs with different cell configuration (i.e. 5-cell or 6-cell pack) where the battery terminal voltages will vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged. When using the timer-based method, discharge-before-charge is recommended.

During discharge and when MULT is pulled down to V_{SS}, the charge status monitor indicates a percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. When V_{BAT} is greater than V_{80}, V_{60}, V_{40}, or V_{20}, the BCD digit format displays the 90%, 70%, 50%, and 30% respective charge indications. The discharge thresholds V_{80}, V_{60}, V_{40}, or V_{20} in bargraph format are indicated by the 90%, 60%, 40%, or 30% respective charge indications.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor BCD format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 2. The display modes are a seven-segment monotonic bargraph or a seven-segment BCD single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single BCD digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment charge status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments. See Figure 3.

The BCD display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a BCD zero count at charge initiation to a BCD nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Figure 4.

Table 2. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

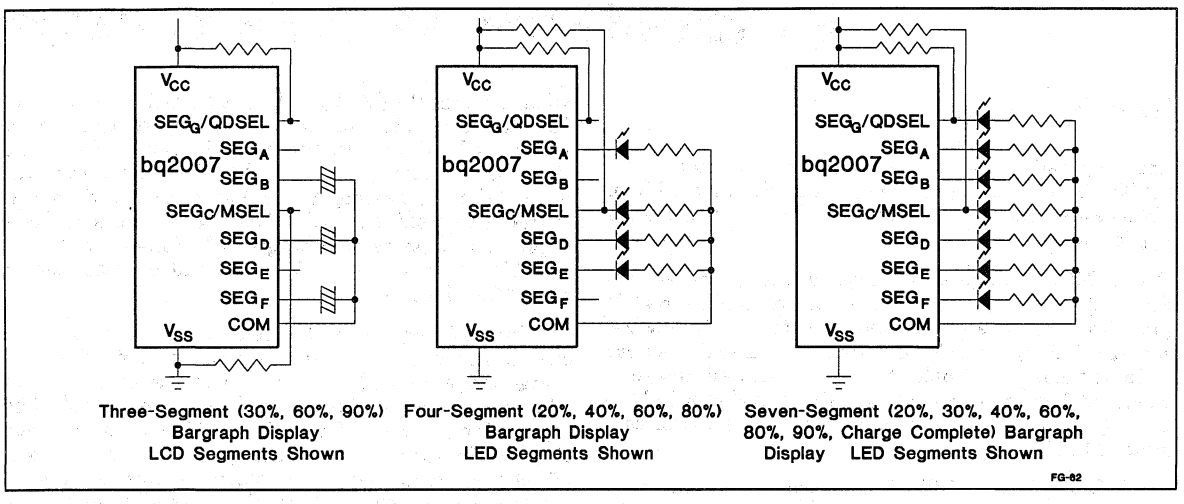


Figure 3. Charge Status Bargraph Display Configurations

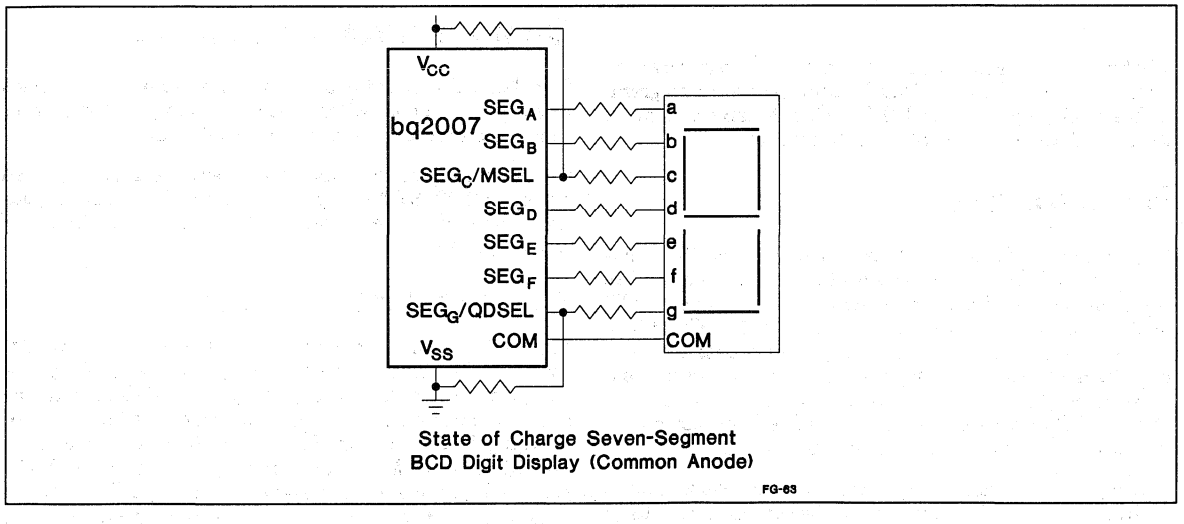


Figure 4. Charge Status BCD Digit Display Mode

Enhanced Features for Fast Charge

Introduction

This application note describes the correct setup of the bq2007 features and gives design examples for a NiCd or NiMH switch-mode and gated current source fast charger applications.

The bq2007 is targeted for applications requiring fast-charging and charge status monitoring at minimal cost. It provides sophisticated full-charge detection techniques such as PVD (peak voltage detection) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd).

The bq2007 offers flexibility by providing a wide variety of charge status monitoring and charge state display formats. The internal charge status monitor can be configured to support up to a seven-segment bargraph or a single-digit display. The bargraph display indicates seven monotonic steps, whereas the single digit counts in ten steps of 10% increments. The output can direct-drive either LCD or LED interface levels.

The bq2007 indicates charge state status with an audio alarm output option and two dedicated output pins with programmable display options. The $DSEL_{1-2}$ inputs can select one of the three display modes for the LED_{1-2} outputs.

Background

A significant advantage of the bq2007 over other fast-charge solutions is the flexibility to select PVD or -ΔV as the primary decisions for fast-charge termination. PVD is the recommended termination method for NiMH batteries, while -ΔV is recommended for NiCd batteries. -ΔV or PVD detection in the bq2007 may be temporarily disabled during periods when the charge current fluctuates. -ΔV or PVD may be permanently disabled without affecting other bq2007 charge-termination functions.

The bq2007 provides battery protection by trickle-charge conditioning of a battery that is below the low-voltage threshold (V_{EDV}). The battery voltage (V_{CELL}) is compared to the low-voltage threshold (V_{EDV}) and charge will be inhibited if $V_{CELL} < V_{EDV}$. The condition trickle current and fault time-out are a percentage of the fast charge rate and maximum time-out (MTO).

To ensure safety for the battery and system, fast charging also terminates based on a high-temperature cutoff threshold (TCO), a safety time-out, and a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2007 disables PVD, and -ΔV detection during a short "hold-off" period at the start of fast charge. During the hold-off period when fast charge is selected, the bq2007 charges at the topoff rate to prevent excessive overcharging of a fully charged battery. This hold-off period is configured as described in the bq2007 data sheet.

The bq2007 may be configured to have two or three charge stages. In a two-stage configuration, the fast-charge stage controlled by the bq2007 is preceded and followed by a pulse trickle charge at a rate controlled by bq2007 input pins FAST, TM, and VSEL. In a three-stage configuration, the fast charge is followed by a "top-off" charge stage where the battery is charged at 1/8 of the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, pulse trickle is used to compensate for self-discharge while the battery is idle. The trickle rate is C/64 for PVD and C/32 when -ΔV is enabled.

Charger Circuit Examples

Two detailed applications follow this section. One provides direct control of a switch-mode regulator, and the other provides control of an external current source.

The switching-mode constant-current regulator is used on the DV2007S1 development system. The board layout and schematic is described in the layout guidelines section on page 9.

Gating Current

Figure 1 shows an example of external gated current source. With SNS connected to V_{SS}, the bq2007 enables charge current to the battery by taking MOD high at the start of charging and maintaining this state until charging is terminated. In this example, R7, R19, R15, and Q1 and Q2 form the switching circuit. When MOD goes high, Q2 switches on—turning on Q1. When MOD goes low, the base current in Q1 is turned off and the charging path is switched off.

The current-handling capability of this circuit is limited by the product of the current gains of the transistors and by the 5mA drive capability of the MOD pin.

This limitation may be removed by replacing the PNP at Q1 with a pFET. See Table 1 for suggested transistors.

Table 1. Suggested Transistors (Q1)

Q1	Type	Package	Maximum Current	Maximum Voltage
IRFR9010	pFET	DPAK	5.3	-50
IRFR9022	pFET	DPAK	9.0	-50
IRFR9020	pFET	DPAK	9.9	-50
IRFD9014	pFET	HEXDIP	1.1	-60
IRFD9024	pFET	HEXDIP	1.6	-60
IRF9Z10	pFET	TO-220	4.7	-50
IRF9Z22	pFET	TO-220	8.9	-50
IRF9Z20	pFET	TO-220	9.7	-50
IRF9Z32	pFET	TO-220	15	-50
BD136	PNP	TO-225	1.5	-60
MJE171	PNP	TO-225	3.0	-60
TIP42A	PNP	TO-220	6.0	-60

Note: For very high currents, two paralleled pFETs or an nFET with a high-side driver circuit may be suitable.

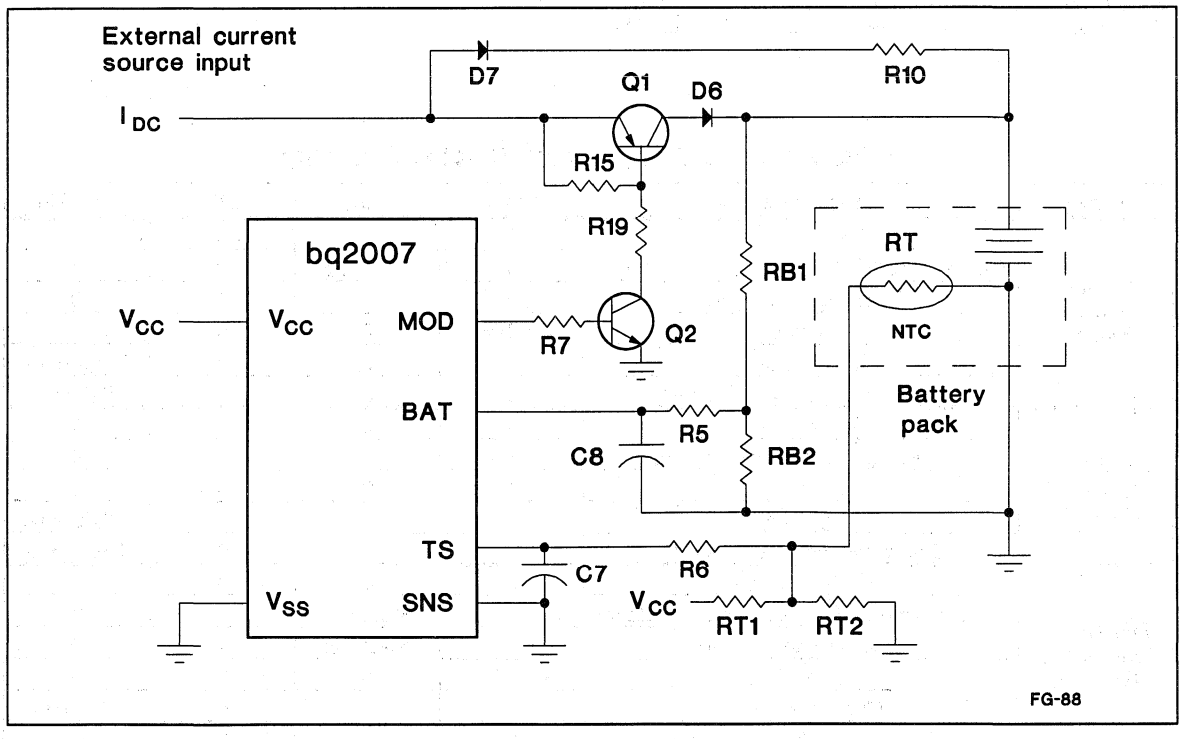


Figure 1. Gated External Source (Bipolar Switch Option)

Charge Action Control

The bq2007 charge action is controlled by input pins $\overline{DCMD}$, VSEL, FAST, and TM. When charge action is initiated, the bq2007 enters the charge-pending state, checks for acceptable battery voltage and temperature, and performs any required discharge-before-charge operations. $\overline{DCMD}$ controls the discharge-before-charge function, and VSEL, FAST, and TM select the charger configuration. See Tables 4 and 5 of the bq2007 data sheet.

Charge Status Indication

Table 2 summarizes the bq2007 charge status display. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED_2.

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system, where LED_2 indicates the precharge status (i.e., charge pending and discharge) and LED_1 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode is for implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} mode allows for fault status information.

Audio Alarm Selection

The alarm output waveform is a 3.5KHz square wave signal that allows a direct connection to drive standard piezoelectric alarm elements. Piezoelectric alarm elements are designed for a maximum sound output at a specific frequency and drive voltage. The alarm element must be selected for a maximum sound output at a frequency of 3.5kHz with a 5V peak-to-peak drive signal. The PCB mount element can be connected directly to the bq2007 alarm output with a 20K isolation resistor. The design of a molded resonant cavity should follow the manufacturers recommended procedures to assure maximum sound output. Manufactures also provide several boost circuits that can be used to increase the drive voltage for increased sound output levels.

Table 2. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Nov. 1994

Selecting the BAT Divider for Charge Monitoring

The voltage based state of charge monitoring is enabled when charging packs with a fixed number of cells by pulling the multi-cell pack select input MULTI to V_{SS}. When MULT = 0, internal voltage thresholds are compared with the BAT pin input voltage for both charge and discharge capacity status indications. When discharge-before-charge is initiated, the state-of-charge monitor indicates the discharge condition as monotonic decreasing steps from the charged condition. The voltage charge status monitoring circuit is shown in Fig. 2. The circuit changes its voltage threshold reference divider for charge or discharge monitoring when the discharge signal is zero or one, respectively. The voltage thresholds are a fixed ratio of the VCC supply voltage and are specified in the bq2007 data sheet in the section entitled "DC Thresholds." The voltage thresholds were selected based on typical NiCad and NiMH battery characteristics for a typical charge rate of 1C and a typical discharge rate of 1 Amp.

To optimize the charge status monitoring for a range of fixed-cell packs (i.e. MULTI = 1), the BAT divider should be calculated such that the highest fixed cell pack will be centered at the EDV threshold. For example, to charge packs that range from 4 to 6 fixed cells, select the BAT divider MULTI = 0. The BAT divider should be determined by BAT divider equation 2 for values shown in Table 4. To further optimize, you can fit the battery characteristics to the end points of the EDV and MCV thresholds. This will center the battery voltage charge characteristics in the center of the bq2007 charge monitoring thresholds. This is possible since the full charge detection methods (PVD, -DV) are not dependent on absolute voltage value. When adjusting the battery divider, the maximum cutoff voltage (V_{MCV}) must not be exceeded.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT input pin.

When MULT is pulled down to V_{SS}, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly

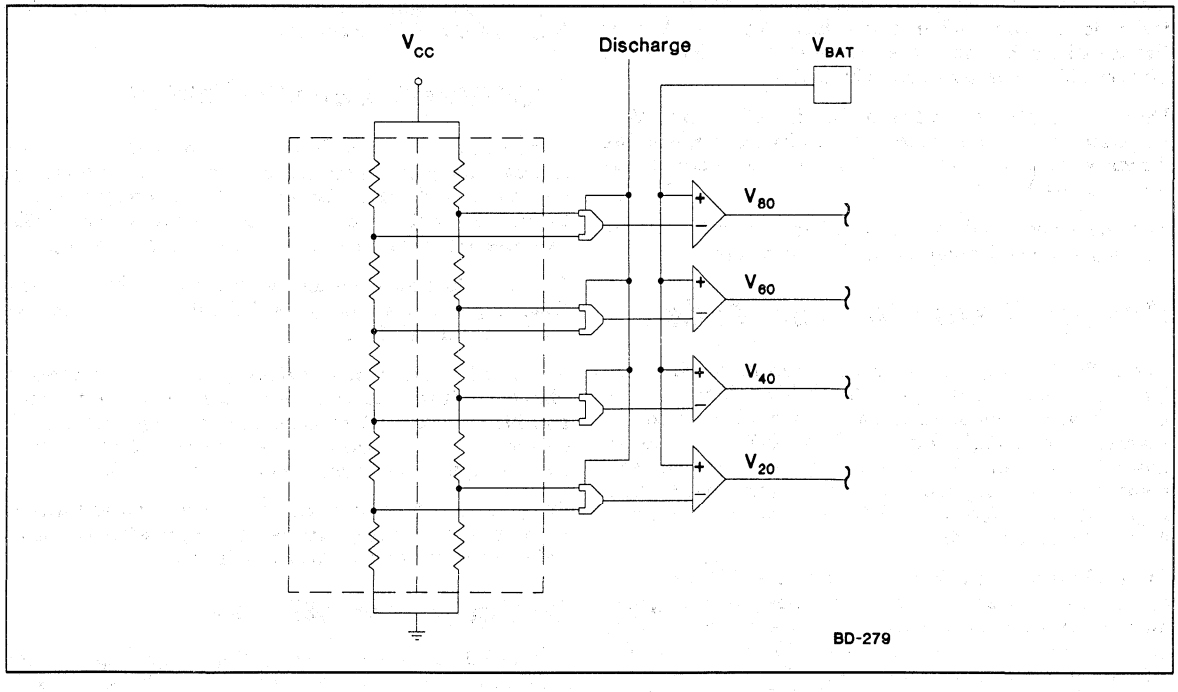


Figure 2. Voltage Charge Status Monitoring Circuit

indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to 1/64 to 1/32 of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays 1/32 of the charge safety timer as a percentage of full charge. This method is recommended over the voltage-based method when charging multi-cell packs where the battery terminal voltages can vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged.

During discharge and when MULT is pulled down to V_{SS}, the charge status monitor indicates a percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. When V_{BAT} is greater than V_{80}, V_{60}, V_{40}, or V_{20}, the single-digit format displays the 90%, 70%, 50%, and 30% respective charge indications. The discharge thresholds V_{80}, V_{60}, V_{40}, or V_{20} in bargraph format are indicated by the 90%, 60%, 40%, or 30% respective charge indications.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor segment format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 3. The display modes are a seven-segment monotonic bargraph or a seven-segment single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single segment digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment charge status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments.

The segment display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a segment zero count at charge initiation to a segment nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Table 3.

Display Driver Modes

The bq2007 is designed to interface with LCD or LED type displays. The LED signal levels are driven when the MSEL input is pulled to V_{CC} at initialization. The output pin COM is the common anode connection for LED SEG_{A-G}.

The LCD interface mode is enabled when the MSEL input pin is pulled to V_{SS} at initialization. An internal oscillator generates all the timing signals required for the LCD interface. The output pin COM is the common connection for static direct-driving of the LCD display backplate and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins is driven with the correct-phase AC signal to activate the LCD segment. In segment mode, output pins SEG_{A-G} interface to LED or LCD segments.

Discharge Before Charge

It may be desirable in the application to allow the user to occasionally discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 3 illustrates the implementation of this function. Discharge-before-charge is initiated on a positive strobe signal on DCMD.

Note: This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS to a high state until the voltage sensed on BAT falls below $V_{CC}/5$. Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

Configuring the BAT Input

The bq2007 uses the battery voltage sense input on the BAT pin to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit,

facilitate peak voltage detect (PVD) and negative delta voltage (-ΔV) detection, and detect a battery replacement.

V_{BAT} may be derived from a simple resistive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range. When MULT is pulled up to V_{CC}, battery voltage is sensed at the BAT pin by a resistive voltage divider that divides the terminal voltage between 0.262 * V_{CC} (V_{EDV}) and 0.8 * V_{CC} (V_{MCV}). The bq2007 charges multi-cell battery packs from a minimum of N cells, to a maximum of 1.5 * N cells. The battery voltage divider is set to the minimum cell battery pack (N) by the BAT pin voltage divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1.33}\right) - 1 \qquad \text{Equation 1}$$

When MULT is pulled down to V_{SS}, tighter charge voltage limits and voltage-based charge status display are selected. This is recommended for charging packs with a fixed number of cells where the battery voltage divider range is between 0.4 * V_{CC} (V_{EDV}) and 0.8 * V_{CC} (V_{MCV}). The bq2007 charges fixed-cell battery packs of N cells. The battery voltage divider is set by the divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{2}\right) - 1 \qquad \text{Equation 2}$$

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the BAT pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from BAT between 20KΩ and 1MΩ is acceptable over the bq2007 operating range. Total impedance between the battery terminal and VSS should typically be about 300KΩ to 1MΩ . See Table 4.

Note: Because V_{SNS} may be positive in bq2007 switching regulation applications, the actual internal comparison uses V_{BAT} – V_{SNS}, or V_{CELL}. This internal value V_{CELL}

Table 3. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Nov. 1994

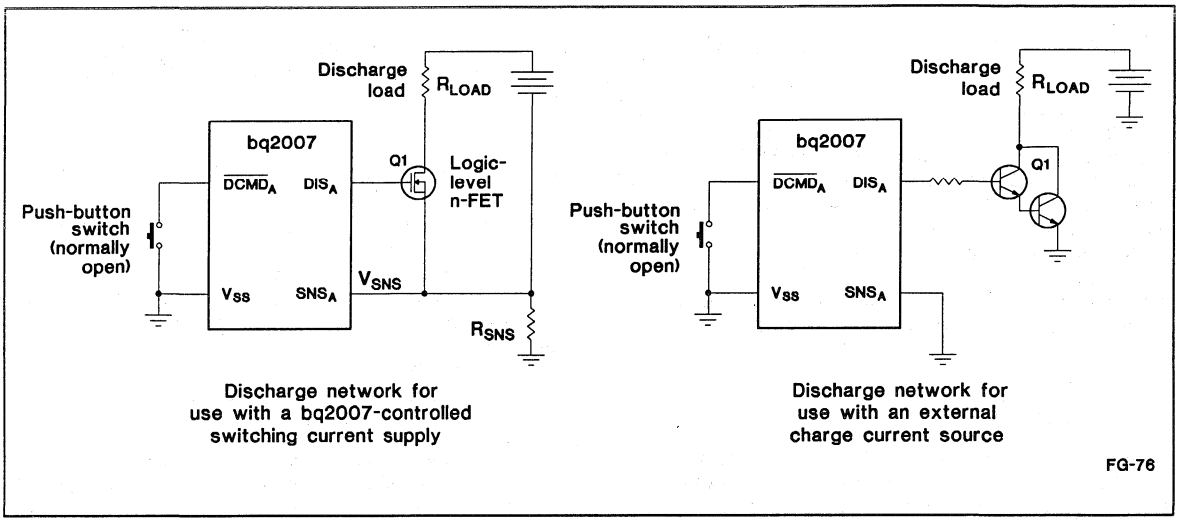


Figure 3. Battery Conditioning Network

maintains a representative voltage independent of any current through R_{SNS}.

Table 4. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1	RB2
4	200 KΩ	200 KΩ
5	200 KΩ	133.3 KΩ
6	200 KΩ	100 KΩ
8	200 KΩ	66.7 KΩ
10	200 KΩ	50 KΩ

Note: MULTI = 0; RB1/RB2 = (N/2) - 1.

Temperature Sensing and the TCO Pin

The bq2007 uses the temperature sense input on the TS pin to qualify charge initiation and termination. A negative temperature coefficient (NTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 1. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT.

Temperature-decision thresholds are defined as LTF (low-temperature fault) and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-TCO range. In this case, the charge pending state is active on the charge status display (see Table 2), and charging does not initiate until the battery temperature returns to this range.

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2007 interprets the reference points V_{LTF} and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at ½ V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 4. Note that since the voltage on pin TS decreases as temperature increases, V_{TCO} should always be less than ½ V_{CC}. The resistive dividers may be used to generate the desired V_{TCO}.

Vcc Supply

The V_{CC} supply provides both power and voltage reference to the bq2007. This reference directly affects BAT voltage and internal time-base voltage measurements.

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = 5V. The oscillator varies directly with V_{CC}. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

Charge State Actions

Once the required discharge is completed and temperature and voltage prequalifications are met, the charge state is initiated. The charge state is configured by the VSEL, FAST, and TM input pins. The FAST input selects between Fast and Standard charge rates. The

Table 5. bq2007 Charge Action Control Summary

FAST Input State	TM Input State	Time-out Period (min)	MOD Duty Cycle	Hold-off period (sec)	Trickle Rep Rate -ΔV C/32	Trickle Rep Rate PVD C/64
V_{SS}	Float	640 (C/8)	25%	2400	219Hz	109Hz
V_{SS}	V_{SS}	320 (C/4)	25%	1200	109Hz	55Hz
V_{SS}	V_{CC}	160 (C/2)	25%	600	55Hz	27Hz
V_{CC}	Float	160 (C/2)	100%	600	219Hz	109Hz
V_{CC}	V_{SS}	80 (C)	100%	300	109Hz	55Hz
V_{CC}	V_{CC}	40 (2C)	100%	150	55Hz	27Hz

Standard charge rate is ¼ of the Fast charge rate, which is accomplished by disabling the regulator for a period of 286µs of every 1144µs (25% duty cycle). In addition to throttling back the charge current, time-out and hold-off safety time are increased accordingly.

The VSEL input selects the voltage termination method. The termination mode sets the top-off state and trickle charge current rates. The TM input selects the Fast charge rate, the Standard rate, and the corresponding charge times. Once charging begins at the Fast or Standard rate, it continues until terminated by any of the following conditions:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum temperature cutoff (TCO)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

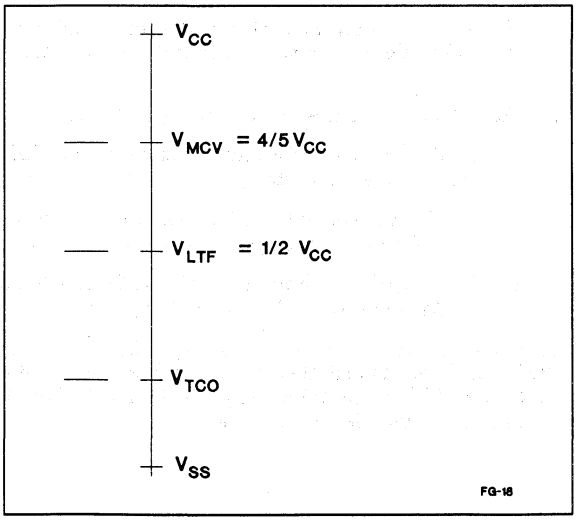


Figure 4. Temperature Reference Points

Voltage Termination Hold-off

To prevent early termination due to an initial false peak battery voltage, the -ΔV and PVD terminations are disabled during a short "hold-off" period at the start of charge. During the hold-off period when fast charge is selected (FAST = 1), the bq2007 will top off charge to prevent excessive overcharging of a fully charged battery. Once past the initial charge hold-off time, the termination is enabled. TCO and MCV terminations are not affected by the hold-off time.

-ΔV or PVD Termination

Table 6 summarizes the two modes for full-charge voltage termination detection. When VSEL = V_{SS}, negative delta voltage detection occurs when the voltage seen on the BAT pin falls 12mV typical per cell below the maximum sampled value. VSEL = V_{CC} selects peak voltage detect termination and the top-off charge state. When charging a battery pack with a fixed number of cells, the battery voltage divider can be set to sense two cells; thus the -ΔV and PVD termination thresholds are -6mV and 0 to -3mV, respectively. The valid battery voltage range on V_{BAT} for -ΔV or PVD termination is from 0.262 * V_{CC} to 0.8 * V_{CC}.

Top-Off Charge

The top-off charge option allows for the self-discharge replacement trickle current to be very low, but still provides for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off occurs at 1/8 of the fast charge rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. It also terminates if TCO or MCV is detected.

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use.

Pulse trickle is used to compensate for self-discharge while the battery is idle and to condition a depleted low-voltage battery to a valid voltage prior to high-current charging. The battery is pulse trickle charged when Fast, Standard, or top-off charge is not active. This results in a trickle rate of C/64 for PVD and C/32 when -ΔV is enabled.

Table 6. VSEL Configuration

VSEL	Detection Method	Top-Off	Pulse Trickle Rate
V_{SS}	-ΔV	Disabled	C/32
V_{CC}	PVD	Enabled	C/64

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2007 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Power Supply Selection

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2007 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the charge operation, V_{DC} > (number of cells * MCV_{MAX}) + V_{LOSS} in the charging path. (MCV_{MAX} is the maximum cell voltage threshold with the maximum bq2007 V_{CC}.)

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by approximately 1V to 2V.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2007 is important when the bq2007 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept relatively isolated from the bq2007 and its supporting components.
3. 0.1μF and 10μF decoupling capacitors should be placed close together and very close to the V_{CC} pin.
4. 0.1μF capacitors and resistors forming R-C filters connected to pins BAT, TS, TCO, and MCV should be as close as possible to their associated pins.
5. Because the bq2007 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the DCMD input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2007-modulated switching applications:
   - A 2KΩ resistor is required between the MOD pin and the transistor.
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the SNS pin.
   - The 0.1μF capacitors for BAT and TS should be routed directly to SNS and not to ground.

Figures 6, 7, and 8 show an example layout of the DV2007S1 Development Board. Figure 9 is a schematic of the board. Table 7 contains the parts list for the board. A comparable layout is recommended.

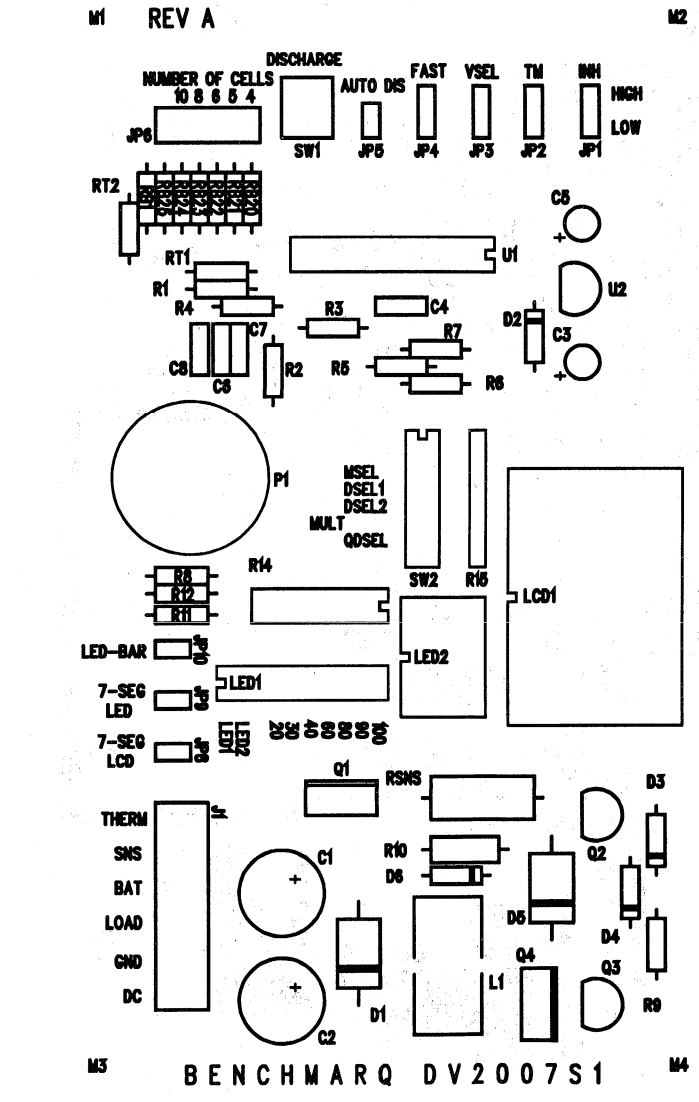


Figure 6. DV2007S1 Development Board Layout

Component Placement

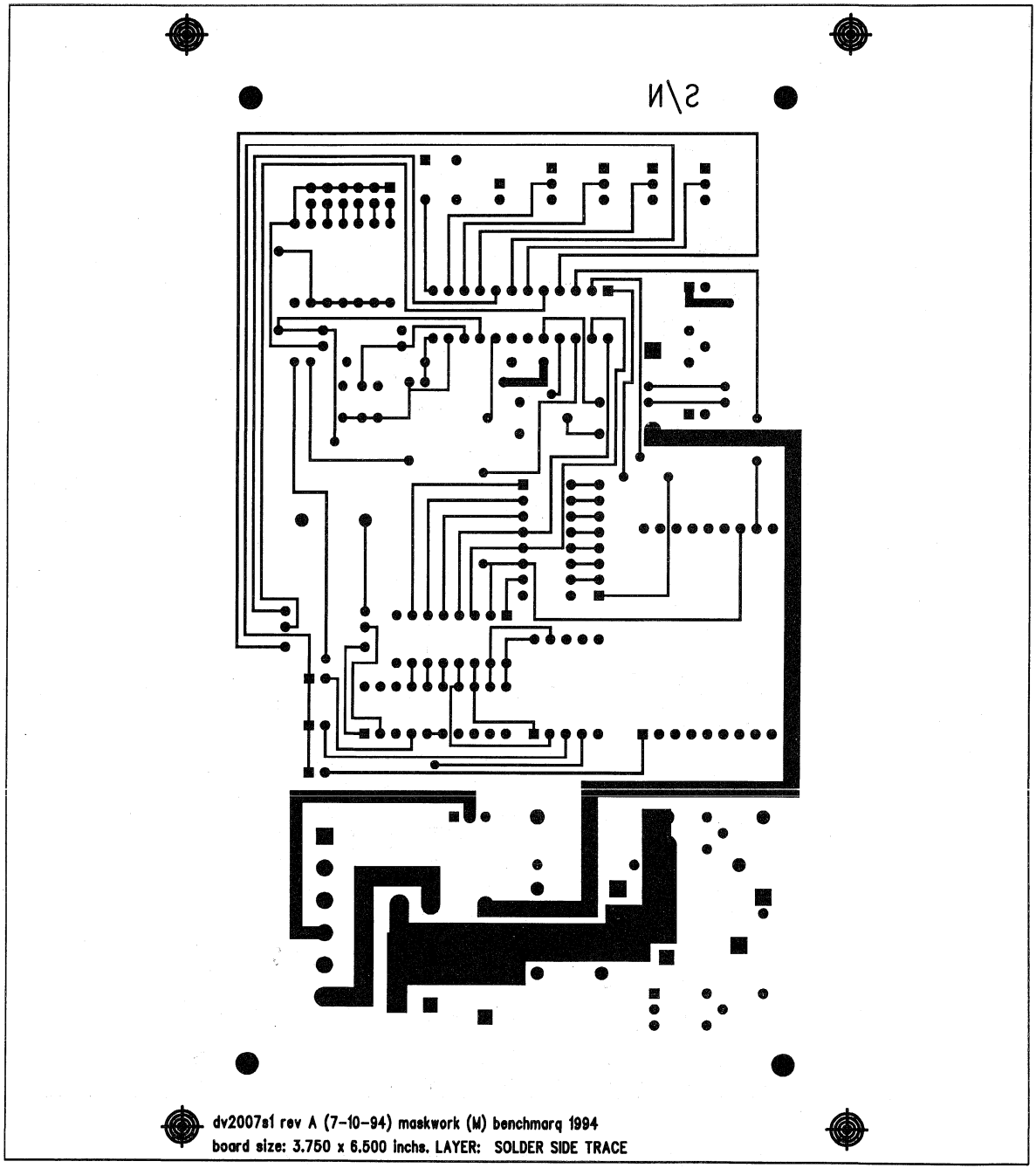


Figure 7. DV2007S1 Development Board Layout

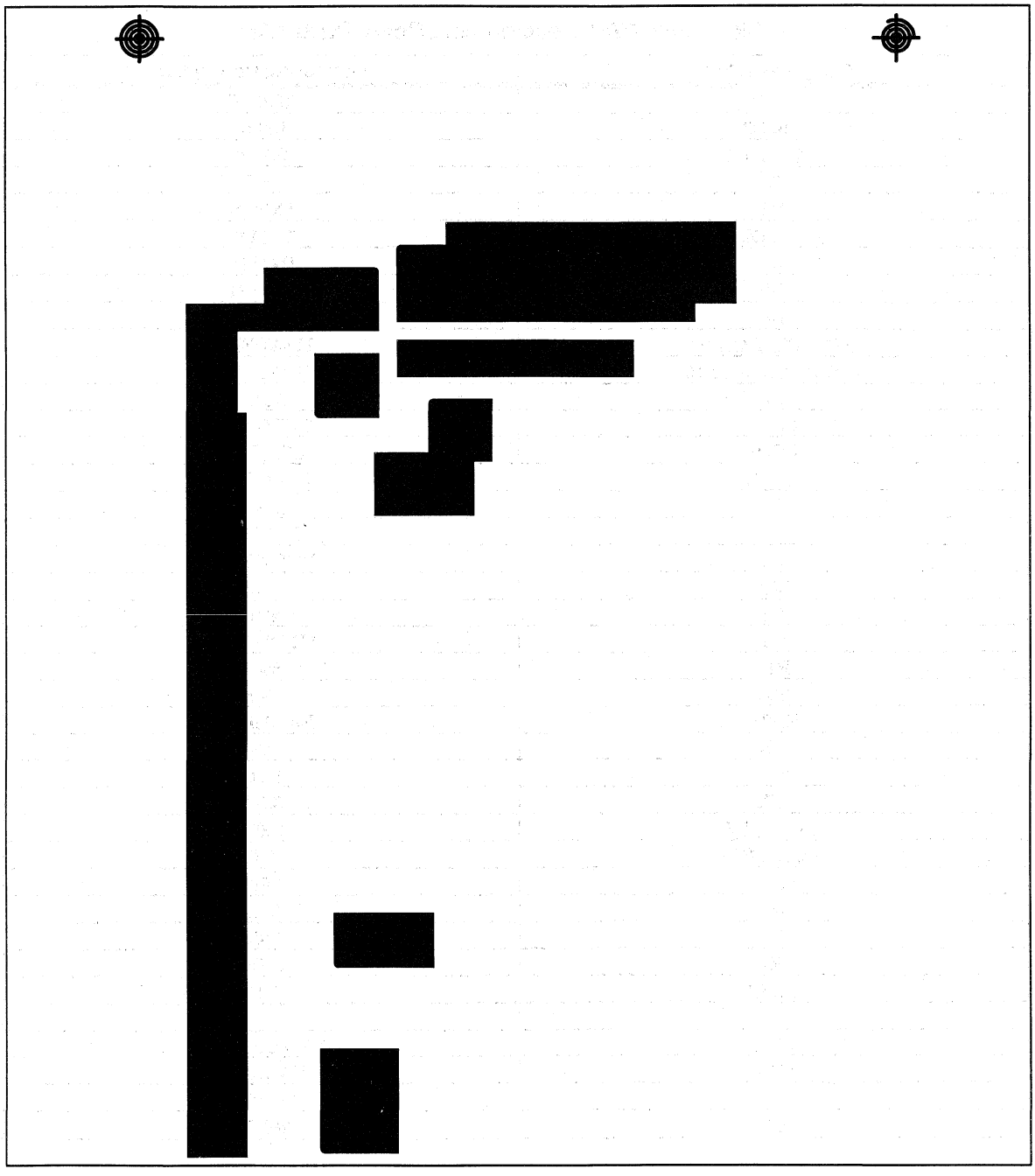


Figure 8. DV2007S1 Development Board Layout

Table 7. DV2007S1 Development Board Parts List

Component Name	Component Description
C2, C1	1000µF
C5, C3	100µF
C4, C6, C7	0.1µF
C8	1nF
D1	1N5400
D4, D2	1N4148
D3	1N751A
D5	1N5821
D6	1N4001
JP1, JP2, JP3, JP4	HEADER 3
JP5, JP8, JP9, JP10	HEADER 2
J1	CON6
LCD1	7-SEG LED
LED1	LED BAR
LED2	7-SEG LCD
L1	100µH
P1	BUZZER
Q1	MTP3055EL
Q2	2N7000
Q3	2N3904
Q4	MTP23P06E
R14	Resistor 8pack
RB1	150K
RB2X	User Selected
RSNS	0.2
RT1	3.9K
RT2	3.0K
R1, R6, R7	100K
R2, R5, R10	2K
R3	88K
R4	30K
R8	20K
R9	8.8K
R12, R11	500
SR	SIP8
SW1	SW pushbutton
SW2	SW DIP-8
U1	bq2007
U2	78L05

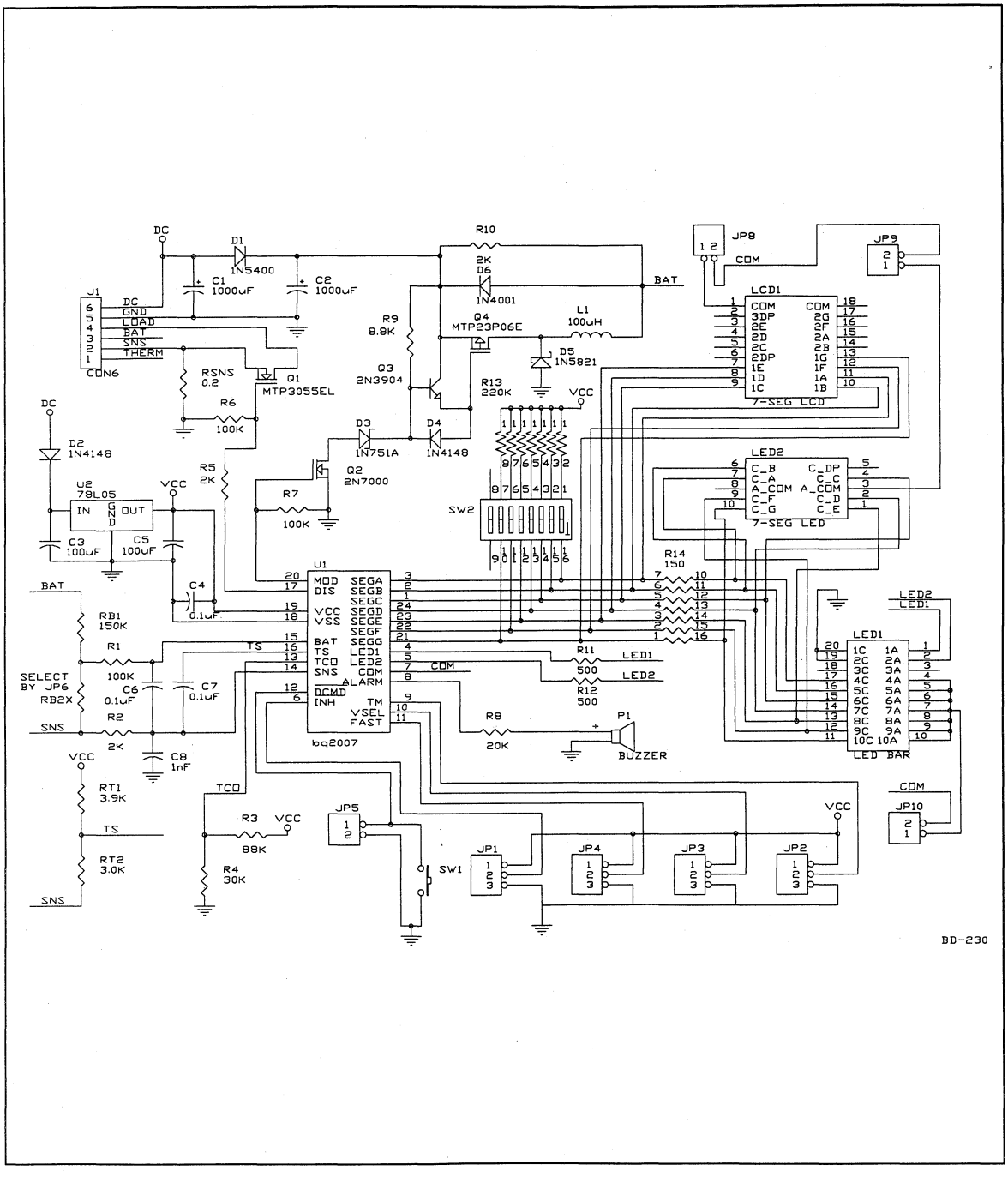


Figure 9. DV2007S1 Development Board Schematic

BENCHMARQ

bq2010

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for battery pack integration
  - 120µA typical standby current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- Accurate measurements across a wide range of current (> 500:1)
- 16-pin narrow DIP or SOIC

General Description

The bq2010 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

NiMH and NiCd battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

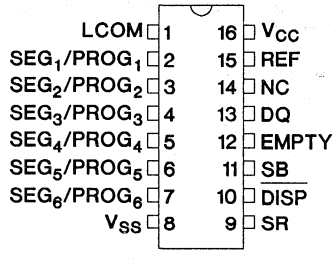
Nominal available charge may be directly indicated using a five- or six-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2010 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2010 outputs battery information in response to external commands over the serial link.

The bq2010 may operate directly from 3 or 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2010 gas gauge data registers.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-35

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	NC	No connect
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	EMPTY	Empty battery indicator output
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
$SEG_6/PROG_6$	LED segment 6/ program 6 input	SR	Sense resistor input
		V_{CC}	3.0–6.5V
		V_{SS}	System ground

Pin Descriptions

LCOM **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_6 **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the self-discharge compensation rate shown in Table 1.

$PROG_6$ **Display mode selection (dual function with SEG_6)**

This three-level pin defines the display operation shown in Table 1.

NC **No connect**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2010 is $V_{SR} + V_{OS}$ (see Table 4 on page 8).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during discharge or charge if the NAC registers update at a rate equivalent to $|V_{SRO}| \geq 4mV$. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY **Battery empty output**

This open-drain output becomes high-impedance on detection of a valid end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

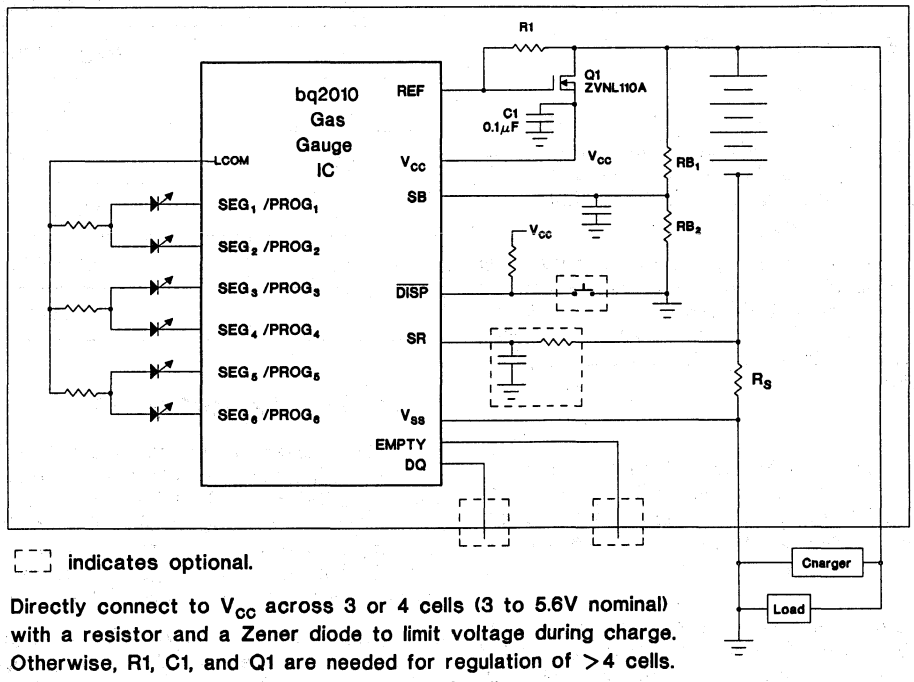
Functional Description

General Operation

The bq2010 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2010 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2010 using the LED display capability as a charge-state indicator. The bq2010 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2010 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 5.6V nominal) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of >4 cells. The value of R1 depends on the number of cells.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required, application-specific.

BD-179

Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2010 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2010 are fixed at:

V_{EDV1} (early warning) = 1.05V

V_{EDVF} (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. EDV monitoring may be disabled under certain conditions as described in the next paragraph.

During discharge and charge, the bq2010 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -150mV typical and resumes ½ second after $V_{SR} >$ -150mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDVF}$ and remains latched until a valid charge occurs. The bq2010 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2010 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described on page 14.

Temperature

The bq2010 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2010 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_{SNS}) should be as close as possible to the bq2010.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2010. The bq2010 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2010 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The PFC also provides the 100% reference for the absolute display mode. The bq2010 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

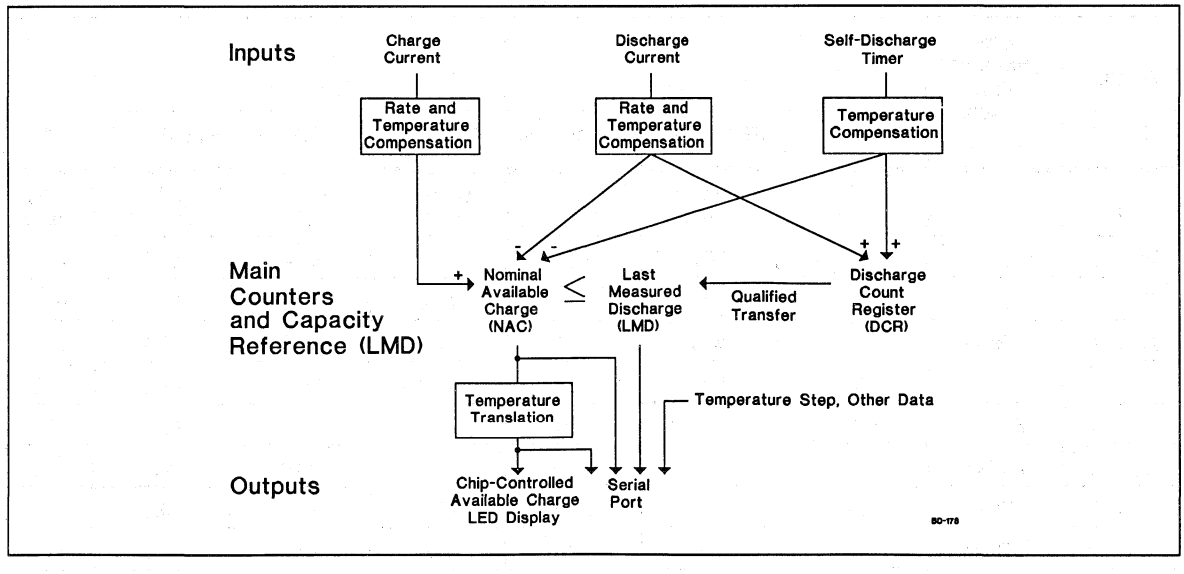


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = $C/64$
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh * 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2010 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2010 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Display Mode	$\overline{DISP}$ Display State
H	Reserved	NAC = PFC on reset	LED disabled
Z	$NAC/64$	Absolute	LED-enabled on discharge or charge when equivalent $\lvert V_{SRO} \rvert \geq 4mV$
L	$NAC/47$	Relative	LED on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2010 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization ($PROG_6$ = Z or low) and on the first valid charge following discharge to EDV1. NAC is set to PFC on initialization if $PROG_6$ = high. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charge initiations (charges greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2010 increments NAC at a rate proportional to V_{SRO} and, if enabled, activates an LED display if the rate is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2010 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} (V_{SR} + V_{OS}) falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRQ} is 375µV.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2010 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/64 * NAC or 1/47 * NAC per day as selected by $PROG_5$. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2010 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge compensation factor is based on the dynamically measured V_{SR}.

The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.0 + (0.05 * N)$$

Where N = Number of 10°C steps below 10°C and $-150mV < V_{SR} < 0$.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C : N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C : N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C : N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C : N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/64 * NAC or 1/47 * NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2010 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2010

The bq2010 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2010 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2010 should be pulled up by the host system, or may be left floating if the serial interface is not used.

Table 5. bq2010 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

The interface uses a command-based protocol, where the host processor sends an eight-bit command byte to the bq2010. The command directs the bq2010 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2010 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2010. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2010 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2010 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2010 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2010 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2010 NAC register.

bq2010 Registers

The bq2010 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2010. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

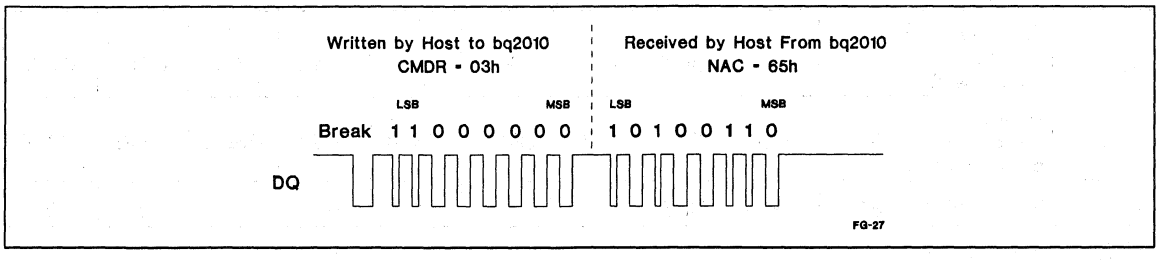


Figure 3. Typical Communication With the bq2010

Table 6. bq2010 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2010 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2010 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2010 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1\ V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2010 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2010 is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2010 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 register description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2010 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2010 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2010. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. NACL stops counting when NACH reaches zero. When the bq2010 detects a valid charge, NACL resets to 0. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2010 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2010. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2010 uses as a measured full reference. The bq2010 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2010 updates the capacity of the battery. LMD is set to PFC during a bq2010 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2010 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV (overload, OVLD=1)

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -150mV. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after V_{SR} > -150mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination. Sampling is re-enabled 0.5 secs after the overload condition is removed.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2010. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2010. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2010 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2010. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2010 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2010.*

Resetting the bq2010 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: NACH = PFC when $PROG_6$ = H.

Display

The bq2010 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2010 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD. The sixth segment, SEG_6, is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC, with SEG_6 representing "overfull" (charge above the PFC). As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-6} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to $|V_{SRO}| \geq 4mV$. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a

short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2010 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2010, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2010 can be inexpensively built using the FET and an external resistor; see Figure 1.

2

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2010 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, $V_{SR} + V_{OS}$
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ, EMPTY
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

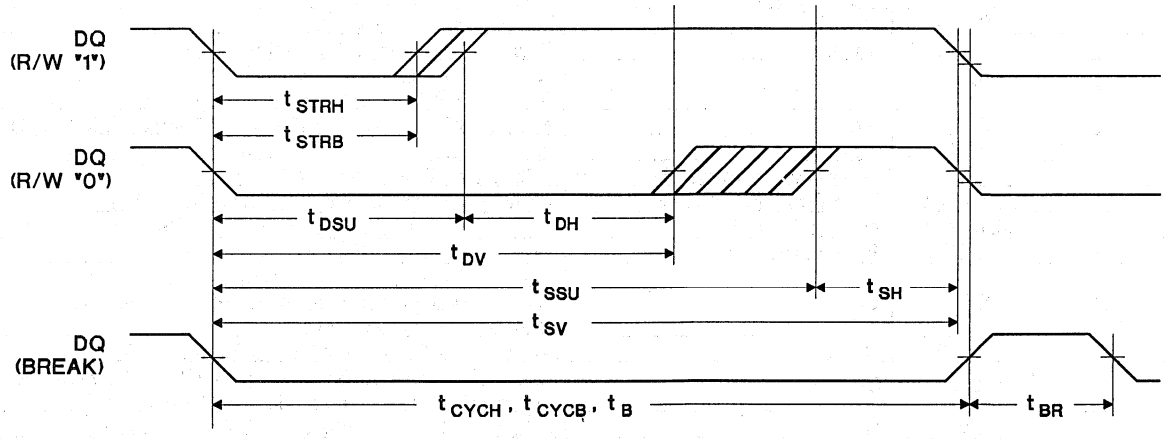
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2010	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2010 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2010	5	-	-	ns	
t_{STRB}	Start hold, bq2010 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



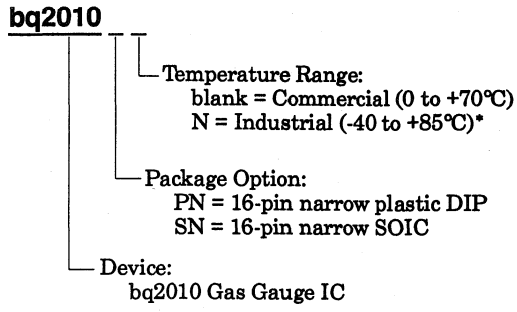
RC-34

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1, 2	2-210	Changed display activation threshold	Was: Based on NAC count rate; Is: Based on V_{SRO} > 4mV
1	2-212	Changed EMPTY output activation voltage	Was: V_{SB} = EDV1; Is: V_{SB} = EDVF
1	2-212,2-219	Maximum cell voltage	Was: V_{SB} = 2.0V; Is: V_{SB} = 2.25V
1	2-214	Updated Table 1	LED activated based on V_{SB}
1, 2	2-215,2-220	Changed valid charge determination	Was: 256 NAC counts/136 min.; Is: 256 NAC counts with $V_{SRO} > V_{SRQ}$
1, 2	2-215	Changed discharge counting	Was: All discharge counts caused NAC to decrement; Is: All discharge counts cause NAC to decrement when $V_{SRO} < V_{SRD}$
1, 2	2-216	Discharge compensation factors	Was: Scaled discharge compensations between 0.95 and 1.15; Is: Scaled discharge compensations between 1.0 and 1.05
1, 2	2-216	Current sensing error	Added digital proportional magnitude filter to eliminate NAC counts between $V_{SRD} \le V_{SR} + V_{SRO} \le V_{SRQ}$
1, 2	2-219	Charge status flag	Was: Initiated if charge exceeded 0.031 counts/sec; Is: Initiated if $V_{SRO} > V_{SRQ}$
1	2-219	Battery removed	Was: V_{SB} = 2.0V; Is: V_{SB} = 2.25V
1	2-220	VDQ	Clarification: VDQ is 1 on first discharge after NAC = LMD.
1, 2	2-221	Discharge rate flag	Was: -50mV to -300mV; Is: -150mV
1	2-223	LED segment outputs	Update: Each segment bank is active for 30% of the period.
1, 2	2-223	Valid charge	Added: V_{SRQ} minimum $V_{SR} + V_{OS}$
1, 2	2-223	Valid discharge	Added: V_{SRQ} maximum $V_{SR} + V_{OS}$
1	2-223	Maximum single-cell voltage	Was: 1.95 to 2.05V; Is: 2.20 to 2.30V
1	2-224	Battery input	Was: - to 2.4V; Is: 0 to V_{CC}
1	2-224	DQ input high	Was: V_{CC} - 1.0; Is: 2.5V
1	2-224	DQ input low	Was: 1.0V; Is: 0.8V
1	2-224	I_{CC}	Defined I_{CC} with DQ = 0
1	2-224	t_{CYCB}	Was: 3 to 5ms; Is: 3 to 6ms
2	2-214	Update Table 1	Was: $PROG_6$ = H: reserved Is: $PROG_6$ = H: NAC = PFC on reset
2	2-215	NAC	Added: NAC is set to PFC on initialization if $PROG_6$ =H
2	2-215	DCR	Was: Temp ≥ 10°C; Is: Temp ≥ 0°C
2	2-216	Discharge compensation factor	Eliminated V_{SR} < -300mV factor
2	2-216,2-222	Digital magnitude filter	Added programmable digital magnitude filter
2	2-218,2-221	Update Table 6	Added: NACL and DMF registers; eliminated OCTL
2	2-220	Valid discharge	Was: Temp ≥ 10°C; Is: Temp ≥ 0°C
2	2-222	CPI	Was: Temp ≥ 10°C; Is: Temp ≥ 0°C; Clarification: CPI incremented only once for a valid charge if NAC > 0.94 * LMD
2	2-222	Reset	Added: NACL = 0; NACH = PFC if $PROG_6$ = H
2	2-222	Display	Clarification: Display becomes active if the NAC registers are counting at a rate equivalent to $\lvert V_{SRO} \rvert \ge 4mV$
2	2-223	REF	Added: REF to absolute maximum ratings table

Note: Change 1 = Nov. 1993 B changes from June 1993 A.
Change 2 = Mar. 1994 C changes from Nov. 1993 B.

Ordering Information



* Contact factory for availability.

Notes

BENCHMARQ

EV2010

bq2010 Evaluation System

Features

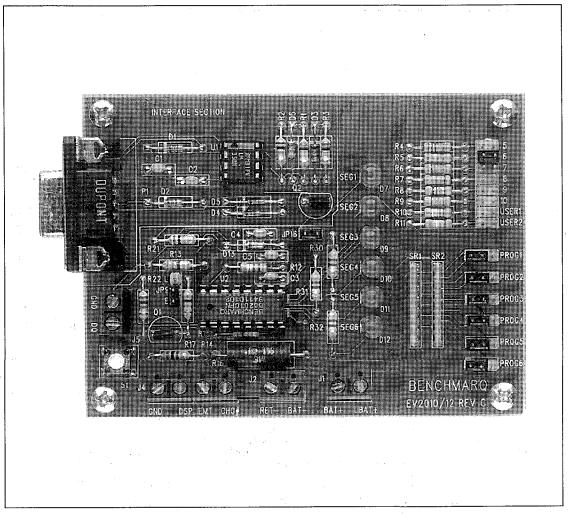
- bq2010 Gas Gauge IC evaluation and development system
- RS-232 interface hardware for easy access to state-of-charge information via the serial port
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- On-board regulator for greater than 4-cell applications
- State-of-charge information displayed on bank of 6 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable
- Display mode jumper-configurable

General Description

The EV2010 Evaluation System provides a development and evaluation environment for the bq2010 Gas Gauge IC. The EV2010 incorporates a bq2010, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd or NiMH cells.

Hardware for an RS-232 interface is included on the EV2010 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2010. Direct connection to the serial port of the bq2010 is also made available for check-out of the final hardware/ software implementation.

The menu-driven software provided with the EV2010 displays charge/discharge activity and allows user interface to the bq2010 from any standard DOS PC.



Contents

1 EV2010 printed circuit board containing:

a) bq2010 PDIP IC
b) RS-232 interface hardware
c) On-board regulator
d) Bank of 6 LEDs
e) Sense resistor (0.1Ω)
f) All programming jumpers

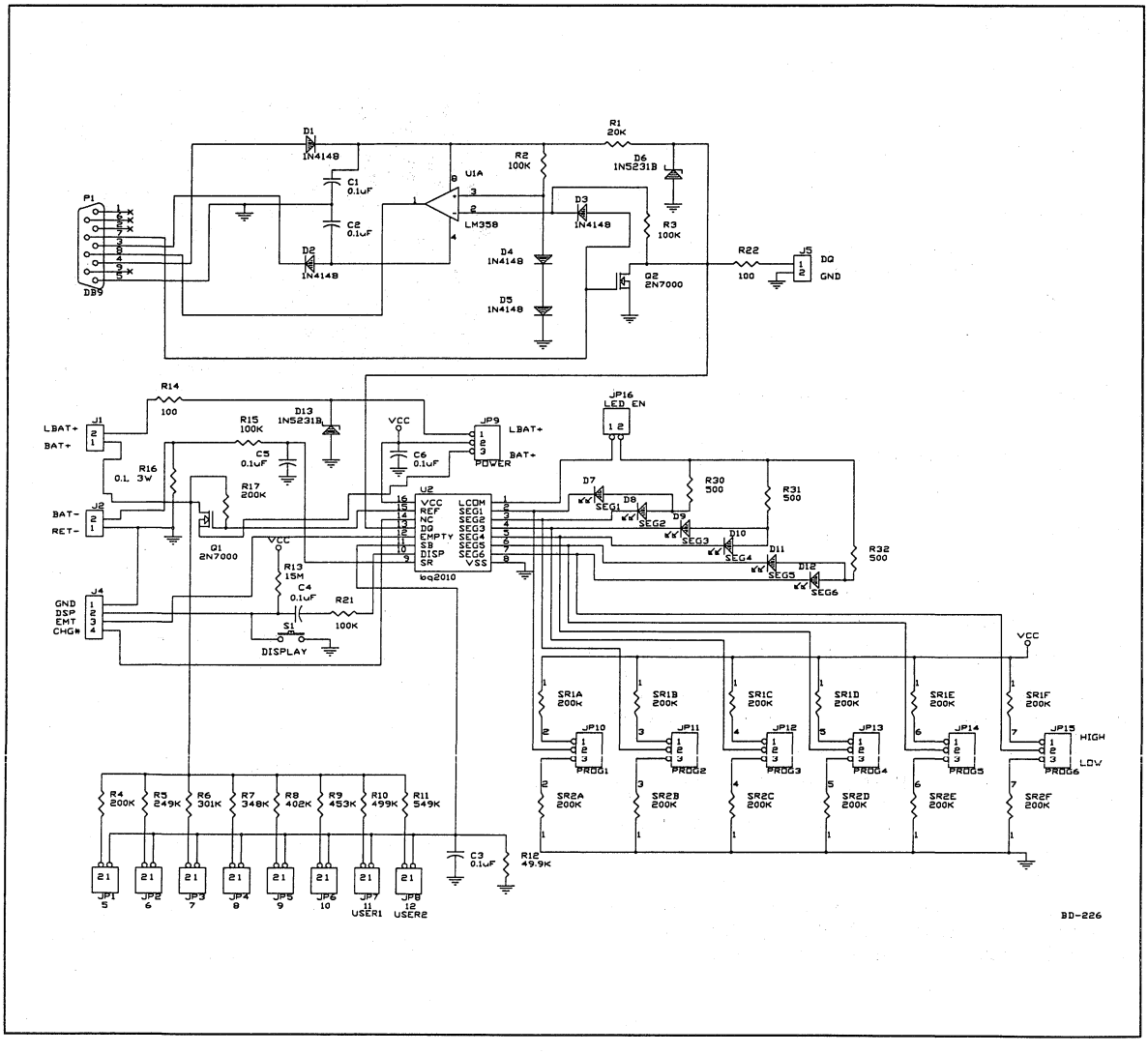
1 RS-232 cable harness

1 User's guide

1 Software diskette containing:

a) EV2010.EXE menu programming for data logging and characterization
b) AP10A.EXE register access program
c) AP10A.C source code

EV2010 Schematic



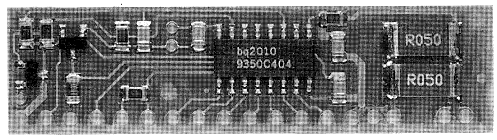
BENCHMARQ

bq2110-KT

Gas Gauge Module Kit

Features

- Complete bq2010 Gas Gauge solution for 5- to 12-cell NiCd or NiMH pack
- RS-232 interface board for easy access to state-of-charge information via the serial port
- Battery state-of-charge monitoring customized for 5- to 12-cell (series) applications (contact Benchmarq for 3, 4, or greater than 12 cells)
- 6 LED output contacts for state-of-charge information display



General Description

The bq2110 Gas Gauge Module Kit provides a complete solution for the bq2010 Gas Gauge IC. The bq2110 incorporates a bq2010, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 5 to 12 series NiCd or NiMH cells. Wires can be provided for direct connection to the battery pack, the empty output from the bq2010, and the DISP display control input to the bq2010. Please refer to the bq2010 data sheet for device specifications.

Contents

1	bq2110 module with bq2010 SOIC
1	EV2010 Software Diskette
1	Documentation kit containing user's guide, schematics, and data sheets
1	RS-232 cable and RS-232 interface board

bq2110 Module Configuration—Complete Before Ordering

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of battery cells (5—12) _____

Sense resistor size in Ω (0.1Ω standard) _____

Sense resistor type:

SMT (1W) or through hole (3W) _____

Battery capacity (mAh) _____

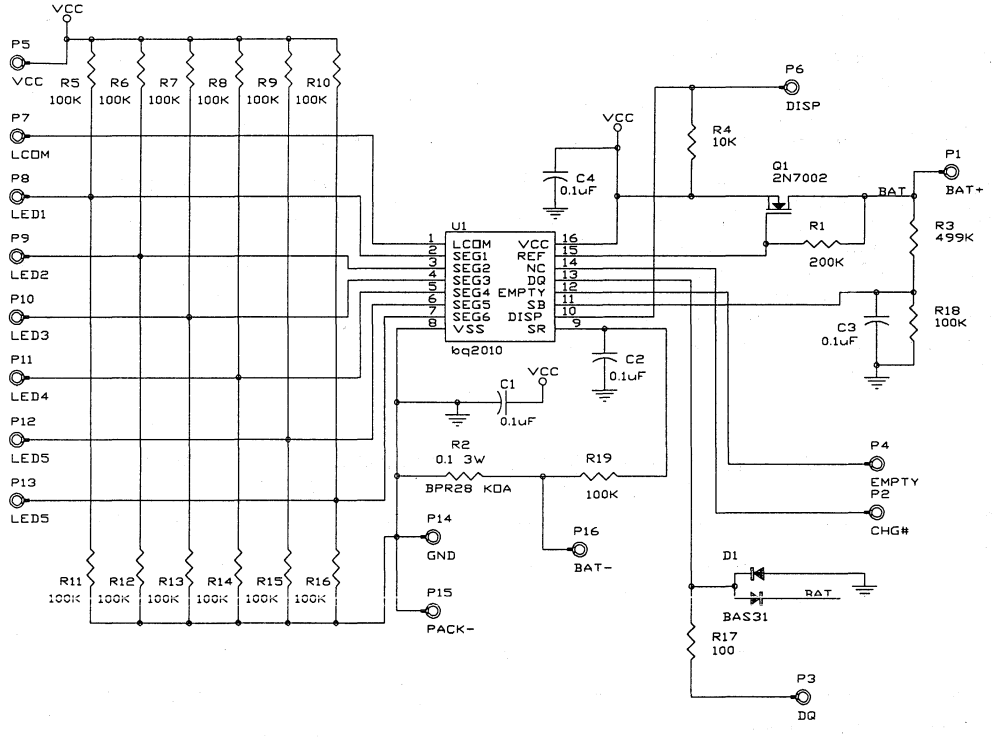
Battery type (NiCd or NiMH) _____

Display mode (absolute or relative) _____

Display type (LED or serial) _____

PB-0010

bq2110 Schematic



BENCHMARQ

Using the bq2010

A Tutorial for Gas Gauging

Introduction

This tutorial introduces the bq2010 Gas Gauge IC (secondary battery available charge monitor). The tutorial is intended to be used with the bq2010 data sheet by engineers and managers designing with or evaluating the bq2010.

The bq2010 Gas Gauge IC is a complete battery monitoring product for NiMH and NiCd batteries. The bq2010 16-pin SOIC provides significant advantages:

- A complete single-chip system solution for in-the-pack monitoring of a battery's available charge
- No battery technology expertise required; the bq2010 is already optimized for NiMH or NiCd use, based on Benchmarq's extensive research on battery characteristics
- Minimal engineering required, typically a single PCB layout specific to the application
- No software required for stand-alone battery-pack applications
- Single-wire serial interface for communication with an external processor to implement a customized display
- Direct LED display drive

This tutorial describes capacity monitoring, compares Benchmarq's gas gauge solutions to microprocessor-based implementations, describes device operation in general terms, and addresses implementation issues.

Available Charge Monitoring

Rechargeable batteries are used in many different applications, from cellular phones, portable computers, and medical equipment to power tools. The operating environment of these batteries covers a wide range of temperatures; therefore, battery efficiency changes due to battery temperature and rate of charge or discharge. The bq2010 compensates for both temperature and charge/discharge rate continuously.

The battery available charge can be displayed on LEDs and is also available via the serial port. The calculated available charge of the battery is also compensated according to battery temperature because the actual available charge is reduced at lower temperatures. For example, if the bq2010 indicates that the battery is 60% full at a temperature of 25°C, then the bq2010 indicates 40% full when cooled to 0°C, which is the predicted available charge at that temperature. When the temperature returns to 25°C, the displayed capacity returns to 60%. This ensures that the indicated capacity is always conservatively representative of the charge available for use under the given conditions.

The bq2010 also adjusts the available charge for the approximate internal self-discharge that occurs in NiCd or NiMH batteries. The self-discharge adjustment is based on the selected rate, elapsed time, battery charge level, and temperature. This adjustment provides a conservative estimate of self-discharge that occurs naturally and that is a significant source of discharge in systems that are not charged often or are stored at elevated temperatures.

Comparing bq2010 Solution With MCU-Based Implementations

Low-power, single-chip microprocessors such as those available from Motorola, Toshiba, NEC, and others have been used to implement gas gauges in battery-powered equipment, notably camcorders and laptop computers. Although adequate, these implementations require extensive development efforts to be suitable for use in a battery pack, and even then, require significant space in the pack because of the high component count.

The bq2010 by comparison offers efficiency, ease of use, simplicity of design, and low component count. With careful PCB layout, the bq2010 system can fit in the space between AA batteries. Table 1 compares the bq2010 and a typical MCU gas gauge implementation.

bq2010 Operation

Gas gauging is accomplished by measuring the charge input to and subsequently removed from a battery. This is done by monitoring the voltage drop across a low-value resistor (typically 20 to 100mΩ) during charge and discharge. This voltage is integrated over time, scaled, and used to drive two 16-bit internal counters:

- Nominal Available Charge (NAC) counter—represents the amount of charge available from the battery.
- Discharge Count Register (DCR)—represents the amount of charge removed from the battery since it was last full.

Also, the Last Measured Discharge (LMD) register is an eight-bit register used to store the most recent count value representing "battery full."

In a typical situation, the Benchmarq Gas Gauge ICs are installed in a battery pack containing unconditioned batteries with an unknown charge state.

On application of power to the bq2010, the following assumptions are made:

- The battery is empty; therefore, the NAC is zero.
- The battery's storage capacity is the Programmed Full Count (PFC) as specified by the programming inputs, which are loaded into the LMD.

The actual storage capacity of the battery has yet to be determined. The battery capacity can be learned by charging the battery until NAC = LMD (LMD = PFC on initialization) and then discharging the battery until the cell voltage reaches the End-of-Discharge Voltage (EDV1) threshold (1.05V for the bq2010). As discharge occurs, the bq2010 tracks the amount of charge removed from the battery in the DCR. The new battery capacity (DCR) is transferred to the LMD if no partial charges have occurred, the temperature is above 10°C, and self-discharge accounts for less than 8 to 18% of the DCR when EDV1 was reached. The valid discharge flag (VDQ) in the bq2010 indicates whether the present discharge is valid for LMD update.

Table 1. Comparing bq2010 and MCU Implementations

Feature	MCU Implementation	bq2010 Solution
Small size	>> 1 square inch; requires extra battery pack space	≤ 1 square inch; fits between batteries
Operating current (not including LEDs)	Typically ≥ 1mA awake; as low as 10µA asleep	125µA typical
LED display	Yes	Yes
Serial I/O	Depends on programming	Yes
Programmable capacity	Depends on programming	Yes
Self-discharge	Generally not implemented	Yes, with temperature compensations
Charge, discharge rate compensations	Generally not available but depends on programming	Yes
Charge, discharge temperature compensations	Generally not available but depends on programming; requires a thermistor	Yes, uses internal temperature sensor
Programming requirements	Extensive MCU programming required for gas gauge functions; possible host programming, algorithm development, and software testing	No programming for stand-alone applications; small host code for serial I/O applications
Hardware design requirements	Extensive low-power-design, op amp, analog switch, MCU, resonator, low-power regulator, LEDs, sense resistor; component count = 56 typical	No engineering required; component count = 23 typical: bq2010, nFET, LEDs, sense resistor, programming resistors and capacitors

Discharging Before the First Charge

Most battery pack manufacturers will assemble their packs with the bq2010 and ship them without charging. When the customer receives a new pack, the pack indicates EMPTY, and the customer then charges the pack until it indicates full. Because chargers terminate fast charge on voltage (-ΔV) or temperature (ΔT/Δt) conditions, it is possible that fast charge will terminate before the gas gauge shows full because the available capacity of the battery was not zero.

The battery pack manufacturer may want to instruct the user to discharge the battery to EDVF before charging. Once this condition is reached, the battery can be fast-charged until termination—allowing NAC to count up to LMD. Now, the gas gauge is synchronized with the battery and learns the true battery capacity on the next valid discharge cycle.

For applications with LED displays, the complete discharge of the battery pack is indicated by all LEDs going off. For applications using the serial I/O port, complete discharge is indicated when the final end-of-discharge voltage (EDVF) flag is set.

To ensure that the bq2010 accurately predicts the amount of available charge, battery pack manufacturers should instruct their end-users to completely discharge a new battery pack and then charge it until the charger terminates.

Alternatively, the NAC can be written with an estimated battery capacity during pack assembly or testing. While this may alleviate the problem of fast charge terminating before NAC = LMD, it may give the user a false indication of battery capacity if the value written was inaccurate. Under this scenario, users should fully charge a new battery pack. The actual capacity is "learned" on the next valid discharge.

Using the bq2010

The bq2010 IC is simple to use and implement into a system. Figure 1 shows the bq2010 configured for full functionality. Almost all of the external connections and components are *optional*, as indicated by the dotted lines. For example, most stand-alone applications do not need the EMPTY pin connection or the DQ port (except possibly for testing).

All the external components except perhaps the sense resistor can be surface-mounted. The sense resistor could fit in the space between most battery cells, and the populated PCB may also fit in that space with the correct layout. A bq2010 Gas Gauge IC could, therefore, be added to existing product battery packs with little re-tooling of plastics.

Monitoring the Battery

To determine and track the charge state of the battery, the bq2010 monitors both the divided battery voltage and the voltage drop across the sense resistor.

The divided battery voltage (V_{SB}) is provided by a resistor-divider that divides the battery pack voltage down to a single-cell voltage. V_{SB} is primarily used to determine when the battery has reached the EDV1 threshold so that the new battery capacity determined during discharge may be saved in the LMD. V_{SB} is also used for EDVF determination, battery-removed indication, and battery-replaced indication.

The battery current is monitored using a low-value sense resistor attached to the negative terminal of the battery. The current through the resistor generates a proportional voltage drop, V_{SR}, which is provided to the SR input of the bq2010.

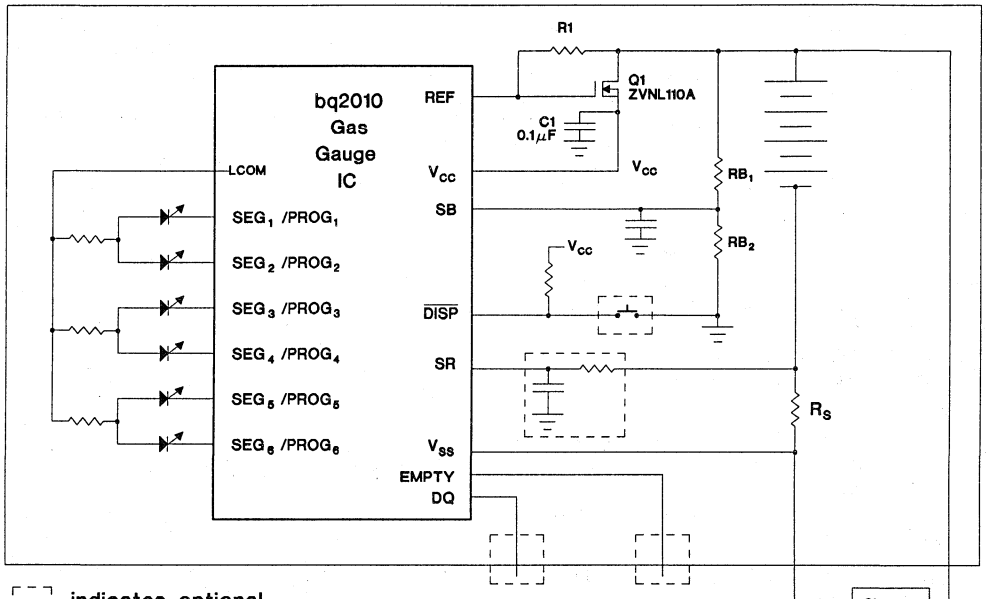
Picking a Sense Resistor

The sense resistor is used to measure the current flowing into or out of the battery. The sense resistor value depends on the currents being measured. The bq2010 specification for V_{SR} ranges from a maximum of 2.0V for charging to -300mV for discharging. The offset error for the bq2010 relative to V_{SR} is ± 150μV.

In general, a sense resistor should be selected so that: (a) the voltage drop across that resistor exceeds 5 to 7mV for the lowest current representing the majority of the battery drain, and (b) the lowest practical V_{SR} voltage drop is achieved to maximize the useful voltage available from the battery pack.

For example, Table 2 summarizes the approximate current requirements for a laptop computer application. The majority of the battery capacity is used in run (no disks) mode. The next largest amount of battery capacity is used in run (with disks) mode, with suspend mode consuming the least amount of battery capacity, even though it makes up the largest block of time.

If a 0.1Ω sense resistor is used, the voltage input to SR is as shown. This means that for both run modes, the integrator repeatability error is a maximum of 2% because $|V_{SR}|$ is well above 30mV. Although the repeatability error associated with suspend mode is approximately 5%, its total error contribution is only 0.5% because suspend mode is responsible for only 10% of the total consumption.



[ ] indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 5.6V nominal) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of >4 cells. The value of R1 depends on the number of cells.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required, application-specific.

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Figure 1. bq2010 Application Diagram—LED Display

Table 2. Approximate Laptop Computer Current Requirements

Mode	Current (A)	0.1Ω Voltage Drop (mV)	Time (min.)	% of Battery Usage
Run (with disks)	1	100.0	20	16.7
Run (no disks)	0.5	50.0	175	72.9
Suspend	0.05	5	250	10.4

Selecting PFCs

When the bq2010 is first connected to the battery pack, a Programmed Full Count (PFC) representing the initial full battery capacity is loaded into the LMD. To select this PFC, determine the initial full battery capacity value in mVh by multiplying the manufacturer's battery capacity rating in mAh by the sense resistor value:

$$mVh = mAh * R_{SNS}$$

Find the nearest corresponding value in Table 3 that is *less than* the calculated mVh value, and then set the programming pin levels to select the Programmed Full Count (PFC), scale, and scale multiplier associated with that value.

Nine PFC settings are available using $PROG_1$ and $PROG_2$, which together with scale ($PROG_3$ and $PROG_4$) settings provide a wide range of initial full battery values. ($PROG_5$ is used to select the self-discharge compensations for either NiMH or NiCd batteries; $PROG_6$ is used to determine the display mode of the bq2010 as described on page 6.)

For example, if a 0.1Ω sense resistor is being used, and the battery is rated at 1100mAh, then the initial full battery value is 110mVh. The nearest available value that is less than 110mVh from Table 3 is 106mVh, which corresponds to $PROG_1$ = Z, $PROG_2$ = Z, $PROG_3$ = L, and $PROG_4$ = L.

Note that some cells in Table 3 have identical initial full battery values. For example, 141mVh can be found two places:

- Example 1: $PROG_1$ = L, $PROG_2$ = L, $PROG_3$ = Z, $PROG_4$ = L = 141mVh
- Example 2: $PROG_1$ = H, $PROG_2$ = Z, $PROG_3$ = L, $PROG_4$ = L = 141mVh

Example 1 corresponds to a PFC of 22528 of 65535 possible counts (34.4%). This means that, in all likelihood, a majority of the counter range will remain unused. Counter resolution could be increased by using the settings in example 2. In this case, the PFC is 45056 of 65535 counts (68.8% of range). In general, when faced with a choice, it is better to pick the finer resolution (that is, a larger PFC).

$PROG_3$ and $PROG_4$ inputs determine the scale to be used by the bq2010. Together these two pins determine the mVh value of a single NAC count. Thus, for any given PFC selected by $PROG_1$ and $PROG_2$, the capacity represented by that PFC (in mVh) is given by:

$$PFC * scale$$

Note that the scale value is given for a $PROG_3$, $PROG_4$ pair at the top of each column in Table 3.

Table 3. bq2010 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2-	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh

Using the Programming Pins

The bq2010 is programmed through the LED display pins during a special programming cycle that occurs during power-up or during a device reset.

Programming Without LED Display

In applications where the LED display is not used, programming is very simple. The bq2010 may be programmed by tying each programming pin directly to the appropriate level:

H = V_{CC}

Z = open

L = V_{SS}

LED outputs must be disabled by tying $\overline{DISP}$ to V_{CC}. LCOM may remain open.

Programming With LED Display

When the LED display is used, it is necessary to provide programming information with either a pull-up resistor to V_{CC}, a pull-down resistor to V_{SS} (200KΩ value in either case), or no resistor at all. The logic states are set as follows:

H ≤ 200K to V_{CC}

Z = no resistor

L ≤ 200K to V_{SS}

LCOM must be used to provide power to the LEDs so that they may be disabled during reading of the programming resistors (see Figure 1).

Selecting Battery Chemistry

$PROG_5$ is used during power-up to select self-discharge compensations for either NiMH or NiCd batteries. $PROG_5$ = Z for NiCd and L for NiMH batteries.

Using the LED Display

The bq2010 supports 6 LEDs that display a gauge of available battery charge. LEDs 1 through 5 provide 20% step indication of charge, while the sixth LED indicates "overfull" when the display is operating in absolute mode ($PROG_6$ = Z).

Selecting Display Mode

$PROG_6$ is used during power-up to determine the display mode of the bq2010. The bq2010 uses either absolute or relative battery charge state as described below ($PROG_6$ = Z or L, respectively).

The display indicates available battery charge as a percentage of "battery full." This is based on the current LMD value ("relative" mode) or on the PFC value (the initial battery capacity value programmed, "absolute" mode). Relative mode is for applications where the customer does not want to see on the display the decline in battery capacity following many charge/discharge cycles. Absolute mode is for applications when the customer wants each segment to represent a fixed amount of charge.

Display Activation

The LED display is normally maintained in the OFF state to conserve battery power. It is activated during a high rate of battery charge and discharge if $\overline{DISP}$ is floating, or continuously if the $\overline{DISP}$ pin is pulled to V_{SS}. When the display is not used, the $\overline{DISP}$ pin can be tied to V_{CC} to disable the display and allow the pins to be used strictly as programming pins.

LED Supply

The current source for the LEDs is provided through the LCOM pin in all applications, because the programming inputs and the LED outputs share common pins. When the bq2010 is initially powered-up, the LCOM output is disabled, thus allowing the pins to be sensed for the presence of programming resistors tied to V_{CC} or V_{SS} (see Figure 1).

Standard LEDs such as the Sharp PR series should provide adequate performance at low cost. For better results, customers could use a high-brightness LED (low current) such as the more expensive Sharp LR or UR series. The suitability of any particular LED depends not only on its luminosity at rated current, but also the packaging and lensing technique used (very important in concentrating viewable energy, especially for high-ambient-light conditions).

Using the DQ Serial Port

The bq2010 is also equipped with a bidirectional single-line serial I/O port (DQ) that allows it to conveniently communicate with a host processor.

Data Interface

The DQ serial port allows the implementation of gas gauge functions without the need for the LED display. For example, in cellular telephone and laptop computer applications, the LED display is not needed because an LCD is available. The host processor in these cases can simply obtain the gas gauge display step and the temperature over the serial port and use these to indicate available charge. The gas gauge step data is a 4-bit value that represents 1 of 16 possible steps (6.25% of full per step), giving a greater possible display accuracy than is possible with the LED display.

In a more sophisticated approach, the host may obtain the NAC, LMD, temperature, and operational status flags, and then use these to customize and display functions and features.

Battery Pack Testing

The DQ serial port is also useful for final testing of assembled battery packs. The bq2010 can be exercised from a host processor over the DQ serial port—allowing the host to directly control the state of the LED output pins and the EMPTY pin. The state of the programming pins may also be checked. A battery ID byte (stored in on-chip RAM) allows the manufacturer to identify battery types.

Using the EMPTY Pin

The EMPTY pin provides external control for automatic load disconnection on low battery, preventing deep discharge. It activates when V_{SB} drops below the EDVF threshold.

Supplying Power to the Part

The V_{CC} specification for the bq2010 is:

$$3.0V \leq V_{CC} \leq 6.5V$$

This may be achieved in several ways under various battery configurations.

Direct Battery Power

The bq2010 may be powered directly from the batteries in configurations of 3 or 4 cells. When using unregulated direct battery power, ensure that the battery voltage does not exceed the maximum of 6.5V or fall below the minimum operational value of 3.0V.

Direct unregulated power supply should be limited to situations where varying or pulsed load conditions during discharge or charge do not cause battery voltage spikes. Such spikes typically result when batteries drive switching power supplies that use inductive storage, or when start-up transients in motors produce significant voltage spikes on the battery.

Low-Cost nFET Regulator

Most applications require some kind of voltage regulator to supply V_{CC} within specifications over a broad range of battery voltage conditions. The bq2010 provides support for a low-cost regulator circuit consisting of an nFET and the on-chip reference voltage V_{REF}.

Across temperature, V_{REF} ranges from 4.5V to 7.5V, given an I_{REF} of 5µA, where:

$$V_{CC} = V_{REF} - V_{GS}$$

where V_{GS} is the gate-source voltage of the nFET, Q1. When the battery voltage drops below V_{REF}, the R1/R_{REF} divider determines V_{CC}. A low-threshold nFET exhibiting a maximum V_{GS} of 0.8 to 1.5V may be adequate for this circuit. An example is the BSS138ZX from Zetex. The correct choice for R_1 is a function of the number of cells in the battery pack. Table 4 lists different values for R_1 for various battery packs.

Table 4. Reference Bias Resistor R_1 Selection

Assuming a Nominal Q1 V_{GS} = 1.5V

Number of Cells	R1 (Ω)
5	33K
6	100K
7	180K
8	240K
9	300K
10	390K
11	430K
12	510K

Split Battery Configurations

When a battery pack contains a large number of cells, the bq2010 may be operated from a small number of cells inside the larger pack. This is possible as long as the current required for LED operation does not significantly reduce the available charge of the small cell cluster relative to the available charge of the other cells in the pack. Generally, it is best not to use the bq2010 display in this configuration.

Notes

BENCHMARQ

bq2011

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow DIP or SOIC

General Description

The bq2011 Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011 is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the PFC and MODE pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

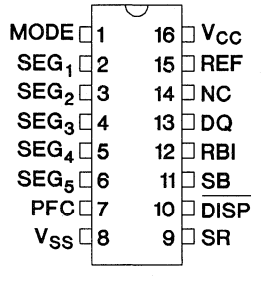
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2011 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011 outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011 gas gauge data registers.

The bq2011 may operate directly from 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-49

Pin Names

MODE	Display mode output	NC	No connect
SEG_1	LED segment 1	DQ	Serial communications input/output
SEG_2	LED segment 2	RBI	Register backup input
SEG_3	LED segment 3	SB	Battery sense input
SEG_4	LED segment 4	$\overline{DISP}$	Display control input
SEG_5	LED segment 5	SR	Sense resistor input
PFC	Programmed full count selection input	V_{CC}	3.0–6.5V
REF	Voltage reference output	V_{SS}	Negative battery terminal

Pin Descriptions

MODE **Display mode output**

When left floating, this output selects relative mode for capacity display. If connected to the anode of the LEDs to source current, absolute mode is selected for capacity display. See Table 1.

SEG_1–SEG_5 **LED display segment outputs**

Each output may activate an LED to sink the current sourced from MODE, the battery, or V_{CC}.

PFC **Programmed full count selection input**

This three-level input pin defines the programmed full count (PFC) thresholds and scale selections described in Table 1. The state of the PFC pin is only read immediately after a reset condition.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor. $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011 is $V_{SR} + V_{OS}$ (see Table 3 on page 8).

NC **No connect**

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ floating allows the LED display to be active during charge and discharge if $V_{SRO} < -1mV$ (charge) or $V_{SRO} > 2mV$ (discharge). Transitioning $\overline{DISP}$ low activates the display for 4 seconds.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI **Register backup input**

This input is used to provide backup potential to the bq2011 registers during periods when $V_{CC} \leq 3V$. A storage capacitor should be connected to RBI.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

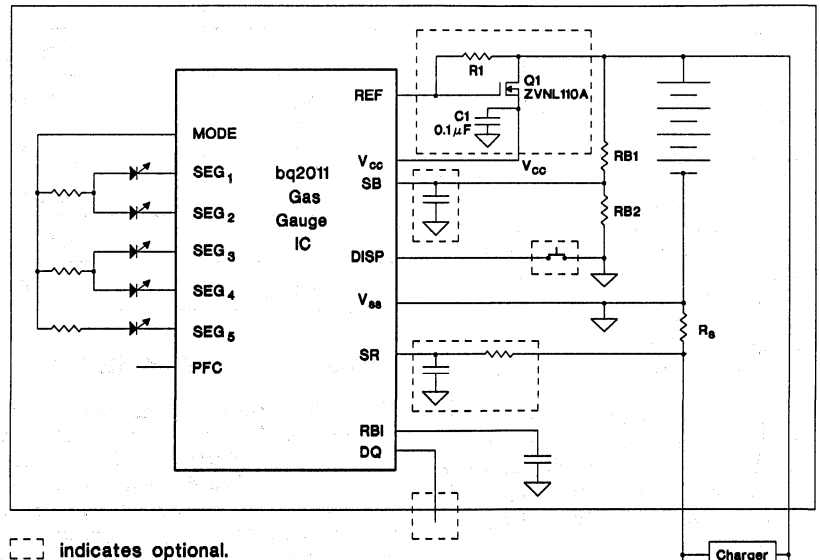
Functional Description

General Operation

The bq2011 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011 using the LED display with absolute mode as a charge-state indicator. The bq2011 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011 monitors the charge and discharge currents as a voltage across a sense resistor (see Rs in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 4 cells (4.8V nominal and should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of > 4 cells.

Programming resistor and ESD-protection diodes are not shown.

R-C on SR may be required (application specific), where the maximum R should not exceed 20K.

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Figure 1. Battery Pack Application Diagram—LED Display, Absolute Mode

Register Backup

The bq2011 RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011 registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011 checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011 are fixed at:

$$V_{EDV} = 0.90V$$
$$V_{MCV} = 2.00V$$

During discharge and charge, the bq2011 monitors V_{SR} for various thresholds, V_{SR1}–V_{SR4}. These thresholds are used to compensate the charge and discharge rates. Refer to the discharge compensation section (page 8) for details. EDV monitoring is disabled if $V_{SR} \geq V_{SR1}$ (50mV typical) and resumes 1 second after V_{SR} drops back below V_{SR1}.

Reset

The bq2011 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described on page 14.

Temperature

The bq2011 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011. The bq2011 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of Vcc or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011 is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

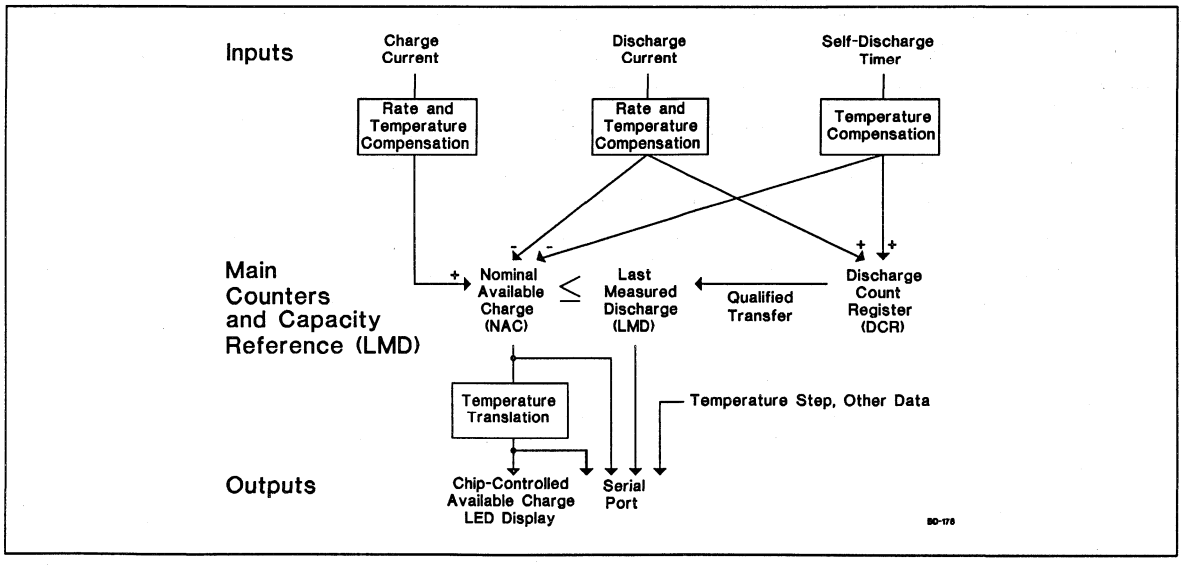


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.005Ω
Number of cells = 6
Capacity = 1300mAh, NiCd cells
Current range = 1A to 80A
Relative display mode
Self-discharge = C/64
Voltage drop over sense resistor = 5mV to 400mV

Therefore:

1300mAh * 0.005Ω = 6.5mVh

Select:

PFC = 34304 counts or 6.5mVh
PFC = Z (float)
MODE = not connected

The initial full battery capacity is 6.5mVh (1300mAh) until the bq2011 "learns" a new capacity with a qualified discharge from full to EDV.

Table 1. bq2011 Programmed Full Count mVh Selections

PFC	Programmed Full Count (PFC)	mVh	Scale	MODE Pin	Display Mode
H	27648	10.5	1/2640	Floating	Relative
Z	34304	6.5	1/5280		
L	44800	8.5	1/5280		
H	42240	8.0	1/5280	Connected to LEDs	Absolute
Z	31744	6.0	1/5280		
L	23808	4.5	1/5280		

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and selfdischarge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

   Note: NAC is set to the value in LMD when SEG_5 is pulled low during a reset.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV} if:

   - No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011 increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011 determines a valid charge activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display becomes inactive after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/64 * NAC rate per day. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot not be decremented below 0.

Count Compensations

The bq2011 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}. The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
$V_{SR} < 50$ mV	1.00	100%
$V_{SR1} > 50$ mV	1.05	95%
$V_{SR2} > 100$ mV	1.15	85%
$V_{SR3} > 150$ mV	1.25	75%
$V_{SR4} > 253$ mV	1.25	75%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 * N)$$

Where N = number of 10°C steps below 10°C and $V_{SR} < 50$mV.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C : N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C : N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C : N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C : N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/64 * NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 2.

Table 2. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	NAC/256
10–20°C	NAC/128
20–30°C	NAC/64
30–40°C	NAC/32
40–50°C	NAC/16
50–60°C	NAC/8
60–70°C	NAC/4
> 70°C	NAC/2

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Table 3. bq2011 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Communicating With the bq2011

The bq2011 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends an eight-bit command byte to the bq2011. The command directs the bq2011 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011 NAC register.

bq2011 Registers

The bq2011 command and status registers are listed in Table 4 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

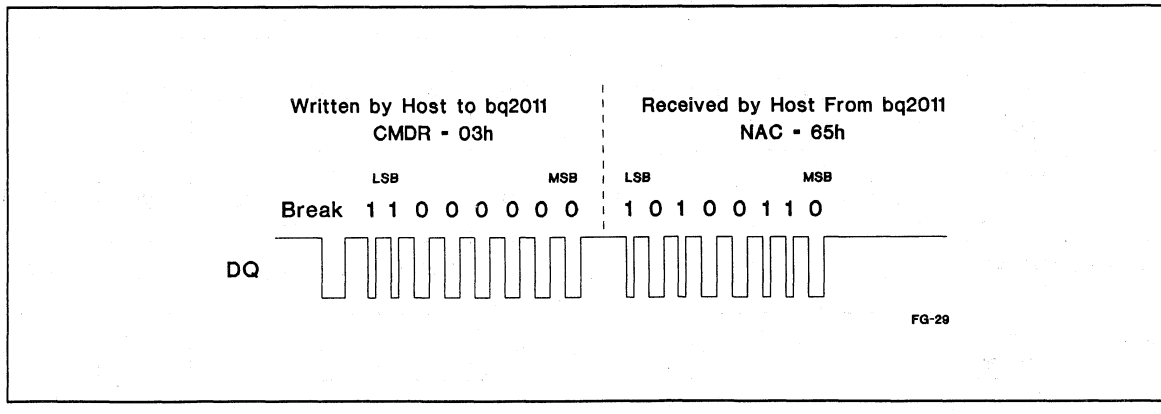


Figure 3. Typical Communication With the bq2011

Table 4. bq2011 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	MCV	CI	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
OCTL	Output control register	0ah	Write	1	OC5	OC4	OC3	OC2	OC1	n/u	OCE
FULCNT	Full count register	0bh	Read	FUL7	FUL6	FUL5	FUL4	FUL3	FUL2	FUL1	FUL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2011 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than- 400µV or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011 is reset (see the RST register description). BRP is latched until either the bq2011 is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 bq2011 is charged until NAC = LMD or discharged until the EDV flag is asserted

1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The ***maximum cell voltage*** flag (MCV) is asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge or the bq2011 is reset

1 After the 64th valid charge action with no LMD updates

The ***valid discharge*** flag (VDQ) is asserted when the bq2011 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with $V_{SRO} < -400\mu V$.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***end-of-discharge warning*** flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if $V_{SR} > V_{SR1}$. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected and $V_{SB} \geq 0.90V$

1 $V_{SB} < 0.90V$ providing that $V_{SR} < V_{SR1}$

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

If SEG_5 = 0 on reset, then NACH = PFC and NACL = 0. If SEG_5 = Z or H, the NACH and NACL registers are cleared to zero, NACL stops counting when NACL reaches zero. When the bq2011 detects a valid charge, NACL resets to zero; *writing to the NAC register affects the available charge counts and, therefore, affects the bq2011 gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011 uses as a measured full reference. The bq2011 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011 updates the capacity of the battery. LMD is set to PFC during a bq2011 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the present discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} < 50mV
0	0	1	50mV < V_{SR} < 100mV (overload, OVLD=1)
0	1	0	100mV < V_{SR} < 150mV
0	1	1	150mV < V_{SR} < 253mV
1	0	0	V_{SRD} > 253mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SRD} > 50mV. OVLD remains asserted as long as the condition persists and is cleared when V_{SRD} < 50mV.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any discharge action other than self-discharge allows detection of another full occurrence during the next valid charge action.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 4 on page 10 for details) is output onto the segment pins, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011 to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011 as explained below. **Note:** Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed,*** *and results in improper operation of the bq2011.*

Resetting the bq2011 sets the following:

- LMD = PFC
- CPI, VDQ, NAC, and OCE = 0 or NAC = LMD when SEG5 = L
- CI and BRP = 1

Display

The bq2011 can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the MODE pin for programming the bq2011.

The bq2011 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description on page 12.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -1mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When pulled low, the segment output becomes active for 4 seconds, ±0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is less than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2011 can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011 can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.87	0.90	0.93	V	SB
V_{SR1}	Discharge compensation threshold	20	50	75	mV	SR (see note)
V_{SR2}	Discharge compensation threshold	70	100	125	mV	SR (see note)
V_{SR3}	Discharge compensation threshold	120	150	175	mV	SR (see note)
V_{SR4}	Discharge compensation threshold	220	253	275	mV	SR (see note)
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{MODE}	MODE input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data-retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} > V_{SS} = discharge; V_{SR} < V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	PFC logic input high	V_{CC} - 0.2	-	-	V	PFC
V_{ILPFC}	PFC logic input low	-	-	V_{SS} + 0.2	V	PFC
V_{IZPFC}	PFC logic input Z	float	-	float	V	PFC
I_{IHPFC}	PFC input high current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
I_{ILPFC}	PFC input low current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
V_{OLSL}	SEG_X output low, low V_{CC}		0.1		V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHML}	MODE output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHMODE} = -5.25mA
V_{OHMH}	MODE output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHMODE} = -33.0mA
I_{OHMODE}	MODE source current	-33	-	-	mA	At V_{OHMODE} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	PFC

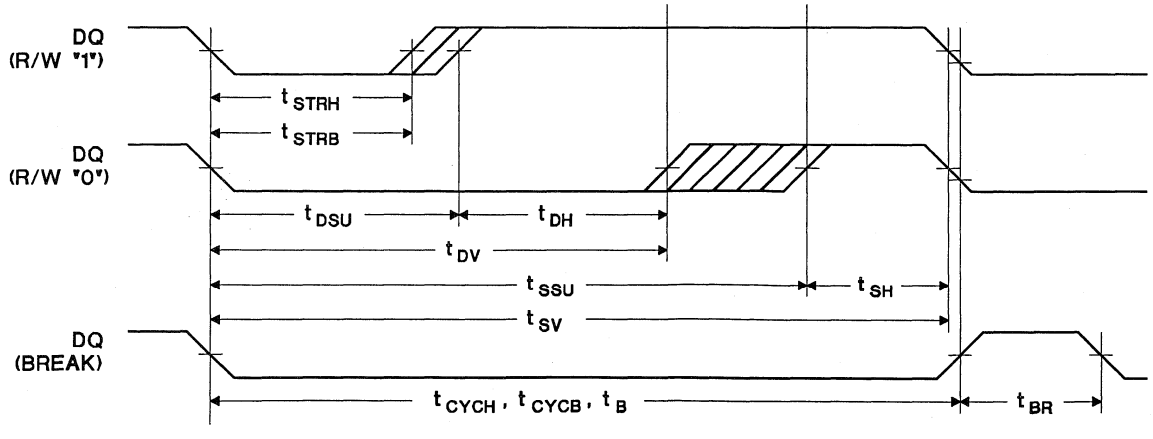
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2011 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2011	5	-	-	ns	
t_{STRB}	Start hold, bq2011 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



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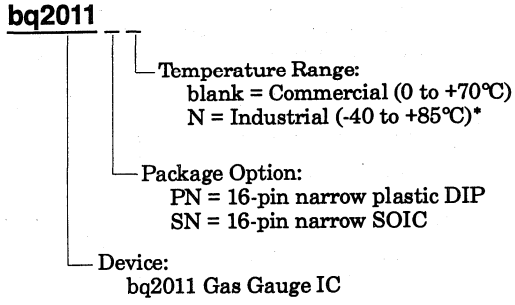
Ordering Information



* Contact factory for availability.

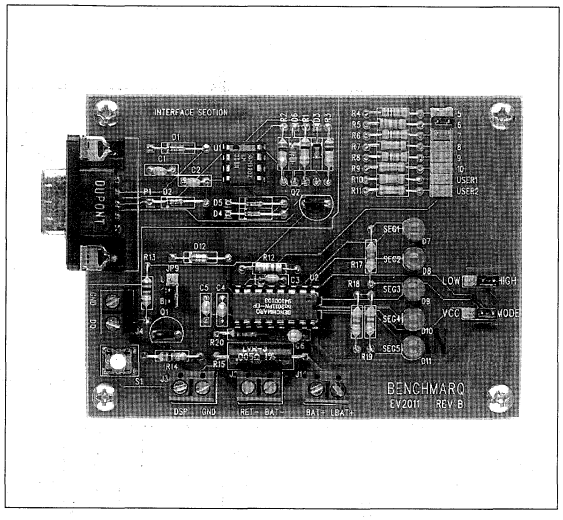
BENCHMARQ

EV2011

bq2011 Evaluation System

Features

- bq2011 Gas Gauge IC evaluation and development system
- RS-232 interface hardware for easy access to state-of-charge information via the serial port
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- On-board regulator for greater than 4-cell applications
- State-of-charge information displayed on bank of 5 LEDs
- Nominal capacity jumper-configurable
- Display mode jumper-configurable



General Description

The EV2011 Evaluation System provides a development and evaluation environment for the bq2011 Gas Gauge IC. The EV2011 incorporates a bq2011, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd cells.

Hardware for an RS-232 interface is included on the EV2011 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2011. Direct connection to the serial port of the bq2011 is also made available for check-out of the final hardware/software implementation.

The menu-driven software provided with the EV2011 displays charge/discharge activity and allows user interface to the bq2011 from any standard DOS PC.

Contents

1 EV2011 printed circuit board containing:

a) bq2011 PDIP IC
b) RS-232 interface hardware
c) On-board regulator
d) Bank of 5 LEDs
e) Sense resistor (0.005Ω)
f) All programming jumpers

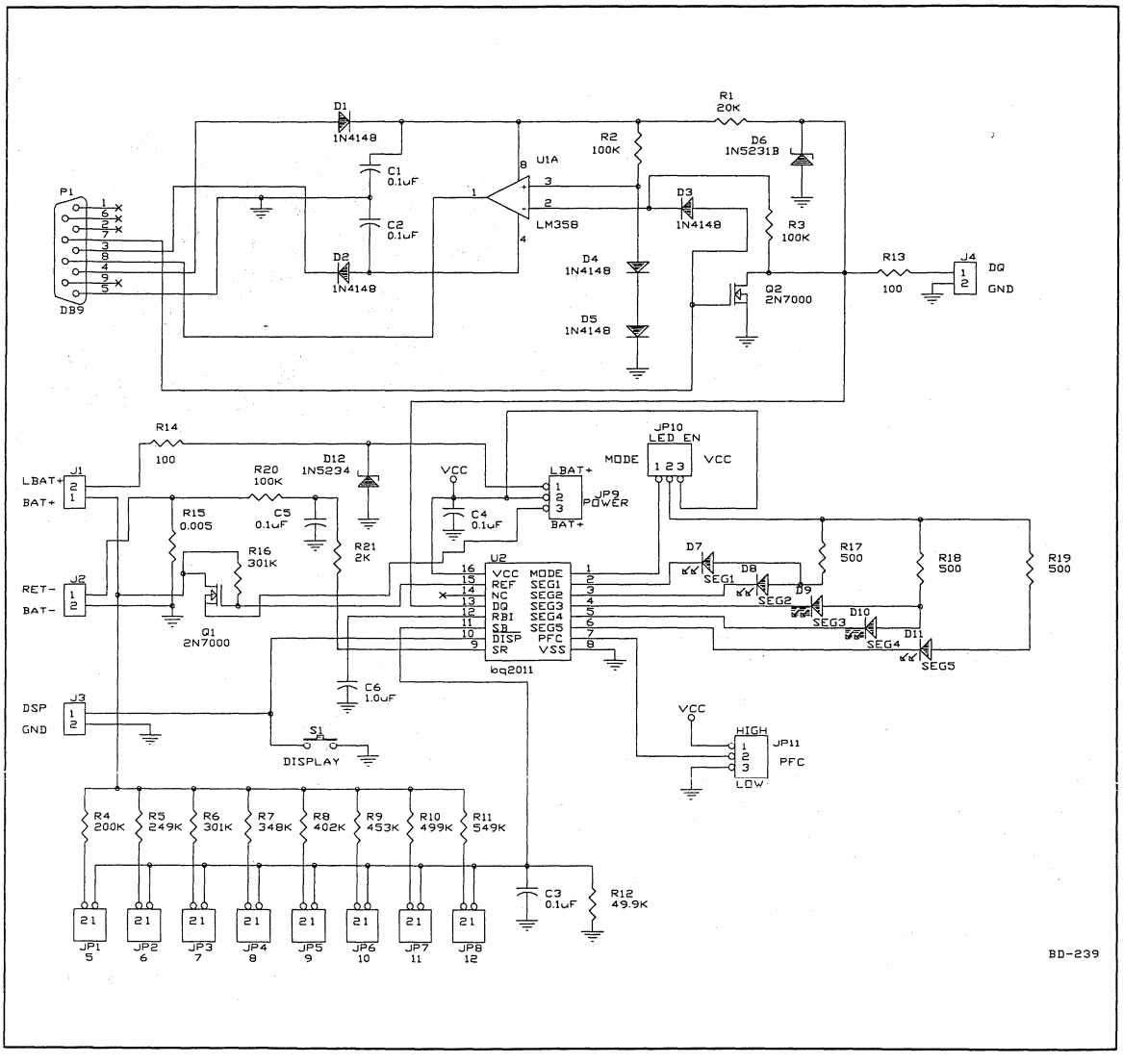
1 RS-232 cable harness

1 User's guide

1 Software diskette containing:

a) EV2011.EXE menu programming for data logging and characterization
b) AP11.EXE register access program
c) AP11.C source code

EV2011 Schematic



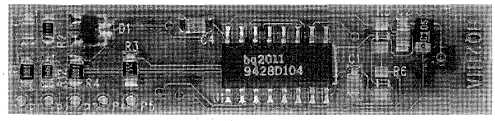
BENCHMARQ

bq2111-KT

Gas Gauge Module Kit

Features

- Complete bq2011 Gas Gauge solution for 4- to 12-cell NiCd pack
- RS-232 interface board for easy access to state-of-charge information via the serial port
- Battery state-of-charge monitoring customized for 4-cell or greater (series) applications
- On-board regulator allows direct connection to the battery
- 5 LEDs for state-of-charge information display



General Description

The bq2111 Gas Gauge Module Kit provides a complete solution for the bq2011 Gas Gauge IC. The bq2111 incorporates a bq2011, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 4 or greater series NiCd cells. Wires can be provided for direct connection to the battery packand external sense resistor. Please refer to the bq2011 data sheet for device specifications.

Contents

1	bq2111 module with bq2011 SOIC
1	EV2011 Software Diskette
1	Documentation kit containing user's guide, schematics, and data sheets
1	RS-232 cable and RS-232 interface board

bq2111 Module Configuration—Complete Before Ordering

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of battery cells _____

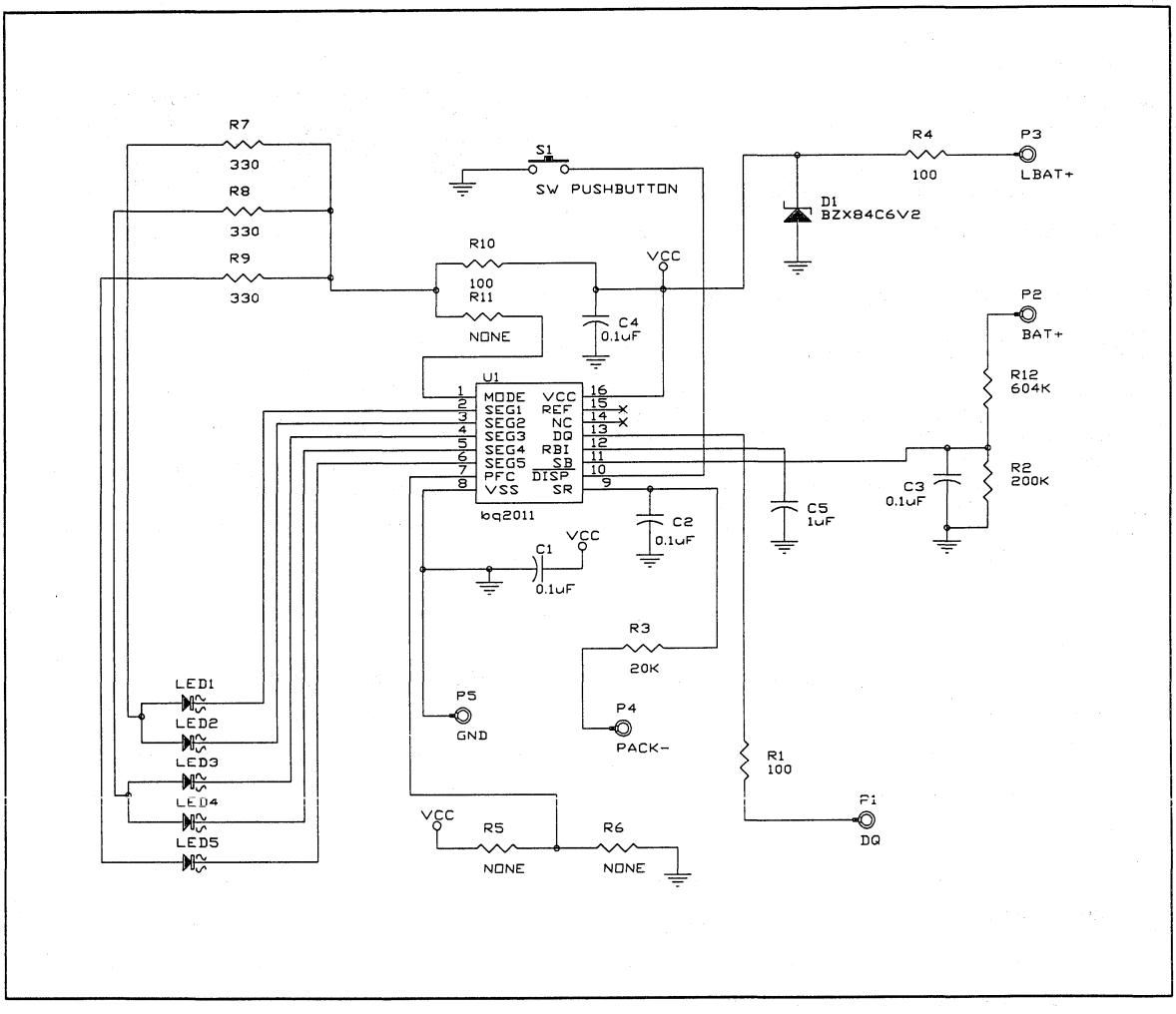
Ext. sense resistor size (0.005Ω standard) _____

Battery capacity (mAh) _____

Display mode (absolute or relative) _____

Display type (LED or serial) _____

bq2111 Schematic



bq2012

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow DIP or SOIC

General Description

The bq2012 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

The bq2012 includes a charge control output that, when used with other full-charge safety termination methods, can provide a cost-effective means of controlling charge based on the battery's charge state.

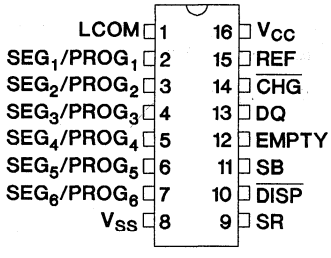
Nominal available charge may be directly indicated using a five- or six-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2012 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2012 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2012 gas gauge data registers.

The bq2012 may operate directly from 3 or 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-50

Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
$SEG_6/PROG_6$	LED segment 6/ program 6 input
REF	Voltage reference output
$\overline{CHG}$	Charge control output
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	System ground

Pin Descriptions

LCOM **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_6 **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the self-discharge compensation rate shown in Table 1.

$PROG_6$ **Display mode selection (dual function with SEG_6)**

This three-level pin defines the display operation shown in Table 1.

$\overline{CHG}$ **Charge control output**

This open-drain output becomes active low when charging is allowed. Valid charging conditions are described in the Charge Control section on page 7.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop (V_{SRO}) as seen by the bq2012 is $V_{SR} + V_{OS}$ (see Table 5 on page 9).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during a valid charge or during discharge if the NAC register is updated at a rate equivalent to $V_{SRO} \leq -4mV$. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY **Battery empty output**

This open-drain output becomes high-impedance on detection of a valid end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

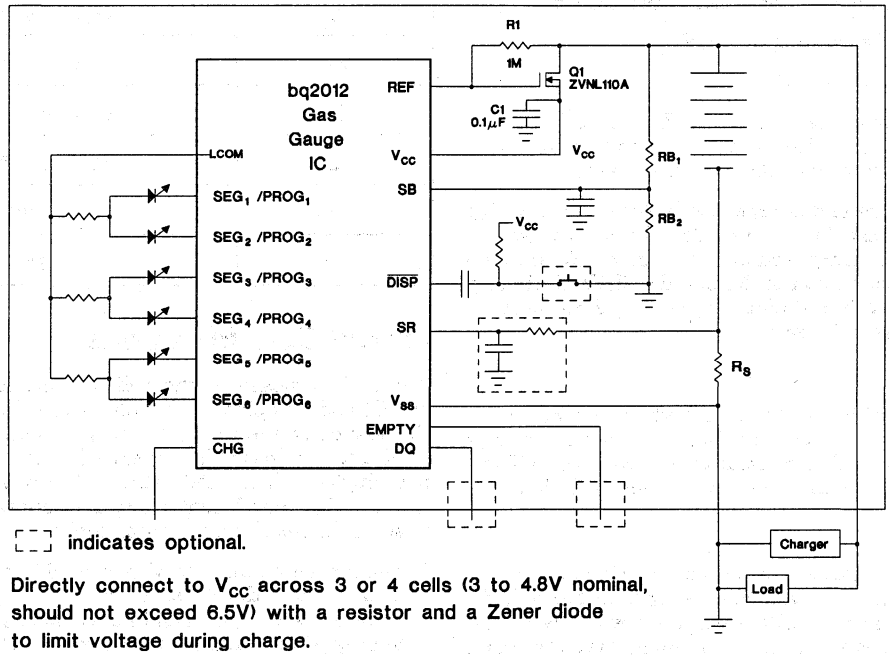
Functional Description

General Operation

The bq2012 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2012 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2012 using the LED display capability as a charge-state indicator. The bq2012 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2012 monitors the charge and discharge currents as a voltage across a sense resistor (see Rs in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 4.8V nominal, should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge.
Otherwise, R1, C1, and Q1 are needed for regulation of >4 cells.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required (application specific), where the R should not exceed 100K.

BD-185

Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2012 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2012 are fixed at:

EDV1 (early warning) = 1.05V

EDVF (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

During discharge and charge, the bq2012 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -250mV typical and resumes ½ second after V_{SR} > -250mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDF}$ and remains latched until a valid charge occurs. The bq2012 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2012 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described on page 14.

Temperature

The bq2012 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2012 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2012.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 100K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2012. The bq2012 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2012 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the programmed full count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The PFC also provides the 100% reference for the absolute display mode. The bq2012 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

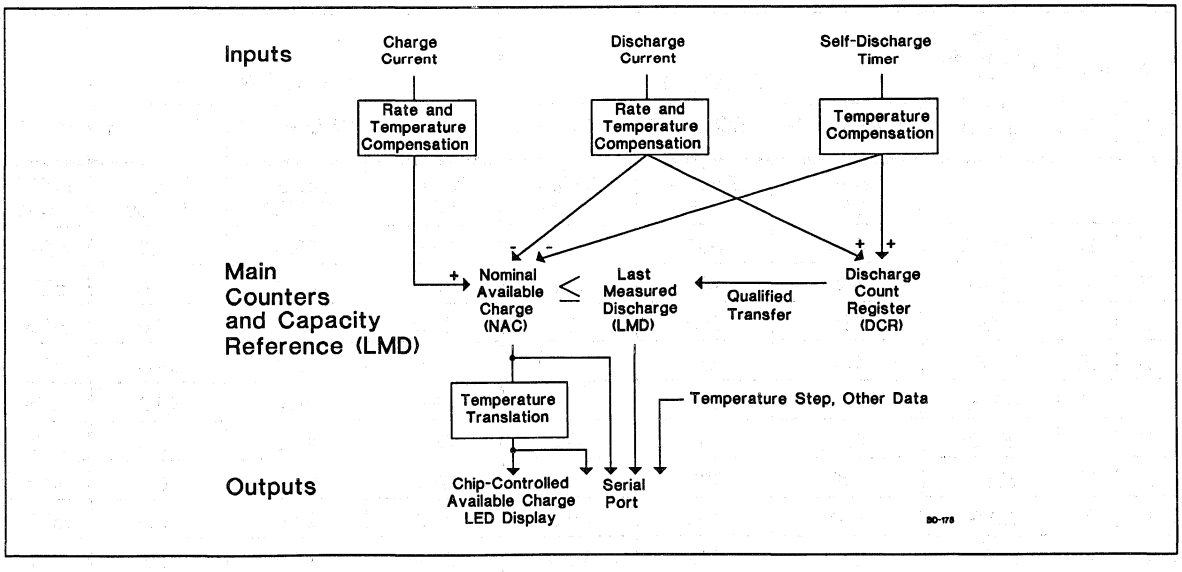


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = C/64
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh * 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2012 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2012 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Display Mode	$\overline{DISP}$ Display State
H	Self-discharge disabled	NAC = PFC on reset	LED disabled
Z	NAC/64	Absolute	LED enabled on discharge when V_{SRO} < -4mV or during a valid charge
L	NAC/47	Relative	LED on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2012 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization ($PROG_6$ = Z or low) and on reaching EDV1. NAC is set to PFC on initialization if $PROG_6$ = high. To prevent overstatement of charge during periods of over-charge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. DCR stops counting when EDV1 is reached. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charge initiations (charges greater than 256 NAC counts; where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2012 increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates the LED display if the rate is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2012 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRQ} is 375µV.

Charge Control

Charge control is provided by the $\overline{CHG}$ output. This output is asserted continuously when:

NAC < 0.94 * LMD and
0.95V < V_{SB} < 2.25V and
0°C < Temp < 50°C and
BRM = 0

This output is asserted at a 1/16 duty cycle (low for 0.5 sec and high for 7.5 sec) when the above conditions are not met and:

NAC < LMD and
0.95V < V_{SB} < 2.25V and
Temp < 50°C and
BRM = 0

This output is also asserted at a 1/16 duty cycle (low for 0.5 sec and high for 7.5 sec) for a 2-hour top-off period after:

NAC = LMD and
Temp < 50°C and
0.95V < V_{SB} < 2.25V and
BRM = 0

This output is inactive when:

NAC = LMD (after a 2-hour top-off period) or
Temp > 50°C or
V_{SB} < 0.95V or
V_{SB} > 2.25V or
BRM = 1

The top-off timer (2 hours) is reset to allow another top-off after the battery is discharged to 0.8 * LMD ($PROG_6$ = L) or 0.8 * PFC ($PROG_6$ = Z or H).

Caution: The charge control output ($\overline{CHG}$) should be used with other forms of charge termination such as ΔT/Δt and -ΔV.

If charge terminates due to maximum temperature, the battery temperature must fall typically 10°C below 50°C before the charge output becomes active again.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2012 continuously decrements NAC and increments DCR for self-discharge based on time and

temperature. The self-discharge count rate is programmed to be a nominal 1/64 * NAC or 1/47 * NAC per day or disabled as selected by $PROG_5$. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2012 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge are compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}. The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

$$\text{Comp. factor} = 1.0 + (0.05 * N)$$

Where N = Number of 10°C steps below 10°C and $-150mV < V_{SR} < 0$.

For example:

T > 10°C	: Nominal compensation, N = 0
0°C < T < 10°C	: N = 1 (i.e., 1.0 becomes 1.05)
-10°C < T < 0°C	: N = 2 (i.e., 1.0 becomes 1.10)
-20°C < T < -10°C	: N = 3 (i.e., 1.0 becomes 1.15)
-20°C < T < -30°C	: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/64 * NAC or 1/47 * NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	$PROG_5$ = Z or H	$PROG_5$ = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2010 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see DCR description, page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2012

The bq2012 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2012 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2012 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends an eight-bit command byte to the bq2012. The command directs the bq2012 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2012 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2012. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2012 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2012 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2012 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2012 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2012 NAC register.

bq2012 Registers

The bq2012 command and status registers are listed in Table 6 and described in the following sections.

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Table 6. bq2012 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	$\overline{CHG}$	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

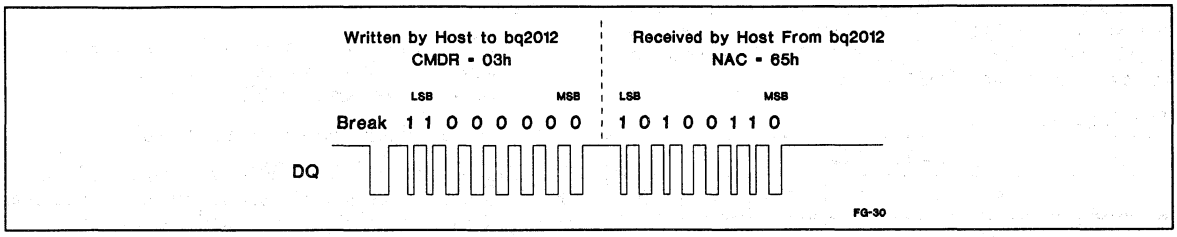


Figure 3. Typical Communication With the bq2012

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2012. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2012 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2012 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2010 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1 V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2012 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates

The ***valid discharge*** flag (VDQ) is asserted when the bq2012 is discharged from NAC = LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***charge control*** flag, $\overline{CHG}$, is asserted whenever the $\overline{CHG}$ pin is asserted (see the charge control section on page 7 for a description of the $\overline{CHG}$ pin function).

The $\overline{CHG}$ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	$\overline{CHG}$	-	-

Where $\overline{CHG}$ is:

0 When the $\overline{CHG}$ pin is asserted active low, signifying that the bq2012 is in a state to allow charge activity.

1 When the $\overline{CHG}$ pin is high-impedance, signifying that no charge activity should take place.

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDV1. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 register description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2012 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown in Table 7.

The bq2012 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2012. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. When the bq2012 detects a valid EDV1, NACH and NACL are reset to 0. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2012 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2012. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2012 uses as a measured full reference. The bq2012

adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2012 updates the capacity of the battery. LMD is set to PFC during a bq2012 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2012 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -250mV. OVLD remains asserted as long as the condition persists and is cleared when V_{SR} > -250mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination. Sampling is re-enabled 0.5 secs after the overload condition is removed.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2012. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2012. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2012 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected if NAC < 0.94 * LMD. When NAC ≥ 0.94 * LMD, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC is discharged below 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2010. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2012 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2012.*

Resetting the bq2012 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: NACH = PFC when $PROG_6$ = H.

Display

The bq2012 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2012 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD. The sixth segment is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC, with the sixth segment representing "overfull" (charge above the PFC). As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description on page 13.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-6} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to V_{SRO} < -4mV or V_{SRO} > V_{SRQ}. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2012 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2012, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2012 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2012 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, $V_{SR} + V_{OS}$ (see note 2)
V_{ORD}	Overload threshold	-230	-250	-280	mV	SR, $V_{SR} + V_{OS}$
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Notes:
1. Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance.
2. Proper threshold measurements require V_{CC} to be more than 1.5V greater than the desired signal value.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	Battery input	-	-	2.4	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEGx output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEGx output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEGx sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ, EMPTY, $\overline{CHG}$
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

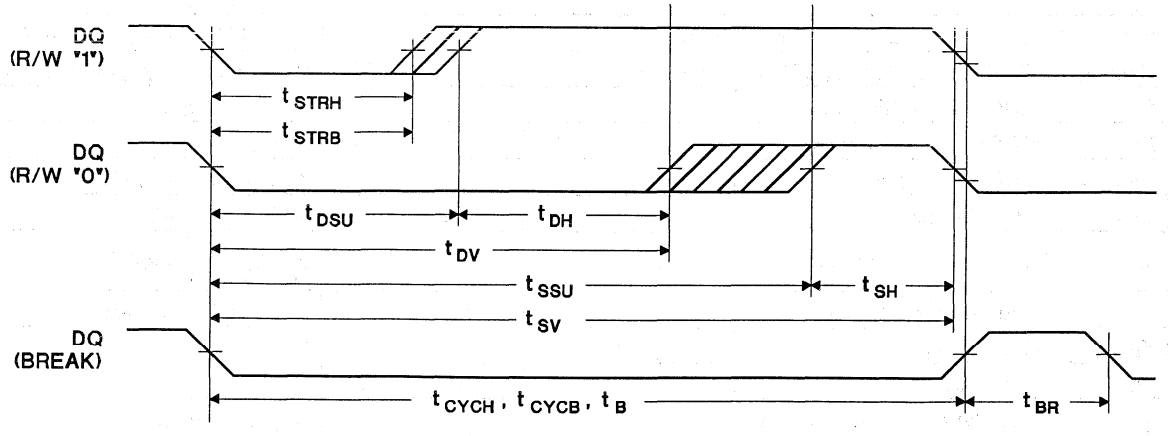
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2012	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2012 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2012	5	-	-	ns	
t_{STRB}	Start hold, bq2012 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

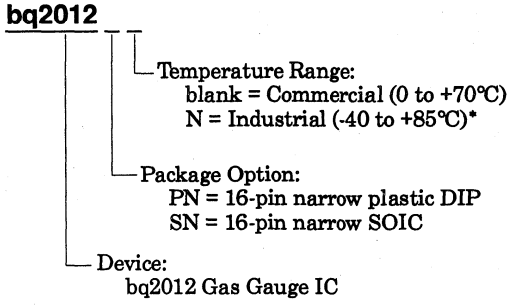
Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



RC-34

Ordering Information



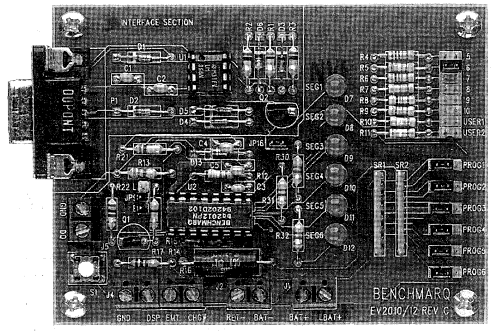
* Contact factory for availability.

EV2012

bq2012 Evaluation System

Features

- bq2012 Gas Gauge IC evaluation and development system
- RS-232 interface hardware for easy access to state-of-charge information via the serial port
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- On-board regulator for greater than 4-cell applications
- State-of-charge information displayed on bank of 6 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable
- Display mode jumper-configurable



General Description

The EV2012 Evaluation System provides a development and evaluation environment for the bq2012 Gas Gauge IC. The EV2012 incorporates a bq2012, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd or NiMH cells.

Hardware for an RS-232 interface is included on the EV2012 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2012. Direct connection to the serial port of the bq2012 is also made available for check-out of the final hardware/software implementation.

The menu-driven software provided with the EV2012 displays charge/discharge activity and allows user interface to the bq2012 from any standard DOS PC.

Contents

1 EV2012 printed circuit board containing:

a) bq2012 PDIP IC
b) RS-232 interface hardware
c) On-board regulator
d) Bank of 6 LEDs
e) Sense resistor (0.1Ω)
f) All programming jumpers

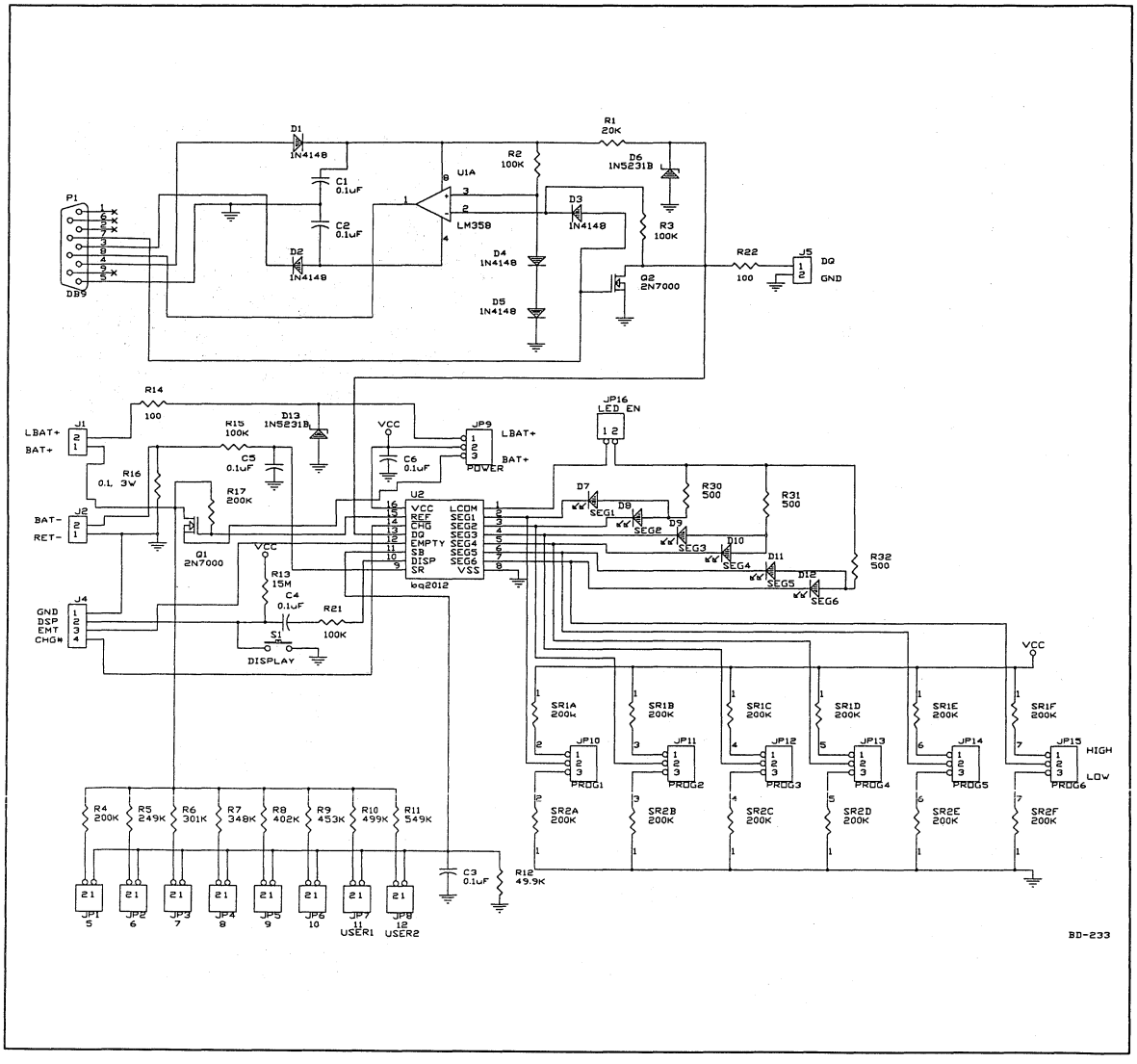
1 RS-232 cable harness

1 User's guide

1 Software diskette containing:

a) EV2012.EXE menu programming for data logging and characterization
b) AP12.EXE register access program
c) AP12.C source code

EV2012 Schematic



BENCHMARQ

bq2014

Gas Gauge IC With External Charge Control

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output operates an external charge controller such as the bq2004 Fast Charge IC
- Designed for battery pack integration
  - 120µA typical standby current
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- User-selectable end-of-discharge threshold
- Battery voltage, nominal available charge, temperature, etc. available over serial port
- 16-pin narrow DIP or SOIC

General Description

The bq2014 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

The bq2014 includes a charge control output that controls an external Fast Charge IC such as the bq2004.

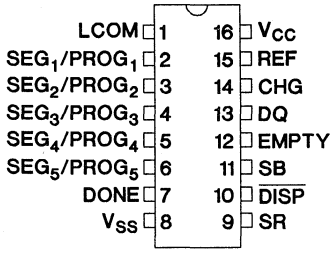
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2014 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2014 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, temperature, capacity, battery voltage, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2014 gas gauge data registers.

The bq2014 may operate directly from 3 or 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-84

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	CHG	Charge control output
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	EMPTY	Empty battery indicator output
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	DISP	Display control input
DONE	Fast charge complete	SR	Sense resistor input
		V_{CC}	3.0–6.5V
		V_{SS}	System ground

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Pin Descriptions

LCOM — **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 — **LED display segment outputs (dual function with $PROG_1$–$PROG_5$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ — **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ — **Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ — **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the self-discharge compensation rate shown in Table 1.

CHG — **Charge control output**

This open-drain output becomes active high when charging is allowed. See page 7 for details.

DONE — **Fast charge complete**

This input is used to communicate the status of an external charge controller such as the bq2004 Fast Charge IC. **Note:** This pin must be pulled down to Vss using a 200KΩ resistor.

SR — **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop (V_{SRO}) as seen by the bq2014 is $V_{SR} + V_{OS}$ (see Table 5 on page 9).

$\overline{DISP}$ — **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during a valid charge or during discharge if the NAC register is updated at a rate equivalent to $V_{SRO} \leq$ -4mV. $\overline{DISP}$ low activates the display. See Table 1.

SB — **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY — **Battery empty output**

This open-drain output becomes high-impedance on detection of a valid final end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ — **Serial I/O pin**

This is an open-drain bidirectional pin.

REF — **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} — **Supply voltage input**

V_{SS} — **Ground**

Functional Description

General Operation

The bq2014 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2014 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2014 using the LED display capability as a charge-state indicator. The bq2014 is configured to display capacity in a relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The LED segments output a percentage of the available charge based on NAC and LMD. A push-button display feature is available for momentarily enabling the LED display.

The bq2014 monitors the charge and discharge currents as a voltage across a sense resistor (see Rs in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

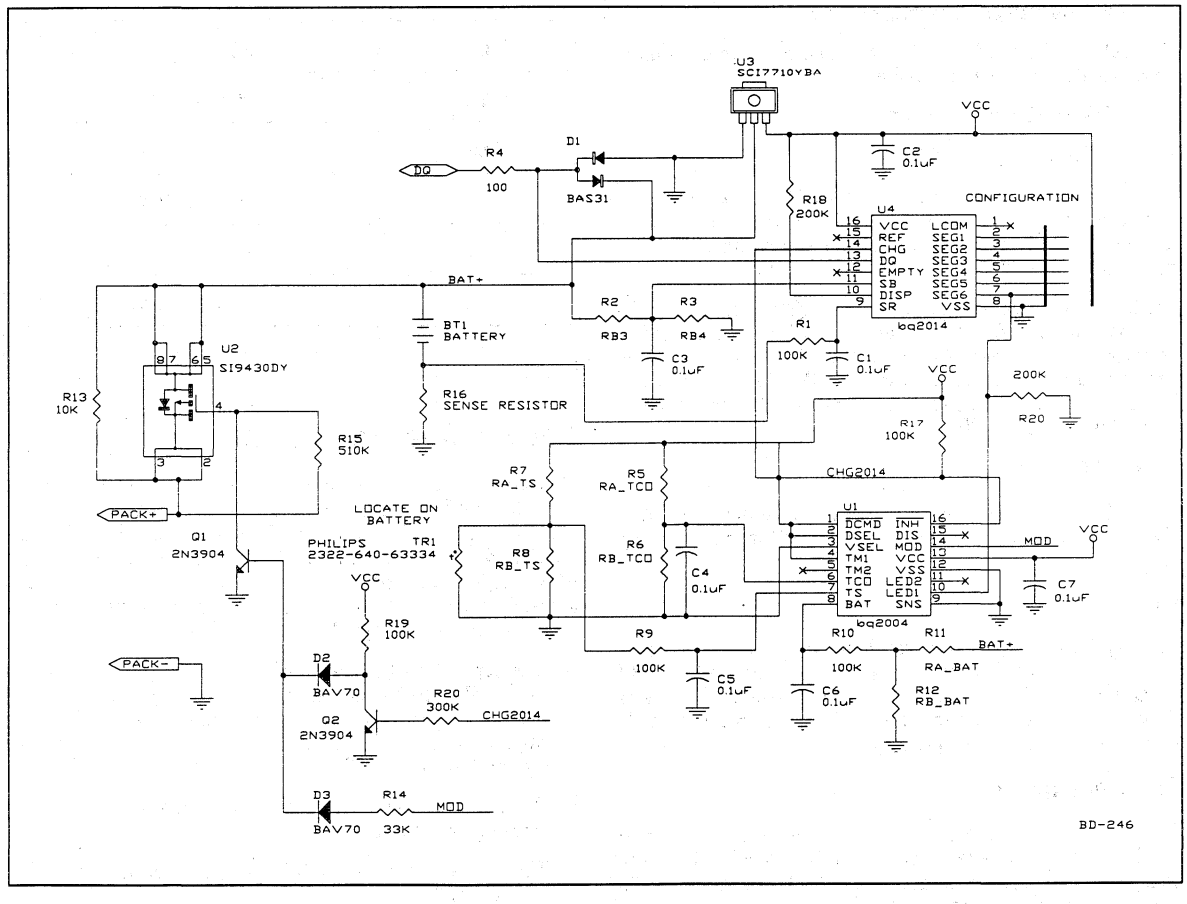


Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2014 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{R2}{R3} = N - 1$$

where N is the number of cells, R2 is connected to the positive battery terminal, and R3 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2014 are programmable with the default values fixed at:

EDV1 (early warning) = 1.05V

EDVF (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2014 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -250mV typical and resumes ½ second after $V_{SR} >$ -250mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDF}$ and remains latched until a valid charge occurs.

Reset

The bq2014 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V (V_{MCV}) resets the device. Reset can also be accomplished with a command over the serial port as described on page 14.

Temperature

The bq2014 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2014 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C2 and C3) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor filter (R1, C1) should be placed as close as possible to the SR pin.
- The sense resistor (R16) should be as close as possible to the bq2014.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2014. The bq2014 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2014 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the programmed full count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2014 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

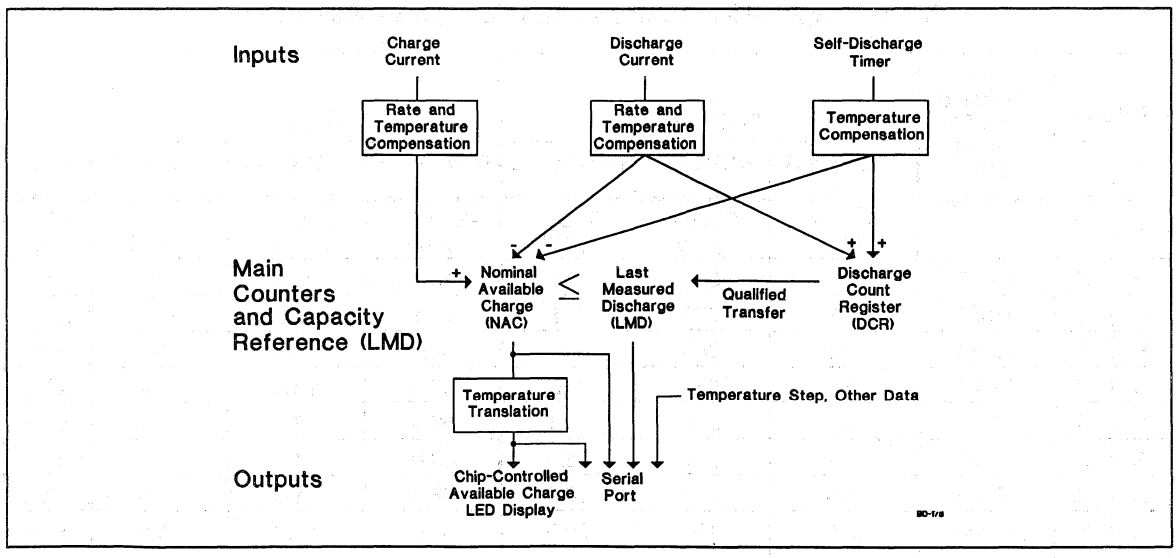


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Relative display mode
Serial port only
Self-discharge = C/64
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh * 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
DONE = low

The initial full battery capacity is 211mVh (2110mAh) until the bq2014 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2014 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$\overline{DISP}$ Display State
H	Disabled	LED disabled
Z	NAC/64	LED enabled on discharge when V_{SRO} < -4mV or during a valid charge
L	NAC/47	LED on

Table 2. bq2014 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and when V_{SB} < EDV1. Tb prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0 until V_{SB} < EDV1. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charge initiations (charges greater than 256 NAC counts; where V_{SRO} > V_{SRQ}) occurred during the period between NAC = LMD and EDV1 detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. The bq2014 determines charge activity sustained at a continuous rate equivalent to V_{SRO} (V_{SR} + V_{OS}) > V_{SRQ}. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold (as described in the Digital Magnitude Filter section) and has a default value of 375µV. If charge activity is detected, the bq2014 increments NAC at a rate proportional to V_{SRO}. If enabled, the bq2014 then activates an LED display. Charge actions increment the NAC after compensation for charge rate and temperature.

Charge Control

Charge control is provided by the CHG output. This output is asserted continuously when NAC > 0.94 * LMD. CHG is also asserted when a valid charge is detected (CHGS in the FLGS1 register is also set). CHG is low when NAC < 0.94 * LMD and there is no valid charge activity.

DONE Input

When the bq2014 detects a valid charge complete with an active-high signal on the DONE input, NAC is set to LMD for $^{NAC}/_{64}$ (NiCd) self-discharge setting. NAC is set to 94% of LMD (if NAC is below 94%) for $^{NAC}/_{47}$ (NiMH) self-discharge setting. VDQ is set when DONE is valid.

Discharge Counting

All discharge counts where V_{SRO} < V_{SRD} cause the NAC register to decrement and the DCR to increment if EDV1 = 0. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2014 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $^1/_{64}$ * NAC or $^1/_{47}$ * NAC per day or disabled as selected by $PROG_5$. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2014 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge are compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}.

The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

$$\text{Comp. factor} = 1.0 + (0.05 * N)$$

Where N = Number of 10°C steps below 10°C and $-150\text{mV} < V_{SR} < 0$.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C : N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C : N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C : N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C : N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/64 * NAC per day, 1/47 * NAC per day, or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2010 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\text{ (mV)} = -45 / \text{DMF}$$

$$V_{SRQ}\text{ (mV)} = -1.25 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see DCR description, page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2014

The bq2014 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2014 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2014 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends an eight-bit command byte to the bq2014. The command directs the bq2014 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2014 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2014. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2014 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2014 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2014 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2014 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2014 NAC register.

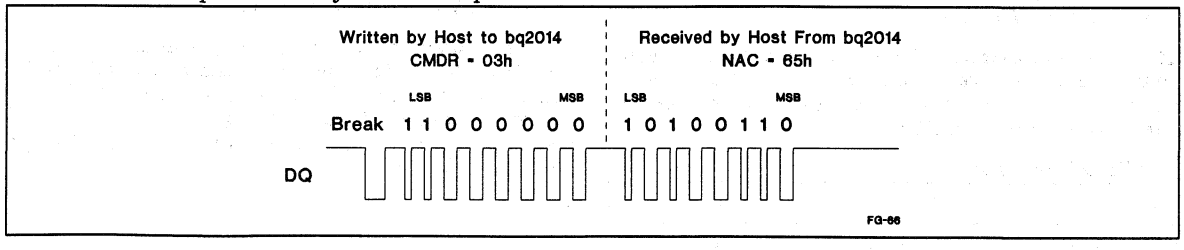


Figure 3. Typical Communication With the bq2014

bq2014 Registers

The bq2014 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2014. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2014 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2014 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2010 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1\ V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2014 is reset. The flag is cleared after an LMD update.

Table 6. bq2014 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0Ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
VSB	Battery voltage	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or when the device is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2014 is discharged from NAC = LMD or DONE is valid. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD or DONE is valid

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery. The EDVF threshold is set 100mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$ - 100mV

1 $V_{SB} < V_{TS}$ - 100mV providing that OVLD=0 (see FLGS2 register description)

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The read/write VTS register sets the EDV1 trip point. EDVF is set 100mV below EDV1. The default value in the VTS register is 75h, representing EDV1 = 1.05V and EDVF = 0.95V. EDV1 = 2.4V * (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register is updated approximately once per second with the present value of the battery voltage. V_{SB} = 2.4V * (VSB/256).

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2014 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

The bq2014 calculates the available charge as a function of NAC, temperature, and LMD. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging registers for the bq2014. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

On reset, NACH and NACL are cleared to 0. When the bq2014 detects a charge, NACL resets to 0. NACH and NACL are reset to 0 when $V_{SB} \leq$ EDV1. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2014 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2014. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2014 uses as a measured full reference. The bq2014 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2014 updates the capacity of the battery. LMD is set to PFC during a bq2014 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2014 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -250mV. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after V_{SR} > -250mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination when excessive discharges occur.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2014. The segment drivers, SEG_{1-5} and DONE, have corresponding PPD register locations, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx101001. (Note: DONE must be pulled down for proper operation.)

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2014. The segment drivers, SEG_{1-5} and DONE, have corresponding PPU register locations, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and DONE have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2014 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0Ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2010. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2014 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2014.*

Resetting the bq2014 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: Self-discharge is disabled when $PROG_5$ = H.

Display

The bq2014 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2014 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description on pages 12 and 13.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. **Note: $\overline{DISP}$ must be tied to V_{CC} if the LEDs are not used.** When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to V_{SRO} < -4mV or charge current is detected, V_{SRO} > V_{SRQ}. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2014 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2014, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2014 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2014 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning, default	0.92	0.95	0.98	V	SB
V_{EDV1}	First empty warning, default	1.02	1.05	1.08	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR
V_{SRO}	SR sense range	-300	-	+2000	mV	SR
V_{OVLD}	Overload threshold	-220	-250	-280	mV	SR
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Notes:
1. Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance.
2. To ensure correct threshold determination and proper operation, $V_{CC} > V_{SB} + 1.5V$

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	Battery input	-	-	2.4	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_5$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_5$; note 1
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_5$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-5}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-5}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ, EMPTY, CHG
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_5$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_5$

Notes: All voltages relative to V_{SS}.

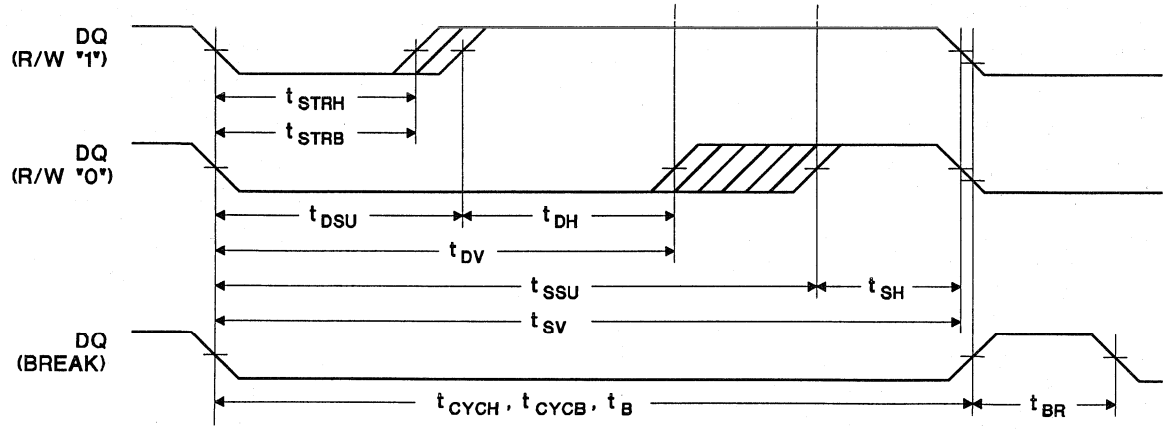
1. DONE must be pulled low for proper operation.

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2014	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2014 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2014	5	-	-	ns	
t_{STRB}	Start hold, bq2014 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



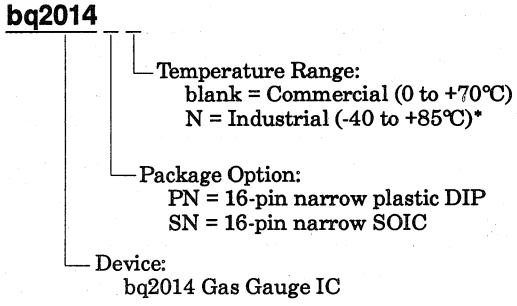
RC-34

Data Sheet Revision History

ChangeNo.	Page No.	Description	Nature of Change
1	2-285, 2-287, 2-289, 2-290, 2-291, 2-297, 2-299	Changed display mode	Relative display mode only
1	2-285, 2-301	DONE pin	Removed $PROG_6$
1	2-286, 2-301	DONE pin	Added: DONE pin must be pulled to V_{SS} with a 200KΩ resistor
1	2-290	Table 1	Removed $PROG_6$
1	2-291	DONE input	Was: NAC is set to 90%... Is: NAC is set to 94%...

Note: Change 1 = Dec. 1994 B "Final"changes from Aug. 1994 A "Preliminary."

Ordering Information



* Contact factory for availability.

BENCHMARQ

Preliminary **bq2031**

Lead Acid Fast Charge IC

Features

- Conforms to battery manufacturers' charge recommendations for cyclic and float service
- Pulse-width modulation regulator
  - Ideal for high-efficiency switch-mode designs
  - External control of frequency reduces EMI concerns
  - Configurable for linear or gated-current regulation use
- Temperature-compensated voltage thresholds
- Pin-selectable auto-cycle charge algorithms
  - Two-step constant voltage
  - Dual-level constant current
  - Constant-current pulse
- State-of-health monitor detects shorted, opened, or damaged cells and conditions battery
- Charging qualified by temperature and voltage limits
- Pin-selectable charge maintenance methods
  - Pulsed current algorithm with automatic battery age compensation
  - Temperature-compensated float voltage
- Direct-drive LED outputs display charge status and fault conditions
- Pin-selectable bulk charge termination by maximum voltage, $-\Delta^2V$, minimum current, and maximum time

General Description

The bq2031 monolithic CMOS IC is designed to optimize charging of lead acid chemistry batteries. The flexible pulse-width modulation regulator can be used to control constant-voltage or constant-current charging. The regulator frequency is set by external components to offer flexibility to control EMI. The switch-mode design keeps power dissipation to a minimum while delivering high efficiency for high-charge-current requirements.

Battery life is extended by temperature-compensated voltage thresholds, which are used during constant-voltage charging to allow continuous float operation over an extended temperature range.

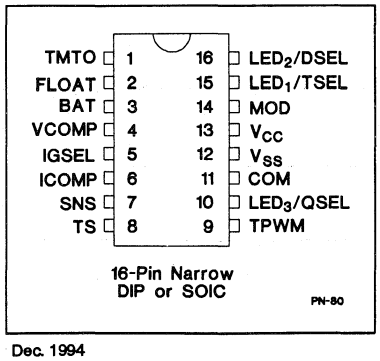
Charge action begins on application of power or battery replacement. For safety, charging is inhibited until the battery voltage and temperature are within configured limits. If the voltage is less than the low-voltage threshold, the bq2031 provides trickle-current conditioning of the battery. The conditioning algorithm is based on the SAE J537 charge acceptance test procedure that senses an increase in both current and voltage. This prevents high-current bulk charging of possibly damaged or reversed cells and can detect a shorted or open cell during all charging.

The bq2031 charger automatically sequences through several charge states based on the battery voltage and charging current conditions. The two-step constant-voltage charge mode includes a current-limited bulk state that typically replenishes up to 80% of the charge, a voltage-regulated "top-off" state that returns the remaining charge, and a temperature-compensated float voltage that maintains the full-charged condition.

The dual-level constant-current mode includes a current-regulated bulk state and a regulated trickle current maintenance state. The bq2031 charge states are terminated by an integrated maximum time-out (MTO) charge safety timer. The timer timebase uses an external RC time constant that allows for timed charge control and prevents overcharging.

The bq2031 current modes offer $-\Delta^2V$ termination to compensate for battery aging and a pulse charge maintenance mode to increase float life.

Pin Connections



16-Pin Narrow DIP or SOIC

PN-80

Pin Names

TMTO	Time-out timebase
FLOAT	State control
BAT	Battery voltage
VCOMP	Voltage loop comp
IGSEL	Current gain select
ICOMP	Current loop comp
SNS	Sense resistor input
TS	Temperature sense
TPWM	Regulator timebase
COM	Common LED output
LED3/ QSEL	Charge status output 3/ charge regulation select
Vss	System ground
Vcc	5.0V ±10% power
MOD	Modulation control
LED1/ TSEL	Charge status output 1/ Termination select
LED2/ DSEL	Charge status output 2/ Display select

Dec. 1994

During under-voltage conditioning, the maximum time-out termination counter is used to indicate a fault condition. The fault indication is a safety factor and an indicator that the battery was unable to reach acceptable charge current and voltage levels within a preset time.

Temperature prequalifications include upper and lower threshold limits that hold the charge-pending state while indicating a temperature pending condition. Charge action resumes when the temperature is within limits. External control of the TS input can be used to inhibit or suspend charge action.

The bulk state is terminated and the float state is initiated when the battery thresholds exceed the programmed values. Bulk charging is terminated by the following:

- Maximum threshold voltage
- Second difference of cell voltage ($-\Delta^2V$)
- Minimum cutoff current (MCI)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

Charger status can be displayed in three modes using three dedicated output pin drivers. Each driver is a direct interface to common-cathode LED displays for indicating the following charger status:

- Charge pending
- Charging
- Charge complete
- Fault conditions

The charge mode, termination method, and voltage and current thresholds are easily set to the manufacturers' specifications. Control of charge method, rate, and time allows the bq2031 to be configured for true "plug and forget" operation.

Figure 1 is a block diagram of the bq2031 lead acid charger IC.

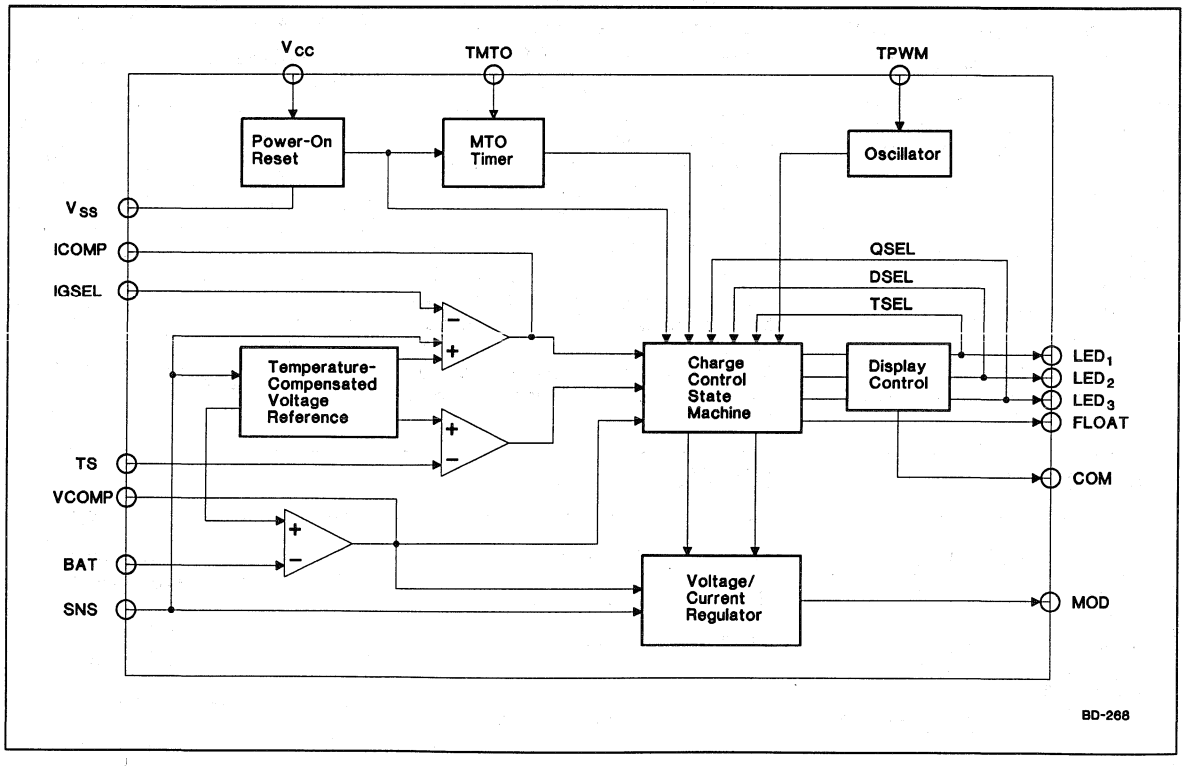


Figure 1. bq2031 Block Diagram

Pin Descriptions

TMTO **Time-out timebase input**

Timebase for maximum time-out charge termination. The external resistor and capacitor connections are shown in Figure 7 and equation 6.

FLOAT **State control output**

Open-drain output for external resistor divider network connection to control the BAT input voltage threshold for the float charge state. See Figure 5.

BAT **Single-cell voltage input**

Single-cell voltage for the battery pack. Resistor divider network connected between the positive and the negative terminals of the battery. See Figure 5 and equations 1–3.

VCOMP **Compensation output**

External capacitor for voltage loop stability.

IGSEL **Current gain select**

External resistor connection to set I_{MIN}. See Figure 8 and Table 4.

ICOMP **Current compensation output**

External capacitor for current loop stability.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor. See equation 4.

TS **Temperature sense input**

Input for external battery temperature monitoring thermistor or probe. The external resistor and thermistor divider network is set for the lower and upper temperature threshold limits shown in Figure 5.

TPWM **Regulation timebase input**

External timing capacitor sets the pulse-width modulation (PWM) frequency. See Figure 7 and equation 5.

COM **Common LED output**

Common output for LED_{1-3}. Output is high impedance during initiation to read soft-program input.

QSEL **Charge regulation select input**

Soft-programmed three-level input selects constant-voltage or constant-current regulation mode. See Table 2.

MOD **Current-switching control output**

MOD is a push/pull output that is used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

LED_{1-3} **Charger display status 1–3 outputs**

Charger status output drivers for direct drive of LED displays. Display modes are shown in Table 3.

DSEL **Display select**

Soft-programmed three-level input controls the LED_{1-3} charge display modes. See Table 3.

TSEL **Termination select**

Soft-programmed input controls constant-current bulk charge termination. See Table 2.

V_{CC} **V_{CC} supply input**

5.0V ± 10% power input

V_{SS} **Ground**

Parameter Definitions

I_{MAX} Maximum current limit. $I_{MAX} = 0.250V/R_{SNS}$.

I_{MIN} Minimum current limit to terminate constant-voltage top-off charge or regulated trickle current maintenance charge.

I_{COND} Conditioning state current detection and regulation threshold. $I_{COND} = I_{MAX}/5$

I_{SNS} Charge current sensed at SNS pin.

V_{BLK} Maximum threshold voltage. Constant voltage mode top-off charge regulation voltage or bulk charge termination threshold.

V_{FLT} Temperature-compensated float voltage.

V_{BAT} Voltage at the BAT pin.

V_{SNS} Voltage at the SNS pin.

V_{TEMP} Voltage at the TS pin.

V_{CELL} Single-cell battery voltage. $V_{CELL} = V_{BAT} - V_{SNS}$.

V_{REF} Internal temperature-compensated voltage reference.

V_{HTF} High-temperature fault that suspends charge actions until V_{TEMP} is greater than V_{HTF}.

V_{LTF} Low-temperature fault that suspends charge actions until V_{TEMP} is less than V_{LTF}.

V_{TCO} High-temperature cutoff limit internally set at $0.4V_{CC}$.

V_{MIN} Minimum low-voltage threshold for beginning bulk charging. If V_{CELL} is less than V_{MIN}, bulk charge will pend, and the industry-standard charge acceptance test is performed.

V_{MCV} Maximum cell voltage threshold to detect battery removal and over-voltage fault for V_{CELL} greater than V_{MCV}.

Functional Description

Table 1 summarizes the bq2031 operation. Charge action states are listed with associated conditions and MOD output control action. Table 2 describes the bq2031 charge action control pins QSEL and TSEL. QSEL is a two-level soft-programmed input pin that sets the charge mode, and soft-programmed input pin TSEL selects the bulk charge termination method and the charge maintenance action. In all charge modes, the bq2031 controller automatically resets to the conditioning 1 state when V_{CELL} is less than V_{MIN}, such as in a deep discharge load.

Charge Modes

For two-step constant-voltage current-limited charging, the bq2031 regulates the battery voltage at a constant value regardless of the battery state of charge. Figure 2 shows the voltage thresholds and charge profile for the constant-voltage mode with the charge maintenance state temperature-compensated float voltage regulation. At the start of the bulk charge state, the current is limited at the maximum value (I_{MAX}), which ensures that the maximum charge is transferred. When the battery cell voltage (V_{CELL}) exceeds 0.94 of the external set threshold (V_{BLK}), the top-off state is indicated because the battery has reached a state-of-charge of approximately 80% or greater. Current-limited charging continues until V_{CELL} equals V_{BLK}; then voltage regulation begins at the V_{BLK} value,

Table 1. bq2031 Operational Summary

Charge Action State	Conditions	MOD Output
Charge initiation	V_{CC} applied, V_{CELL} increases > 0.8V	Low
Conditioning 1	Charge initiation and $V_{HTF} < V_{TEMP} < V_{LTF}$ and if $V_{CELL} < V_{MIN}$; $V_{CELL} = V_{FLT} + 0.250V$ if $I_{SNS} < I_{COND}$ and 0.02 * MTO; conditioning MTO fault	Voltage regulation
Conditioning 2	Conditioning 1 completed and $V_{HTF} < V_{TEMP} < V_{LTF}$ and if $I_{SNS} \geq I_{COND}$; $I_{SNS} = I_{COND}$ if $V_{CELL} < V_{MIN}$ and 0.16 * MTO; conditioning MTO fault	Current regulation
Charge pending	Charge initiation and $V_{TEMP} < V_{HTF}$ or $V_{TEMP} > V_{LTF}$	Low
Bulk charging	Charge pending and conditioning 2 completed and $V_{MIN} < V_{CELL} < V_{MCV}$ and if $V_{CELL} < V_{BLK}$; $I_{SNS} = I_{MAX}$, or if QSEL = 1 and TSEL = 1; $V_{CELL} < V_{BLK}$ and $\Delta^2V > 0$; $I_{SNS} = I_{MAX}$	Current regulation
Top-off charging	Bulk charging completed and $V_{HTF} < V_{TEMP} < V_{LTF}$ and $V_{MIN} < V_{CELL} < V_{MCV}$ and if QSEL = 0; $I_{SNS} > I_{MIN}$; $V_{CELL} = V_{BLK}$	Voltage regulation
Charge completion	Bulk and top-off charging completed and maximum time-out (MTO) and $V_{MIN} < V_{CELL} < V_{MCV}$ or maximum cut-off voltage (MCV) or if QSEL = 0; $I_{SNS} \leq I_{MIN}$ or if QSEL = 1; $V_{CELL} \geq V_{BLK}$ or $\Delta^2V < 0$	Low
Charge maintenance	Charge completion and $V_{HTF} < V_{TEMP} < V_{LTF}$ and $V_{MIN} < V_{CELL} < V_{MCV}$ and if QSEL = 0; $V_{CELL} = V_{FLT}$	Voltage regulation
Charge maintenance	Charge completion and $V_{HTF} < V_{TEMP} < V_{LTF}$ and $V_{MIN} < V_{CELL} < V_{MCV}$ and if QSEL = 1 and TSEL = 1; set $I_{SNS} = 0$ if $V_{CELL} \leq V_{FLT}$, go to bulk charging	Low
Charge maintenance	Charge completion and $V_{HTF} < V_{TEMP} < V_{LTF}$ and $V_{MIN} < V_{CELL} < V_{MCV}$ and if QSEL = 1 and TSEL = 0; $I_{SNS} = I_{MIN}$	Current regulation

Note: 1 = V_{CC}, 0 = V_{SS}.

Table 2. bq2031 Charge Action Control Summary

Charger Mode	QSEL	TSEL	Bulk Charge Termination	Top-off Charge Termination	Charge Maintenance Action
Constant voltage	0	X	V_{BLK}/MTO	I_{MIN}/MTO	Voltage regulation at V_{FLT}
Constant current pulsed	1	1	V_{BLK}/-Δ^2V/MTO	-	Pulsed current regulation at I_{MAX}
Constant current	1	0	V_{BLK}/-Δ^2V/MTO	-	Pulsed current regulation at I_{COND}

and the current tapers off exponentially as the battery approaches full charge. Top-off charge is terminated when the charge current (I_{SNS}) decreases below the externally set I_{MIN} threshold. During constant-voltage mode, the charge safety timer (MTO) terminates both the bulk and top-off states. In the top-off state, the MTO timer is reset, which terminates top-off and initiates the maintenance state.

The advantage of the constant-voltage mode is that the battery self-regulates the amount of current depending on the state of charge and all voltages are temperature-compensated. The constant-voltage mode can be used in both cyclic and float applications to control rapid charging at an elevated level and then step down to the temperature-compensated float voltage.

Figure 3 shows the current thresholds and charge profile for the dual-level constant-current mode with charge maintenance state trickle current regulation. The constant-current mode provides a high initial charge rate at a maximum current (I_{MAX}) until the battery cell voltage (V_{CELL}) approaches a fully charged condition. The bq2031 terminates bulk charge when V_{CELL} is greater than or equal to V_{BLK} and then enters the maintenance state and regulates trickle current at I_{MIN}.

The advantage of the constant-current method is the efficiency and control of a high charge volume transferred at the beginning of charging and the maintenance state trickle current (I_{MIN}). The battery can be charged very quickly with the cells receiving a limited amount of overcharge, whereas series cells can be well-equalized with the regulated trickle current. During the bulk charge state when current is at I_{MAX}, the charge safety timer allows for accurate timed charge control.

The constant-current pulse mode shown in Figure 4 uses the same current-limited bulk charge state as the constant-current mode, but uses a pulsed current method to maintain the charged condition. The bulk charge state terminates either when V_{CELL} exceeds V_{BLK} or when the second difference of the cell voltage is less than zero ($\Delta^2V < 0$). The pulsed current algorithm uses the two exter-

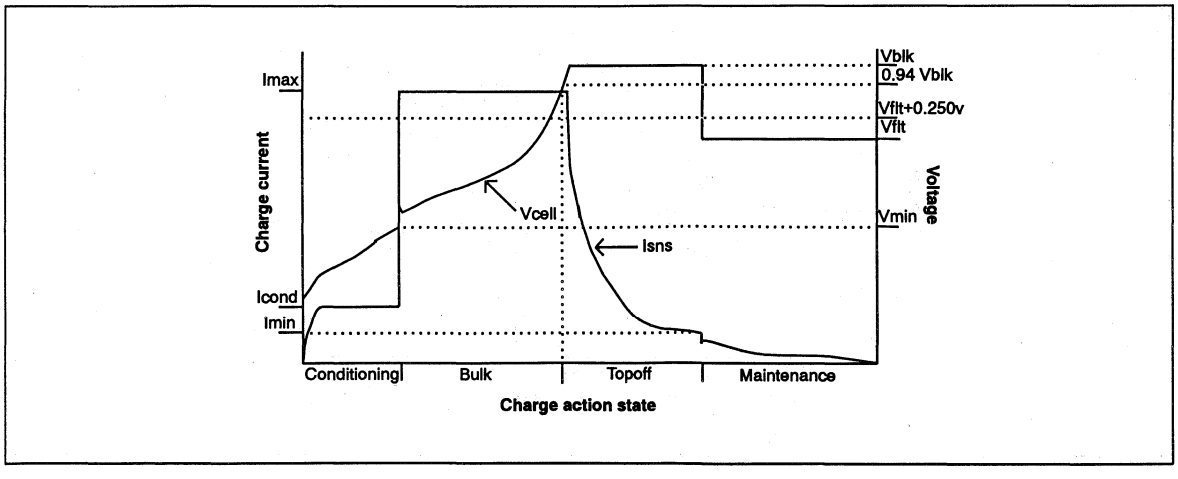


Figure 2. Charging Profile for Constant-Voltage Mode

nally set voltage thresholds (V_{BLK} and V_{FLT}) to enable or disable current regulation. When V_{CELL} is less than or equal to the externally set float voltage (V_{FLT}), the bulk charge state is initiated and V_{CELL} increases rapidly. When V_{CELL} rises to be greater than or equal to the V_{BLK} or when the second difference of V_{CELL} is less than zero ($\Delta^2V < 0$), the maintenance state is indicated with no charge action (i.e., $I_{SNS} = 0$). The battery cell voltage then slowly decays to the V_{FLT} threshold and the cycle repeats. The time of each successive bulk charge current pulse time decreases, and the maintenance state time increases until an equilibrium pulsed duty cycle is established to maintain the charge condition. During the bulk state, the MTO timer is a safety termination method.

The advantage of the pulsed current algorithm is that it provides a method to compensated for battery aging. As the battery ages, the cell voltage may not reach the initial V_{BLK} threshold of a new battery, but the bq2031 terminates the bulk charge state by detecting the second difference of cell voltage ($-\Delta^2V$), which is a characteristic of the battery electrochemistry. This threshold is used to terminate the bulk state on every charge cycle and offers an automatic compensation to assure full charge is replenished regardless of battery age or cell voltage deg-

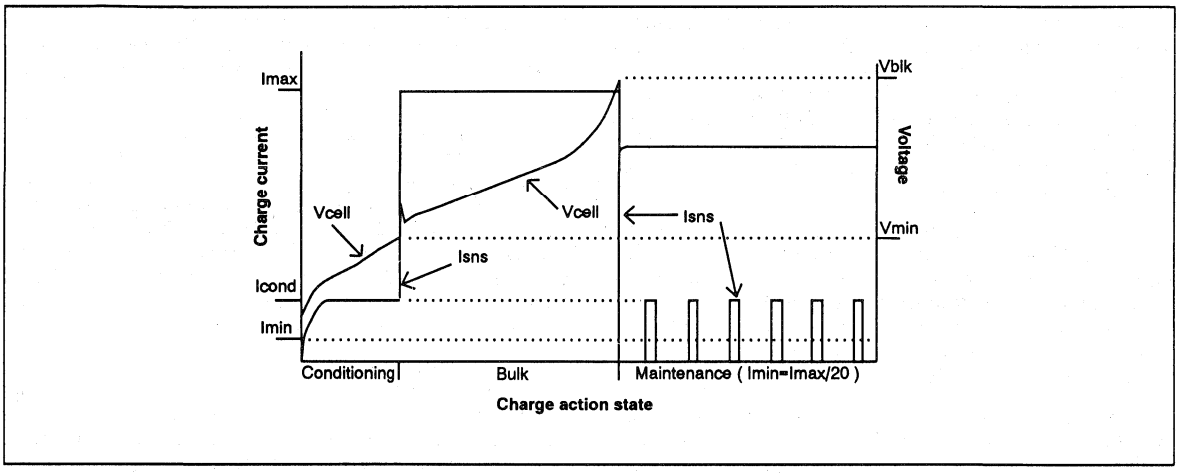


Figure 3. Charging Profile for Constant-Current Mode

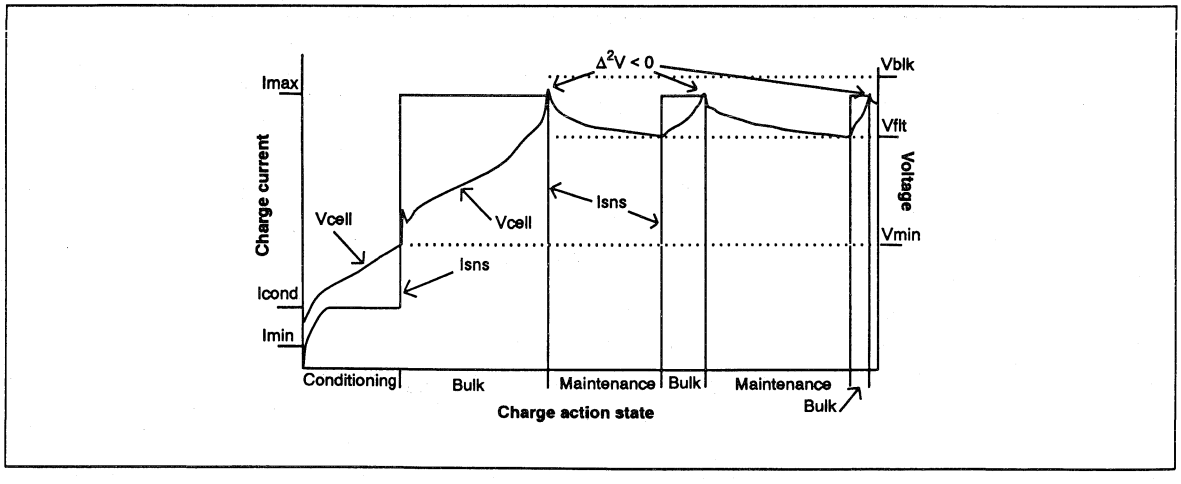


Figure 4. Charging Profile for Constant-Current Pulse Mode

radation. The pulse charging method also has benefits to prolong battery life by reducing the continuous charge potential during float applications.

Charge Terminations and Faults

The bq2031 terminates the bulk charge state by one of the methods that are determined by the charge mode input QSEL and termination select input TSEL. See Table 2.

The maximum threshold voltage (V_{BLK}) is a normal bulk termination for both constant-current and constant-voltage current-limited charging. In constant-current mode, when the cell voltage exceeds the threshold ($V_{CELL} > V_{BLK}$), the bulk charge state is terminated. In constant-voltage mode, when $V_{CELL} > 0.94 * V_{BLK}$, the top-off state is indicated, and voltage regulation at V_{BLK} begins when $V_{CELL} = V_{BLK}$.

The battery cell voltage second difference ($-\Delta^2V$) termination is available in the constant-current modes only. The bq2031 makes termination decisions based on a proprietary algorithm of monotonic accumulation of decreasing voltage changes.

The minimum cutoff current (MCI) is used for normal termination in the constant-voltage mode top-off state. When the charge current tapers below the MCI value ($I_{SNS} < I_{MIN}$), the charge state controller terminates the top-off charge state and enters the maintenance state.

The maximum time-out (MTO) termination provides an override normal termination for all constant-voltage and constant-current charge modes. The timer value sets the maximum time allocated for battery charge acceptance conditioning, bulk charging, and top-off charging. At the start of the conditioning, bulk, and top-off charge states, the MTO timer is cleared and begins counting. When the MTO timer completes, the bulk or top-off charge terminates and the maintenance state is initiated. This prevents overcharging and provides a safety valve to ensure that charging completes in the programmed time interval. The timer value is set with an external R-C as shown in Figure 7.

Lower-temperature fault (LTF) is a prequalification condition during the charge-pending state and a fault condition for the bulk charge state. LTF is the low-temperature limit for safe charging to continue. Maximum-temperature fault (HTF) is a prequalification condition during the charge-pending state and a fault condition for the bulk charge state. HTF is the high-temperature limit for safe charging to continue.

Voltage Termination Hold-off

At the start of the bulk charge state, there is a hold-off time period; during this period, V_{BLK}, $-\Delta^2V$ voltage terminations, and top-off state indication are disabled. Once past this hold-off period, V_{BLK}, $-\Delta^2V$, and top-off state indication are re-enabled. This hold-off period ($t_{HOLDOFF}$) is to prevent false termination due to the initial voltage surges when a deeply discharged or sulfated battery is subjected to a high current charge. The maximum cutoff voltage (V_{MCV}) is not disabled during voltage termination holdoff. In the constant current pulse mode, the hold-off period is applied only on the first bulk charge cycle.

Temperature and Voltage Qualifications

To provide maximum safety for the battery and system, the battery voltage and temperature must fall within acceptable limits before charging is initiated. The V_{TEMP} voltage is compared to an internal low-temperature threshold of V_{LTF} ($0.6 * V_{CC}$) and a high-temperature threshold of V_{HTF} ($0.4 * V_{CC}$). For a charge action to be initiated, V_{TEMP} must be

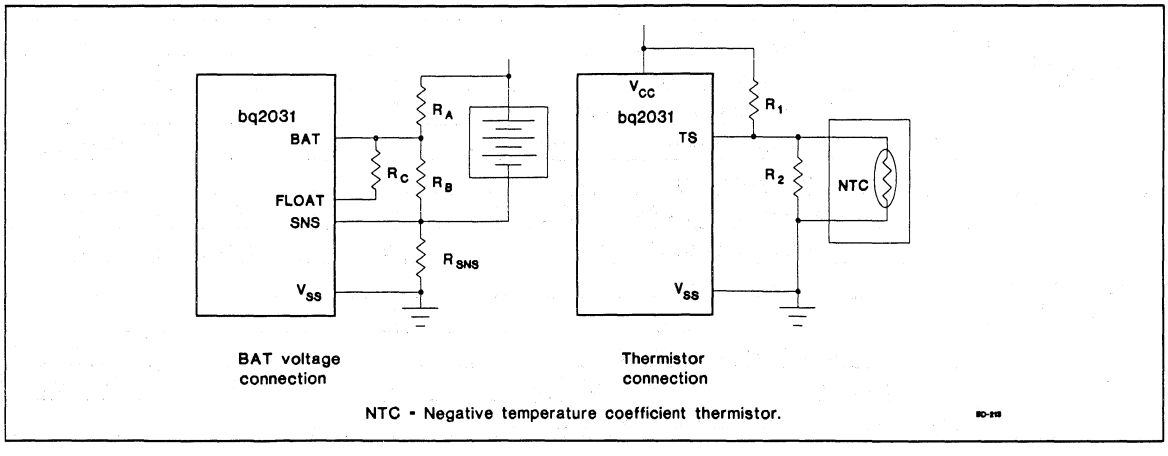


Figure 5. Voltage and Temperature Limit Measurement

greater than V_{HTF} and less than V_{LTF}. These limits establish the temperature range to qualify bulk and maintenance charging. The charging profile in Figure 3 shows the charge-pending condition for $V_{TEMP} < V_{HTF}$. If the battery temperature is outside these limits, the bq2031 enters the charge-pending state with no charge action and waits until the temperature is within limits. Figure 5 shows the temperature threshold circuit.

The bq2031 provides undervoltage protection by detecting when the battery voltage is below the low-threshold voltage (V_{MIN}). In the case of a deeply discharged battery ($V_{CELL} < V_{MIN}$), the bq2031 enters the conditioning state and charges the battery until the voltage and current increase, indicating positive charge acceptance. The conditioning algorithm is based on the SAE industry-standard J537 charge acceptance test procedure. The conditioning algorithm first provides a constant voltage (V_{FLT} + 0.250V) for a time t_{UV1} and measures if the charge current (I_{SNS}) is greater than I_{COND}. If $I_{SNS} \geq I_{COND}$ during the t_{UV1} time, conditioning state 1 is terminated and conditioning state 2 is initiated. If $I_{SNS} < I_{COND}$, a fault is indicated, and charge action is stopped. Conditioning state 2 provides a constant current for a time t_{UV2}. If the cell voltage is greater than V_{MIN} during the t_{UV2} time, conditioning state 2 is terminated and the bulk state is initiated. The conditioning algorithm senses the current after t_{UV1} and the voltage after t_{UV2}. If $I_{SNS} < I_{COND}$ at t_{UV1} or $V_{CELL} < V_{MIN}$ at t_{UV2}, a conditioning maximum time-out (MTO) fault is indicated.

The charging profile in Figure 2 shows the charge conditioning state for $V_{CELL} < V_{MIN}$. The conditioning parameters (time-out values and I_{COND}) are a function of the battery capacity, where conditioning time-out values (t_{UV1} and t_{UV2}) are percentages of the bulk charge time-out (t_{MTO}).

Temperature Compensation

A precision internal reference is temperature compensated to track the lead acid cells reaction temperature coefficient. Temperature compensation assures proper charging and termination over an extended temperature range. The float voltage is a critical value that is precisely regulated to prevent overcharging, extend battery life, and ensure that a full charge is maintained. The bq2031 varies the float voltage based on the battery temperature to compensate for changes in the battery charge rate.

Table 3. bq2031 Display Output Summary

Mode	Charge Action State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent or over-voltage fault	0	0	1
	Charge conditioning	Flashing	0	0
	Bulk or top-off charging	1	0	0
	Maintenance charging	0	1	0
	Charge pending (temperature out of range)	X	X	Flashing
	Charging fault (over-voltage or conditioning MTO)	X	X	1
DSEL = 1 (Mode 2)	Battery absent or over-voltage fault	0	0	1
	Charge conditioning	1	1	0
	Bulk charging	0	1	0
	Maintenance or top-off charging	1	0	0
	Charge pending (temperature out of range)	X	X	Flashing
	Charging fault (over-voltage or conditioning MTO)	X	X	1
DSEL = Float (Mode 3)	Battery absent or over-voltage fault	0	0	1
	Charge conditioning	Flashing	Flashing	0
	Bulk charging	0	1	0
	Top-off charging	1	1	0
	Maintenance charging	1	0	0
	Charge pending (temperature out of range)	X	X	Flashing
	Charging fault (over-voltage or conditioning MTO)	X	X	1

Note: 1 = V_{CC}, 0 = V_{SS}, X = don't care.

The internal reference is precisely designed to track the lead-acid cells temperature coefficient of -3.7mV/°C.

Charge Status Indication

Table 3 lists the bq2031 status display modes. The three modes offer flexibility for different types of visual displays and varying amounts of displayed information. The DSEL = 0 mode is intended for implementation of a simple two-LED indication system, where one LED indicates charging and the second LED indicates completion. DSEL = 1 mode is for implementation of a single common-cathode tri-color LED such that charging, completion, and fault each have a unique color. DSEL = Z mode is intended to offer charging capacity information in the constant-voltage mode by indicating the top-off state where approximately 80% or greater charge has been replenished. In all modes, LED_3 indicates the charge pending or fault condition. The LED_{1-3} flashing rate is typically 1/8 second on and 1/8 second off.

Charge Current Control

The bq2031 controls charge current through the MOD output pin. The current control is designed to support implementation of a bulk regulator configuration as shown in Figure 6. The PWM switch-mode regulation allows the designer to set the frequency to constrain electro-magnetic interference (EMI). The PWM timebase is set with an external capacitor as shown in Figure 7.

Voltage and Current Thresholds

Battery voltage is sensed at the BAT pin through a high-impedance resistive divider network. The bq2031 controls the voltage thresholds by changing the FLOAT output pin impedance. Figure 5 and Figure 8 show the voltage measurement circuit.

Equations 1 and 2 define the bulk charge voltage, and equation 3 defines the float maintenance voltage.

$$N * V_{BLK} * \frac{R_{BP}}{R_A + R_{BP}} = 2.30 \qquad \text{Equation 1}$$

$$R_{BP} = R_B * \frac{R_C}{R_B + R_C} \qquad \text{Equation 2}$$

$$N * V_{FLT} * \frac{R_B}{R_A + R_B} = 2.30 \qquad \text{Equation 3}$$

where:

N = number of cells and

2.30V = bq2031 voltage reference

The battery current is sensed through a low-impedance resistor in the battery current return loop. The bq2031 controls the current thresholds by changing the gain of the sense amplifier. Table 4 and 5 and Figure 8 show the IGSEL input circuit configuration. Equation 4 defines the maximum charge current limits.

$$I_{MAX} = \frac{0.250V}{R_{SNS}} \qquad \text{Equation 4}$$

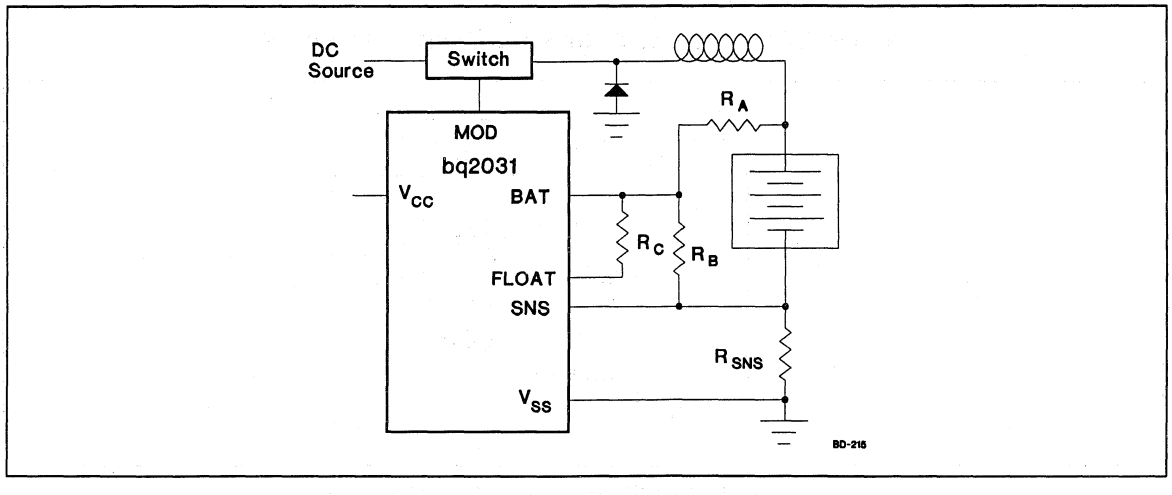


Figure 6. Switch-Mode Buck Regulator Configuration

It is recommended that:

$$300K < (R_A + R_B) < 800K$$

Follow these steps to calculate R_A, R_B, and R_C in Figure 8.

1. Start with $R_A = 200K\Omega$.
2. Determine R_B from equation 3.
3. Determine R_{BP} from equation 1.
4. Compute R_C from equation 2.

Table 4. I_{MIN} Termination Thresholds

IGSEL	I_{MIN}
0	$I_{MAX}/10$
1	$I_{MAX}/20$
Z	$I_{MAX}/40$

Table 5. I_{MIN} Pulse Current Regulation

IGSEL	I_{MIN}	DC	T(sec.)
0	$I_{COND}/2$	1/2	1
1	$I_{COND}/4$	1/4	2
Z	$I_{COND}/8$	1/8	4

Note: $I_{COND} = I_{MAX}/5$

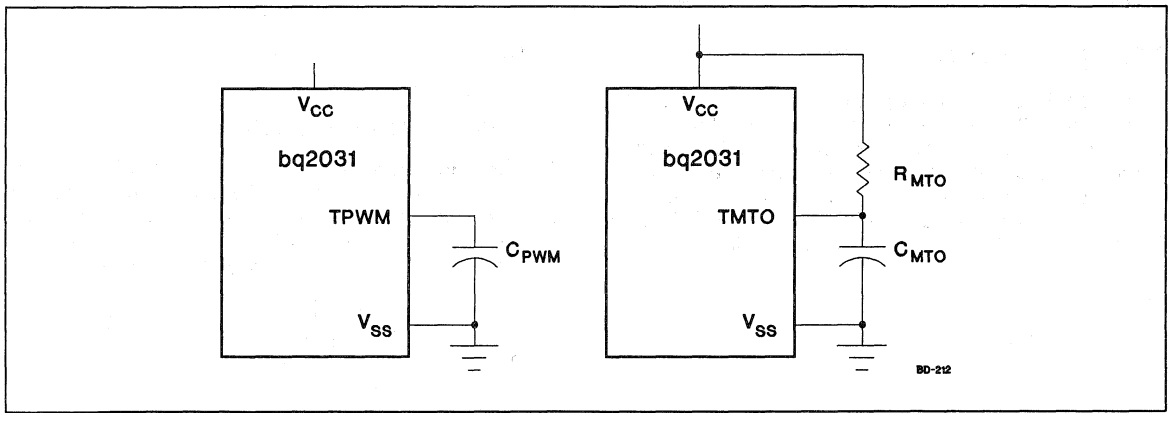


Figure 7. Regulator and Time-out Timebase Circuits

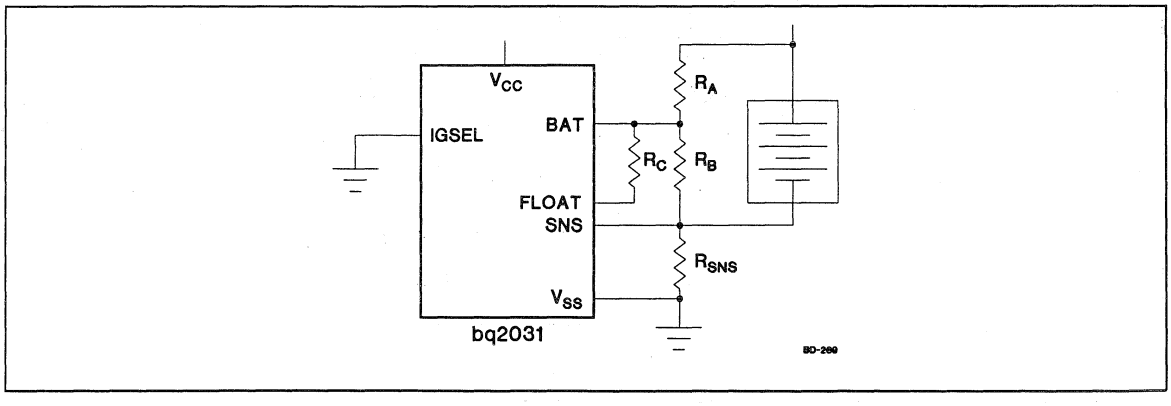


Figure 8. IGSEL External Setting Circuit ($I_{MIN} = I_{MAX}/10$)

Timebase Control

The bq2031 PWM frequency is set with an external capacitor shown in Figure 7. The frequency is linear with capacitance values.

$$F_{PWM\ (KHz)} = (1/C_{PWM\ (\mu F)}) * 10^{-1} \quad \text{Equation 5}$$

The bq2031 charge safety timer (MTO) is set with an external resistor and capacitor as shown in Figure 7. For fixed capacitor, the resistor value is linear with time.

$$t_{MTO\ (hours)} = R_{MTO\ (k\Omega)} * C_{MTO\ (\mu F)} * 10^{-1} \quad \text{Equation 6}$$

2

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REF}	Internal reference voltage	2.30	V	1%	T_A = 25°C
	Temperature coefficient	-3.7	mV/°C	10%	
V_{BAT}	Voltage sense error to MOD	-	V	TBD	
V_{LTF}	TS maximum threshold	0.6 * V_{CC}	V	±0.030V	Low temperature fault
V_{HTF}	TS minimum threshold	0.44 * V_{CC}	V	±0.030V	High temperature fault
V_{TCO}	Minimum cutoff voltage	0.4 * V_{CC}	V		High temperature cutoff
V_{MCV}	Maximum cutoff voltage	0.60 * V_{CC}	V	10%	10% V_{CC}
V_{MIN}	Under-voltage threshold at BAT	0.38 * V_{CC}	V	10%	10% VCC
V_{INT}	Charge initiation threshold	0.8	V	±0.030V	Valid battery insertion
V_{PWM}	Timebase threshold at PWM	TBD		TBD	
V_{MTO}	Time-out threshold at MTO	0.6 * V_{CC}	V	±10%	10% V_{CC}
I_{SNS}	Current sense at SNS	I_{MAX}	%	±10%	10% V_{CC}
		I_{MIN}	%	TBD	

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{IH}	Logic input high	V_{CC}-1.0	-	-	V	QSEL,TSEL
		V_{CC}-0.3	-	-	V	DSEL, IGSEL
V_{IL}	Logic input low	-	-	V_{SS}+1.0	V	QSEL,TSEL
		-	-	V_{SS}+0.3	V	DSEL, IGSEL
I_{CC}	Supply current	-	TBD	-	mA	
I_{IZ}	DSEL tri-state open detection	-	TBD	-	µA	Note 2
I_{IL}	DSEL logic input low source	-	+30	-	µA	V = V_{SS} to V_{SS} + 0.3V
	IGSEL login input low source	-	-	+70	µA	V = V_{SS} to V_{SS} + 0.3V
I_{IH}	DSEL logic input high source	-	-30	-	µA	V = V_{CC} - 0.3V toV_{CC}
	IGSEL logic input high source	-70	-	-	µA	V = V_{CC} - 0.3V toV_{CC}
V_{OH}	LED_1, LED_2 ,LED_3, output high	V_{CC}-0.8	-	-	V	I_{OH} <= 10mA
	MOD output high	V_{CC}-0.8	-	-	V	I_{OH} <= 5mA
V_{OL}	LED_1, LED_2 ,LED_3, output low	-	-	V_{SS}+0.8V	V	I_{OL} <= 10mA
	MOD output low	-	-	V_{SS}+0.8V	V	I_{OL} <= 5mA
	FLOAT output low	-	TBD	-	V	I_{OL} <= TBD, Note 3
	COM output low	-	-	V_{SS}+0.5	V	I_{OL} <=30mA
I_{OH}	LED_1, LED_2 ,LED_3, source	-	-	-10	mA	V_{OH} =V_{CC}-0.5V
	MOD source	-5.0	-	-	mA	V_{OH} =V_{CC}-0.5V
I_{OL}	LED_1, LED_2 ,LED_3, sink	TBD	TBD	-	mA	V_{OL} = V_{SS}+0.5V
	MOD sink	-	TBD	-	mA	V_{OL} = TBD
	FLOAT sink	-	TBD	-	mA	V_{OL} = TBD, Note 3
	COM sink	-	30	-	mA	V_{OL} = V_{SS}+0.5V
I_L	Input leakage	-	-	±1	µA	QSEL, TSEL; Note 2

Notes: 1. All voltages relative to V_{SS}.

2. Conditions during initialization after V_{CC} applied.

3. SNS = OV

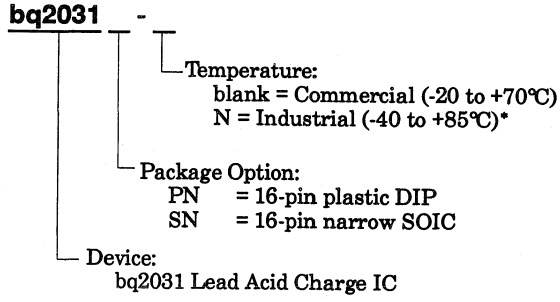
Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	Battery input impedance	50	-	-	MΩ	
R_{SNSZ}	SNS input impedance	50	-	-	MΩ	
R_{TSZ}	TS input impedance	50	-	-	MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)	-	-	10	KΩ	DSEL, TSEL, and QSEL
R_{PROG2}	Pull-up or pull-down resistor value	-	-	3	KΩ	IGSEL
R_{MTO}	Charge timer resistor	10	-	240	KΩ	C_{MTO} = 0.01µF, Maximum recommended value

Timing (TA = TOPR; VCC = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge timer time-out range	1	-	24	hours	See Figure 7, Equation 7
t_{UV1}	Conditioning time-out current sense period	-	$0.02t_{MTO}$	-		Fraction of t_{MTO}
t_{UV2}	Conditioning time-out voltage sense period	-	$0.16t_{MTO}$	-		Fraction of t_{MTO}
t_{DV}	$-\Delta^2V$ termination sample time period	-	$0.008t_{MTO}$	-		Fraction of t_{MTO}
$t_{HOLDOFF1}$	Conditioning state 2 holdoff time period	-	$0.002t_{MTO}$	-		Fraction of t_{MTO}
$t_{HOLDOFF2}$	Bulk-charge hold-off time period	-	$0.015t_{MTO}$	-		Fraction of t_{MTO}
F_{PWM}	Regulator timebase frequency range	-	100	TBD	KHz	See Figure 7, Equation 6
	External C_{PWM} range	-	0.001	-	µF	
	Charge timer time-out (t_{TMO}) accuracy		TBD			
	Regulator timebase frequency accuracy		TBD			

Ordering Information



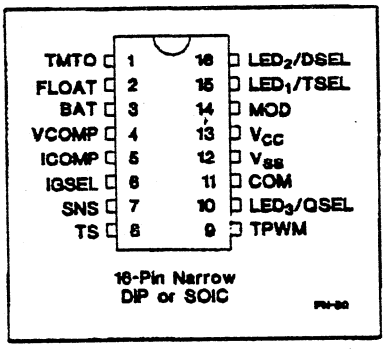
* Contact factory for availability.

Errata to bq2031

Lead Acid Fast Charge IC

The pinout on the bq2031 data sheet in the *1995 Data Book* is incorrect. The correct pinout is shown below:

Pin Connections



Pin Names

TMTO	Time-out timebase	COM	Common LED output
FLOAT	State control	LED_3/ QSEL	Charge status output 3/ charge regulation select
BAT	Battery voltage	Vss	System ground
VCOMP	Voltage loop comp	Vcc	5.0V ±10% power
IGSEL	Current gain select	MOD	Modulation control
ICOMP	Current loop comp	LED_1/ TSEL	Charge status output 1/ Termination select
SNS	Sense resistor input	LED_2/ DSEL	Charge status output 2/ Display select
TS	Temperature sense		
TPWM	Regulator timebase		

Gas Gauge IC With SMBus Interface

Features

- Provides conservative and repeatable measurement of available charge in NiCd, NiMH, and Lithium Ion rechargeable batteries
- Designed for battery pack integration
  - 120µA typical standby current
  - Small size enables implementations in as little as 1/2 square inch of PCB
- Supports Rev. 0.95 System Management Bus interface and Smart Battery Data specifications
- Measurements compensated for current and temperature
- Contains self-discharge compensation using internal temperature sensor
- Internal time base eliminates external resonator or crystal
- 16-pin narrow DIP or SOIC

General Description

The bq2040 Gas Gauge IC With SMBus Interface is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The bq2040 directly supports NiCd, NiMH, and Lithium Ion battery chemistries. Other battery chemistries will be supported with future variations of the device.

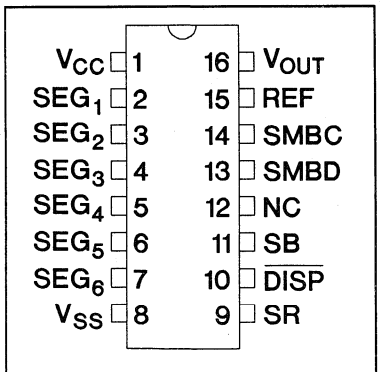
The bq2040 supports the System Management Bus (SMBus) protocol and the Smart Battery Data (SBData) specifications. Battery voltage, temperature, state-of-charge, capacity, charge-cycle count, etc. are available over the SMBus serial link. Battery-charge state can be directly indicated using a five- or six-segment LED display to graphically depict battery full-to-empty in 20% increments.

The bq2040 estimates battery self-discharge based on an internal timer and temperature sensor. The bq2040 applies compensations for battery temperature and rate of charge or discharge to the charge, discharge, and self-discharge calculations, providing available charge information across a wide range of operating conditions. The bq2040 automatically recalibrates, or "learns" battery capacity in the full course of a discharge cycle from full to empty.

The bq2040 may operate directly from 3 or 4 nickel chemistry cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} for other battery cell configurations.

An external E^2PROM is used to program initial values into the bq2040. Values such as design capacity, chemistry, and serial number, can be customized for individual battery pack configurations.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-76

Pin Names

V_{OUT}	Supply output	SB	Battery sense input
SEG_1	LED segment 1	$\overline{DISP}$	Display control input
SEG_2	LED segment 2	SR	Sense resistor input
SEG_3	LED segment 3	SMBC	Serial communication clock
SEG_4	LED segment 4	SMBD	Serial communication data input/output
SEG_5	LED segment 5		
SEG_6	LED segment 6	V_{CC}	3.0–6.5V
REF	Voltage reference output	V_{SS}	System ground

Pin Descriptions

SEG_1–SEG_6 **LED display segment outputs**

Each output may activate an external LED to sink the current sourced from V_{CC}.

SMBC **System management bus clock**

This open-drain bi-directional pin is used to clock the data transfer to and from the bq2040.

SMBD **System management bus data**

This open-drain bi-directional pin is used to transfer address and data to and from the bq2040.

SCL **Serial clock (shared with SEG_1)**

This output is used to clock the data transfer between the bq2040 and the external configuration memory.

SDA **Serial data and address (shared with SEG_2)**

This bi-directional pin is used to transfer address and data to and from the bq2040 and the external configuration memory.

NC **No connect**

V_{OUT} **Supply output**

This output supplies power to the external E^2PROM configuration memory, if present. Do not connect this pin if you are not using the external memory.

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2040 is $V_{SR} + V_{OS}$ (see Table 3 on page 8).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ floating allows the LED display to be active during charge or during discharge if the rate is greater than a user-programmable threshold. $\overline{DISP}$ low activates the display.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2040 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2040 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2040 using the LED capacity display, the serial port, and an optional external E^2PROM for battery pack programming information. The bq2040 can be configured for battery chemistry, manufacturer name and serial number, display mode, self-discharge compensation, and various other battery-specific information. Table 1 outlines the externally programmable functions available in the bq2040.

An internal temperature sensor eliminates the need for an external thermistor—reducing cost and components. An internal, temperature-compensated time-base eliminates the need for an external oscillator, further reducing cost and components. The entire circuit in Figure 1 could occupy less than ¾ square inch of board space.

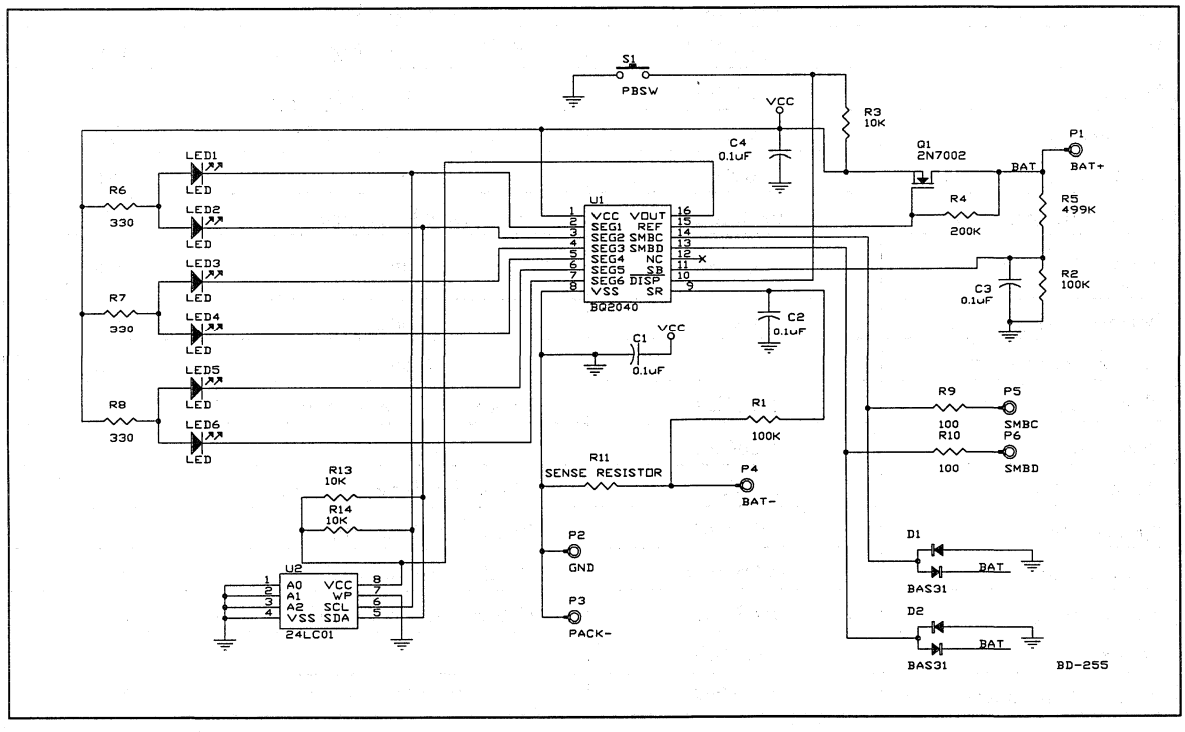


Figure 1. Battery Pack Application Diagram—LED Display

Table 1. Configuration Memory Programming Values

Parameter Name	Address	Length	Units
Design capacity	0x00/0x01	16 bits: low byte, high byte	mAh
Initial battery voltage	0x02/0x03	8 bits	N/A
Fast charging current	0x04/0x05	16 bits: low byte, high byte	mA
Charging voltage	0x06/0x07	16 bits: low byte, high byte	mV
Remain capacity alarm	0x08/0x09	16 bits: low byte, high byte	N/A
FLAGS1	0x0a	8 bits	N/A
FLAGS2	0x0b	8 bits	N/A
Current measurement gain	0x0c/0x0d	16 bits: low byte, high byte	N/A
EDV_1	0x0e/0x0f	16 bits: low byte, high byte	mV
EDV_F	0x10/0x11	16 bits: low byte, high byte	mV
Temperature offset	0x12/0x13	16 bits: low byte, high byte	°K
Self-discharge rate	0x14	16 bits: low byte, high byte	N/A
Digital filter	0x15	8 bits	N/A
Current integration gain	0x16/0x17	16 bits: low byte, high byte	N/A
Discharge display threshold	0x18	8 bits	N/A
Battery voltage offset	0x19	8 bits	mV
Battery voltage gain	0x1a	8 bits	N/A
Slow charging current	0x1b/0x1c	16 bits: low byte, high byte	mA
Reserved	0x1d/0x31	-	-
Design voltage	0x32/0x33	16 bits: low byte, high byte	mV
Specification info	0x34/0x35	16 bits: low byte, high byte	N/A
Manufacturer date	0x36/0x37	16 bits: low byte, high byte	N/A
Serial number	0x38/0x39	16 bits: low byte, high byte	N/A
Reserved	0x3a/0x3f	-	-
Manufacturer name	0x40/0x4f	8 + 120 bits	N/A
Device name	0x50/0x5f	8 + 120 bits	N/A
Chemistry	0x60/0x6f	8 + 120 bits	N/A
Manufacturer data	0x70/0x7f	8 +120 bits	N/A

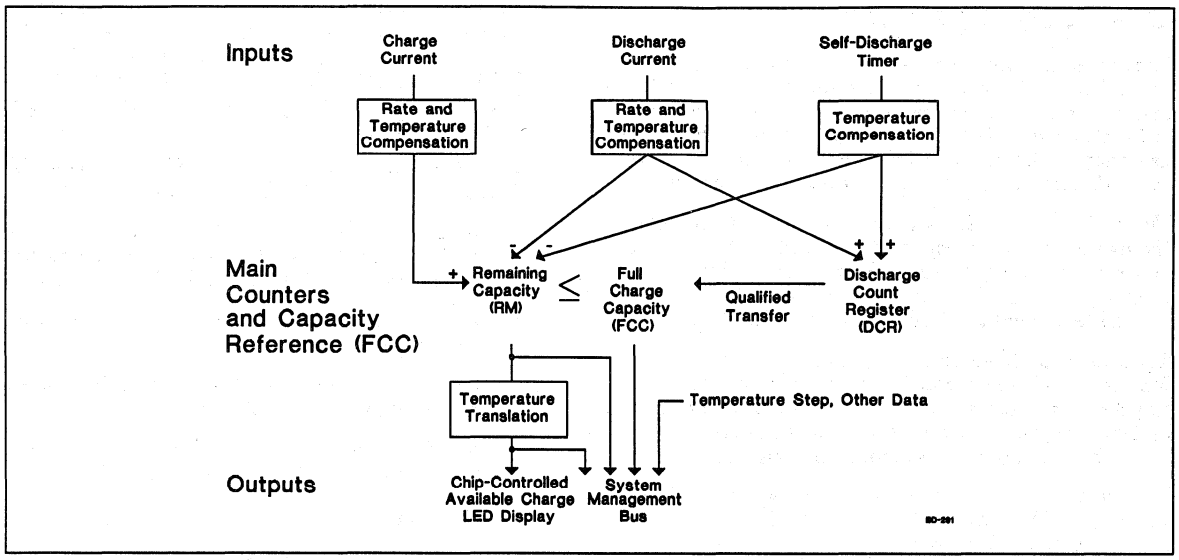


Figure 2. Operational Overview

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2040 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{R_5}{R_2} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_2 is connected to the negative battery terminal. R_5/R_2 should be rounded to the next highest integer. The battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV) and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The battery voltage gain is programmed via E^{2}PROM.

Two EDV thresholds for the bq2040 are externally programmable.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than 3A, EDV monitoring is disabled and resumes after the current falls below 1.5A.

Reset

The bq2040 is reset when first connected to the battery pack; the bq2040 can also be reset with a command over the serial port.

Temperature

The bq2040 monitors temperature using an internal sensor. The temperature is used to adapt charge/discharge and self-discharge compensations. Temperature may also be accessed over the serial port.

Layout Considerations

The bq2040 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1, C3, and C4) should be placed as close as possible to the SB and V_{CC} pins, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor (C2) should be placed as close as possible to the SR pin.
- The sense resistor (R_{11}) should be as close as possible to the bq2040.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2040. The bq2040 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature-compensated and charge is rate-compensated. Self-discharge is only temperature compensated.

The main counter, Remaining Capacity (RM), represents the available battery capacity at any given time. Battery charging increments the RM register, while battery discharging and self-discharge decrement the RM register and increment the DCR (Discharge Count Register).

The Discharge-Count Register (DCR) is used to update the Full-Charge Capacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2040 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Design Capacity (DC). Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent charges.

1. **Full-Charge Capacity or learned-battery capacity:**

   FCC is the last measured discharge capacity of the battery. On initialization (application of V_{CC}), FCC = DC. During subsequent discharges, the FCC is updated with the latest measured capacity in the Discharge Count Register (DCR), representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. The FCC also serves as the 100% reference threshold used by the relative display mode.

2. **Design Capacity (DC):**

   The DC is the user specified battery capacity and is programmed by using an external E^2PROM or by writing data over the serial port if the E^2PROM is not present. The DC also provides the 100% reference for the absolute display mode.

3. **Remaining Capacity (RM):**

   RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. RM is reset to 0 on initialization and when EDV1 = 1. To prevent overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of RM and can continue increasing after RM has decremented to 0. Prior to RM = 0 (empty battery), both discharge and self-discharge increment the DCR. After RM = 0, only discharge increments the DCR. The DCR resets to 0 when RM = FCC. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new FCC value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charge initiations (charges greater than 10mAh, where $V_{SRO} > V_{SRQ}$) occurred during the period between RM = FCC and EDV1 detected.
   - The self-discharge count is not more than 256mAh.
   - The temperature is ≥ 273°K when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for FCC update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2040 increments RM at a rate proportional to V_{SRO} and, if enabled, activates an LED display. Charge actions increment the RM after compensation for charge rate and temperature.

The bq2040 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 10 mAh. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the RM register to decrement and the DCR to increment. Exceeding the user-programmable discharge display threshold, stored in external E^2PROM, activates the display, if enabled. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2040 continuously decrements RM and increments DCR for self-discharge based on time and temperature. The self-discharge rate is dependent on the battery chemistry. The bq2040 self-discharge estimation rate is externally programmed in E^2PROM and can be programmed from 0 to 25% per day at 20°C. This rate doubles every 10°C from 0°C to 70°C.

Count Compensations

The bq2040 determines fast charge when the charge rate exceeds the programmed fast charge rate. Charge activity is compensated for temperature and rate before updating the RM and/or DCR. Discharge rate is compensated for temperature before updating the RM register. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for rate, temperature, and battery chemistry. For Li-ion chemistry cells, the charge efficiency is unity for all cases. However, the charge efficiency for nickel chemistry cells is adjusted using the following equation:

$$Q_{EFF} = Q_{EB} + 0.125 * \frac{\text{AverageCurrent()}}{\text{FullCapacity()}}$$

where $Q_{EB} = 0.80$ if $T < 30°C$

$Q_{EB} = 0.75$ if $30°C \le T < 40°C$

$Q_{EB} = 0.60$ if $T \ge 40°C$

and AverageCurrent() $\le$ FullCapacity()

$Q_{EFF} = Q_{EB} + 0.125$ if AverageCurrent() > FullCapacity()

Digital Magnitude Filter

The bq2040 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. Table 2 shows typical digital filter settings. The proper digital filter setting can be calculated using the following equation.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a valid discharge occurs and FCC is updated (see the DCR description on page 6). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

Remaining Capacity Compensation

The bq2040 adjusts the RM as a function of temperature. This adjustment accounts for the reduced capacity of the battery at colder temperatures. The following equation is used to adjust RM:

If $T \ge 5°C$

RemainingCapacity () = NominalAvailableCapacity()

If $T < 5°C$

RC() = NAC() (1 + TCC * (T - 5°C))

where T = temperature °C

TCC = 0.016 for Li-Ion cells

TCC = 0.0004 for Ni chemistry cells

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Display

The bq2040 can directly display capacity information using low-power LEDs. The bq2040 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the FCC. Each LED segment represents 20% of the FCC. The sixth segment, SEG_6, is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial design capacity. In absolute mode, each segment represents 20% of the design capacity, with SEG_6 representing "overfull" (charge above the design capacity). As the battery wears out over time, it is possible for the FCC to be below the initial design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The displayed capacity is compensated for the present battery temperature. The displayed capacity will vary as temperature varies, indicating the available charge at the present conditions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-6} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2040 recognizes a valid charge or if the discharge rate exceeds the programmed fast discharge display threshold. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SR} has been detected to be below V_{EDV1} (EDV_1 = 1), indicating a low-battery condition. V_{SR} below V_{EDVF} (EDV_F = 1) disables the display output.

Microregulator

The bq2040 can operate directly from 3 or 4 nickel chemistry cells. To facilitate the power supply requirements of the bq2040, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2040 can be inexpensively built using the FET and an external resistor; see Figure 1.

Communicating With the bq2040

The bq2040 includes a simple two-pin (SMBC and SMBD) serial data interface. A host processor uses the interface to access various bq2040 registers. This allows battery characteristics to be easily monitored, by adding two contacts to the battery pack. The open-drain SMBD and SMBC pins on the bq2040 are pulled up by the host system, or may be connected to V_{SS}, if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends the smart battery address and an eight-bit command byte to the bq2040. The command directs the bq2040 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2040 Data Protocols

The SMBus Host, acting in the role of an SMBus master, uses the read word and write word protocols to communicate integer data with the bq2040. The read block protocol is used to access block data, such as ManufacturerName(). When the bq2040 needs to inform the SMBus Host about an alarm condition or to inform the Smart Battery Charger about its desired charging voltage or current, the bq2040, acting as an SMBus master, uses the write word protocol to communicate with the SMBus Host or Smart Battery Charger acting as an SMBus slave.

Table 3. bq2040 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

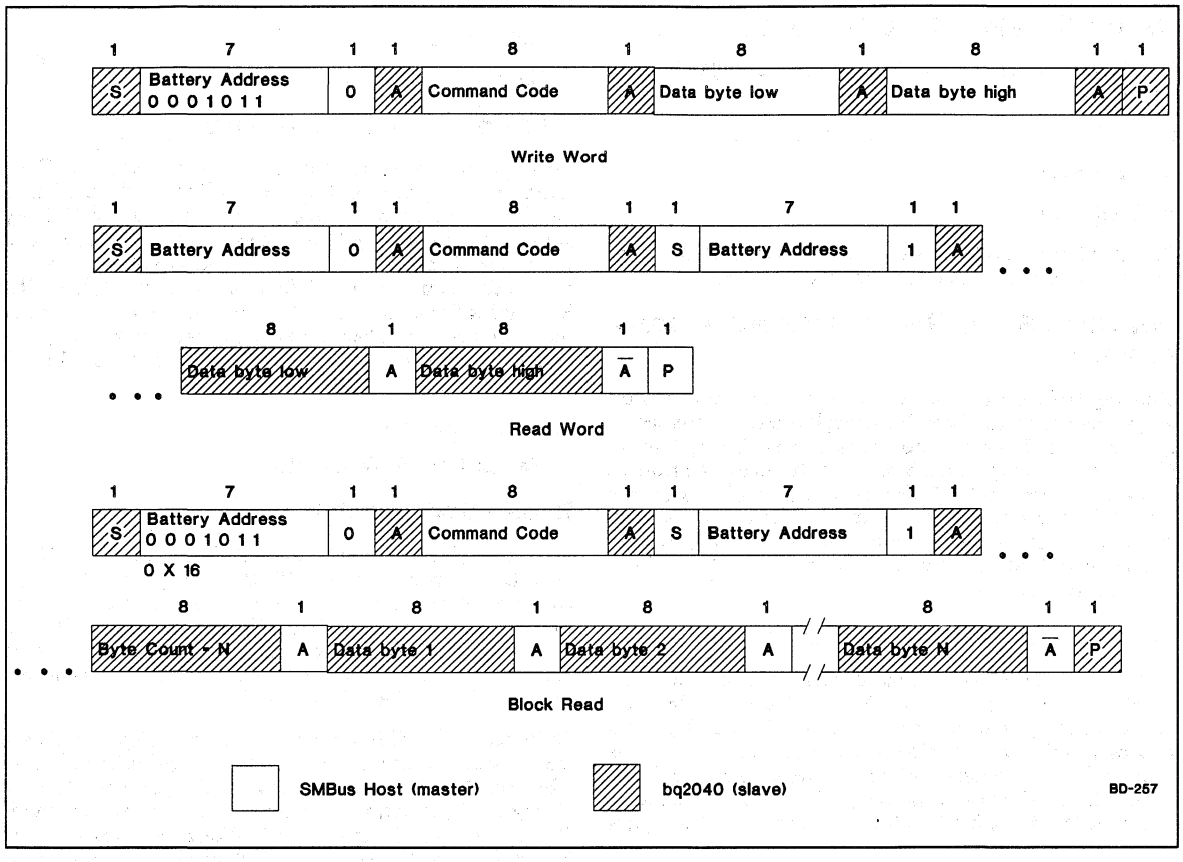


Figure 3. SMBus Host Protocols

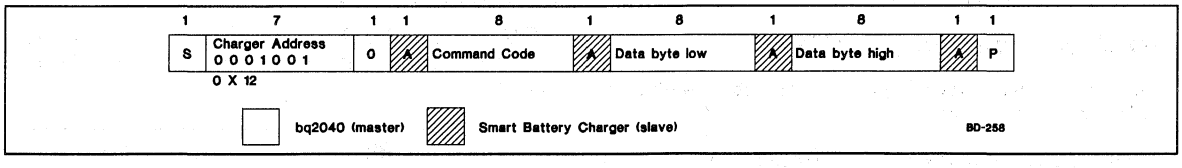


Figure 4. bq2040-to-Smart Battery Charger Message Protocol

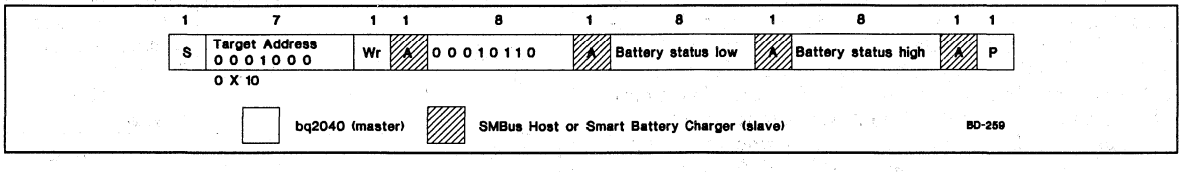


Figure 5. bq2040-to-Bus Host Message Protocol

SMBus Host-to-bq2040 Message Protocol

The SMBus Host communicates with the bq2040 using one of three protocols:

- Read word
- Write word
- Read block

The particular protocol used is a function of the command. The protocols used are shown in Figure 3.

bq2040-to-Smart Battery Charger Message Protocol

The bq2040, acting as an optional SMBus master, sometimes tries to alter the charging characteristics. It also may send critical messages to the Smart Battery Charger, behaving as an SMBus slave using the SMBus write word protocol. Communication begins with the Smart Battery Charger's address, followed by a command code and a two-byte value. The Smart Battery Charger adjusts its output to correspond with the request. See Figure 4.

bq2040 Critical Message Protocol

The bq2040 to SMBus Host message is sent using the SMBus write word protocol. Communication begins with the SMBus Host's address, followed by the bq2040's address, which also replaces the command code. The SMBus Host or Smart Battery Charger can now determine that the bq2040 was the originator of the message and that the following 16 bits are its status. See Figure 5.

SMBus Host-to-Smart Battery Messages (see Table 7)

ManufacturerAccess() (0x00)

This read or write word is optional and its meaning is implementation specific.

RemainingCapacityAlarm() (0x01)

This read or write word sets or gets the LowCapacity threshold value. Whenever the RemainingCapacity() falls below the RemainingCapacity alarm value, the Smart Battery sends AlarmWarning() messages to the SMBus Host with the REMAINING_CAPACITY_ALARM bit set. A value of 0 disables this alarm. The value is set to 10% of the design capacity at time of manufacture. The value will remain unchanged until altered by the RemainingCapacityAlarm() function.

Units: mAh

Range: 0 to 65,535 mAh

RemainingTimeAlarm() (0x02)

This read/write word sets or gets the RemainingTime alarm value. Whenever the AverageTimeTo Empty() falls below the RemainingTime value, the Smart Battery sends AlarmWarning() messages to the SMBus Host with the REMAINING_TIME_ALARM bit set. A RemainingTime value of 0 disables this alarm. The RemainingTime alarm is set to 10 minutes at the time of manufacture. The RemainingTime alarm value may be changed until altered by the RemainingTimeAlarm() function.

Units: Minutes

Range: 0 to 65,535 minutes

BatteryMode() (0x03)

This read/write word selects the various battery operational modes. The bq2040 supports the battery's capacity information specified in mAh. This function also determines whether the ChargingCurrent() and ChargingVoltage() values are broadcast to the Smart Battery Charger when the Smart Battery requires charging (CHARGER_MODE bit).

CHARGER_MODE bit enables or disables the Smart Battery's transmission of ChargingCurrent() and ChargingVoltage() messages to the Smart Battery Charger. When set, the Smart Battery will *not* transmit ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger. When cleared, the Smart Battery will transmit the ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger when charging is desired.

CAPACITY_MODE bit indicates that capacity information will be reported in mAh and current is in mA units.

Field	Bits Used	Format	Allowable Values
Reserved	0–13		
CHARGER_MODE	14	bit flag	0-Enable broadcast to charger 1-Disable broadcast to charger
CAPACITY_MODE	15	bit flag	0-Report in mA or mAh

AtRate() (0x04)

This read/write word is the first half of a two-function set used to set the AtRate value used in calculations made by the AtRateTimeToFull(), and AtRateTimeTo Empty().

- When the AtRate value is positive, the AtRateTimeTo-Full() function returns the predicted time to full-charge at the AtRate value of charge.
- When the AtRate value is negative, the AtRateTimeTo Empty() function returns the predicted operating time at the AtRate value of discharge.

Units: mA

Range: -32,768 mA to 32,767 mA

Note: The AtRate value is set to zero at time of manufacture (default).

AtRateTimeToFull() (0x05)

This read-only word returns the predicted remaining time to fully charge the battery at the AtRate value (mA).

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Invalid Data Indication: 65,535 indicates the battery is not being charged

AtRateTimeToEmpty() (0x06)

This read-only word returns the predicted remaining operating time if the battery is discharged at the AtRate value.

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Invalid Data Indication: 65,535 indicates the battery is not being discharged

AtRateOK() (0x07)

This read-only word returns a Boolean value that indicates whether or not the EDV_1 flag has been set.

Boolean: Indicates if the battery can supply additional energy

Units: Boolean

Range: TRUE ≠ 0 ,FALSE = 0

Temperature() (0x08)

This read-only word returns the cell-pack's internal temperature (°K).

Output: unsigned int—cell temperature in tenths of degrees Kelvin increments

Units: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned int—battery terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

Granularity: 0.2% of design voltage

Accuracy: ±0.2% of design voltage

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed int—charge/discharge rate in mA —positive for charge, negative for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity() or better

Accuracy: ±0.2% of the Design Capacity

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. The AverageCurrent() function returns meaningful values after the battery's first minute of operation.

Output: signed int—charge/discharge rate in mA — positive for charge, negative for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity() or better

Accuracy: ±0.2% of the Design Capacity

MaxError() (0x0c)

This read-only word returns the expected margin of error (%).

Output: unsigned int—percent uncertainty

Units: %

Range: 0 to 100%

Granularity: 1% or better

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity() (%).

Output: unsigned int—percent of remaining capacity

Units: %

Range: 0 to 100%

Granularity: 1% or better

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity() (%). Note that AbsoluteStateOfCharge can return values greater than 100%.

Output: unsigned int—percent of remaining capacity

Units: %

Range: 0 to 65,535 %

Granularity: 1% or better

Accuracy: ±MaxError()

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned int—estimated remaining capacity in mAh

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of DesignCapacity() or better

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. The FullChargeCapacity() value is expressed in mAh at a C/5 discharge rate.

Output: unsigned int—estimated full charge capacity in mAh or 10mWh

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of design capacity or better

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty() value is calculated based on Current().

Output: unsigned int—minutes of operation left

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is being charged

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent().

Output: unsigned int—minutes of operation left

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is being charged

AverageTimeToFull() (0x13)

This read-only word returns the predicted time until the Smart Battery reaches full charge at the present average charge rate (minutes).

Output: unsigned int—remaining time in minutes

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is not being charged

BatteryStatus() (0x16)

This read-only word returns The Smart Battery's status word (flags). Some of the BatteryStatus() flags (REMAINING_CAPACITY_ALARM and REMAINING_TIME_ALARM) are calculated based on current. See Table 4. for definitions.

unsigned int: Status Register with alarm conditions bit mapped as follows:

Alarm Bits	
0x8000	OVER_CHARGED_ALARM
0x4000	TERMINATE_CHARGE_ALARM
0x2000	DTEMP_ALARM
0x1000	OVER_TEMP_ALARM
0x0800	TERMINATE_DISCHARGE_ALARM
0x0400	reserved
0x0200	REMAINING_CAPACITY_ALARM
0x0100	REMAINING_TIME_ALARM
Status Bits	
0x0080	INITIALIZED
0x0040	DISCHARGING
0x0020	FULLY_CHARGED
0x0010	FULLY_DISCHARGED
Error Code	
0x0000–0x000f	reserved for error codes

CycleCount() (0x17)

This read-only word returns the number of charge/discharge cycles the battery has experienced. A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge, upon completion of a charge cycle. The bq2040 increments the cycle counter during the current charge cycle, if the battery has been discharged to below 85% of the state-of-charge at the end of the last charge cycle. A discharge > 0.5% prevents false reporting of small charge/discharge cycles.

Output: unsigned int—count of charge/discharge cycles the battery has experienced

Units: cycles

Range: 0 to 65,535 cycles; 65,535 indicates battery has experienced 65,535 or more cycles

Granularity: 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack. The DesignCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned int—battery capacity in mAh

Units: mAh

Range: 0 to 65,535 mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack (mV).

Output: unsigned int—the battery's normal terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

SpecificationInfo() (0x1a)

This read-only word returns the version number of the SmartBattery specification the battery pack supports, as well as voltage and current scaling information in packed integer. The SpecificationInfo is packed as follows: (major version number * 0x10 + minor version number) + (voltage scaling + current scaling * 0x10) * 0x100.

Field	Bits Used	Format	Allowable Value
Revision	0–3	4-bit binary value	0–15
Version	4–7	4-bit binary value	0–15
VScale	8–11	4-bit binary value	0–3 (multiplies voltage by 10 ^ VScale)
IPScale	12–15	4-bit binary value	0–3 (multiplies current/power by 10 ^ IPScale)

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980), month, day.

Field	Bits Used	Format	Allowable Value
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4-bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0 • 127 (corresponds to year biased by 1980)

SerialNumber() (0x1c)

This read-only word returns a serial number. This number, when combined with the ManufacturerName(), the DeviceName(), and the ManufactureDate(), uniquely identifies the battery (unsigned int).

Output: unsigned int

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The character string contains the battery manufacturer's name. For example, "BattCorp" identifies the Smart Battery manufacturer as BattCorp.

Output: string—character string

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's name. For example, a DeviceName() of "MBC301" indicates that the battery is a model BC301.

Output: string—character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's chemistry. For example, if the DeviceChemistry() function returns "NiMH," the battery pack contains nickel metal hydride cells.

Output: string—character string

ManufacturerData() (0x23)

This read-only string allows access to an up to 15-byte manufacturer data string.

Output: block data—data whose meaning is assigned by the Smart Battery's manufacturer

bq2040 or SMB Host-to-Smart Battery Charger Messages(See Table 6)

Whenever the BatteryMode() CHARGER_MODE bit is set to zero (default) and the bq2040 detects the presence of a Smart Battery Charger (level 2 charger—refer to the Smart Battery Charger Specification), the bq2040 sends the ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger. The bq2040 continues broadcasting these values at whatever interval it deems appropriate to maintain correct charging. For example, the bq2040 detects the presence of a Smart Battery Charger by recognizing a charge current. See BatteryMode().

ChargingCurrent() (0x14)

The bq2040 sends the desired charging rate to the Smart Battery Charger (mA).

Output: unsigned int—maximum charger output current in mA

Units: mA

Range: 0 to 65,534 mA

Granularity: 0.2% of the design capacity or better

Accuracy: -± 0.2% of the design capacity

Invalid data indication: 65,535 indicates the Smart Battery Charger should operate as a voltage source outside its maximum regulated current range

ChargingVoltage() (0x15)

The bq2040 sends the desired voltage to the Smart Battery Charger (mV).

Output: unsigned int—charger output current in mV

Units: mV

Range: 0 to 65,534 mV

Granularity: 0.2% of the design voltage or better

Accuracy: -± 0.2% of the design voltage

Invalid data indication: 65,535 indicates the Smart Battery Charger should operate as a current source outside its maximum regulated voltage range

bq2040 Critical Messages

Whenever the bq2040 detects a critical condition, it becomes a bus master and sends AlarmWarning() messages to both the Smart Battery Charger, if enabled, and the SMBus Host, as appropriate, notifying them of the critical condition(s). The message sent by the AlarmWarning() function is similar to the message returned by the BatteryStatus() function. The bq2040 continues broadcasting the AlarmWarning() messages at 10-second intervals until the critical condition(s) has been corrected.

AlarmWarning() (0x16)

The bq2040, acting as a bus master device to the SMBus Host and/or the Smart Battery Charger, sends this message to notify them that one or more alarm conditions exist. Alarm indications are encoded as bit fields in the Battery's status, which is then sent to the SMBus Host and/or Smart Battery Charger by this function. The AlarmWarning() is repeated at 10-second intervals until the condition(s) causing the alarm has been corrected.

Output: unsigned int—Status Register with alarm conditions bit mapped as follows:

Alarm Bits	
0x8000	OVER_CHARGED_ALARM
0x4000	TERMINATE_CHARGE_ALARM
0x2000	DTEMP_ALARM
0x1000	OVER_TEMP_ALARM
0x0800	TERMINATE_DISCHARGE_ALARM
0x0400	reserved
0x0200	REMAINING_CAPACITY_ALARM
0x0100	REMAINING_TIME_ALARM
Status Bits	
0x0080	INITIALIZED
0x0040	DISCHARGING
0x0020	FULLY_CHARGED
0x0010	FULLY_DISCHARGED
Error Code	
0x0000–0x000f	All bits set high prior to AlarmWarning() transmission

Note: Alarm bits 0x0200 and 0x0100 cause the AlarmWarning() to be sent only to the SMBus Host. All other alarm bits cause the AlarmWarning() to be sent to both the SMBus Host and the Smart Battery Charger, if CHARGER_MODE = 0.

Status Bits and Error Codes

Status bits are listed in Table 4 and error codes are listed in Table 5.

Table 4. Status Bits

Alarm Bits		
Bit Name	**Set When:**	**Reset When:**
OVER_CHARGED_ALARM	bq2040 detects that it is being charged beyond an end-of-charge indication	bq2040 detects that it is no longer being overcharged
TERMINATE_CHARGE_ALARM **Note:** Failure to correct the problem may result in permanent damage to the battery.	bq2040 detects that one or more of its charging parameters are out of range (for example, its voltage or current is too high)	Parameter falls back into the allowable range
DTEMP_ALARM	bq2040 detects that the rate of its internal thermal rise ($\Delta T/\Delta t$) is greater than 1.25°C/min	Rate of thermal rise falls back into the acceptable range($T < 50°C$)
OVER_TEMP_ALARM	bq2040 detects that its internal temperature is greater than 60°C	Internal temperature falls back into the acceptable range
TERMINATE_DISCHARGE_ALARM	bq2040 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	Battery reaches a state of charge sufficient for it to once again safely supply power
REMAINING_CAPACITY_ALARM	bq2040 detects that the RemainingCapacity() is less than that set by the RemainingCapacity() function	Either the value set by the RemainingCapacityAlarm() function is lower than the Remaining Capacity() or the RemainingCapacity() is increased by charging
REMAINING_TIME_ALARM	bq2040 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm() function	Either the value set by the RemainingTimeAlarm() function is lower than the AverageTimeToEmpty() or the AverageTimeToEmpty() is increased by charging
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	bq2040 is set when the bq2040 has reached a full or empty state	Battery detects that power-on or user-initiated reset has occurred
DISCHARGING	bq2040 determines that it is not being charged	Battery detects that it is being charged
FULLY_CHARGED	bq2040 determines that it has reached a charge termination point	Battery may be charged again
FULLY_DISCHARGED	bq2040 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	RelativeStateOfCharge() is greater than or equal to 20%

Table 5. Error Codes

Error	Code	Access	Description
OK	0x0000	read/write	bq2040 processed the function code without detecting any errors
Busy	0x0001	read/write	bq2040 is unable to process the function code at this time
NotReady	0x0002	read/write	bq2040 can not read or write the data at this time—try again later
UnsupportedCommand	0x0003	read/write	bq2040 does not support the requested function code
AccessDenied	0x0004	write	bq2040 detected an attempt to write to a read-only function code
Overflow/Underflow	0x0005	read/write	bq2040 detected a data overflow or underflow
BadSize	0x0006	write	bq2040 detected an attempt to write to a function code with an incorrect size data block
UnknownError	0x0007	read/write	bq2040 detected an unidentifiable error

Table 6. bq2040 Master Functions

Function	Code	Access	Data
ChargingCurrent (to Smart Battery Charger)	0x14	write	mA
ChargingVoltage (to Smart Battery Charger)	0x15	write	mV
AlarmWarning (to SMBus Host)	0x16	write	word
AlarmWarning (to Smart Battery Charger)	0x16	write	word

Table 7. Smart Battery Slave Functions

Function	Code	Access	Units	Defaults
ManufacturerAccess	0x00	read/write	word	
RemainingCapacityAlarm	0x01	read/write	mAh	0.1* DC
RemainingTimeAlarm	0x02	read/write	minutes	000Ah
BatteryMode	0x03	read/write	bit flags	0000h
AtRate	0x04	read/write	mA	0000h
AtRateTimeToFull	0x05	read	minutes	FFFFh
AtRateTimeToEmpty	0x06	read	minutes	FFFFh
AtRateOK	0x07	read	Boolean	0000h
Temperature	0x08	read	0.1°K	-
Voltage	0x09	read	mV	-
Current	0x0a	read	mA	0000h
AverageCurrent	0x0b	read	mA	0000h
MaxError	0x0c	read	percent	2%
RelativeStateOfCharge	0x0d	read	percent	0000h
AbsoluteStateOfCharge	0x0e	read	percent	0000h
RemainingCapacity	0x0f	read	mAh	0000h
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	-
AverageTimeToEmpty	0x12	read	minutes	-
AverageTimeToFull	0x13	read	minutes	-
ChargingCurrent	0x14	read	mA	E^2
ChargingVoltage	0x15	read	mV	E^2
BatteryStatus	0x16	read	bit flags	0050h
CycleCount	0x17	read	count	0000h
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	0x19	read	mV	E^2
SpecificationInfo	0x1a	read	unsigned int	E^2
ManufactureDate	0x1b	read	unsigned int	E^2
SerialNumber	0x1c	read	number	E^2
Reserved	0x1d - 0x1f	-	-	-
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2
DeviceChemistry	0x22	read	string	E^2
ManufacturerData	0x23	read	string	E^2

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2040 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (T_A = T_{OPR}; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-30mV	-	30mV	V	See note

Note: The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset, stored in external E^2PROM. For proper operation, V_{CC} should be 1.5V greater than V_{SB}.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LVOUT}	V_{OUT} output leakage	-0.2	-	0.2	µA	E^2PROM off
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = discharge; $V_{SR} > V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	1.4	-	5.5	V	SCL, SDA, SMBC, SMBD
V_{IL}	Logic input low	-0.5	-	0.6V	V	SCL, SDA, SMBC, SMBD
V_{OL}	Data, clock output low	-	-	0.4	V	I_{OL}=350µA, SDA, SMBD
I_{OL}	Sink current	100	-	350	µA	V_{OL}≤0.4V, SDA, SMBD
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHVL}	V_{OUT} output, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{VOUT} = -33.0mA
I_{VOUT}	V_{OUT} source current	-33	-	-	mA	At $V_{OHVH} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V

Note: All voltages relative to V_{SS}.

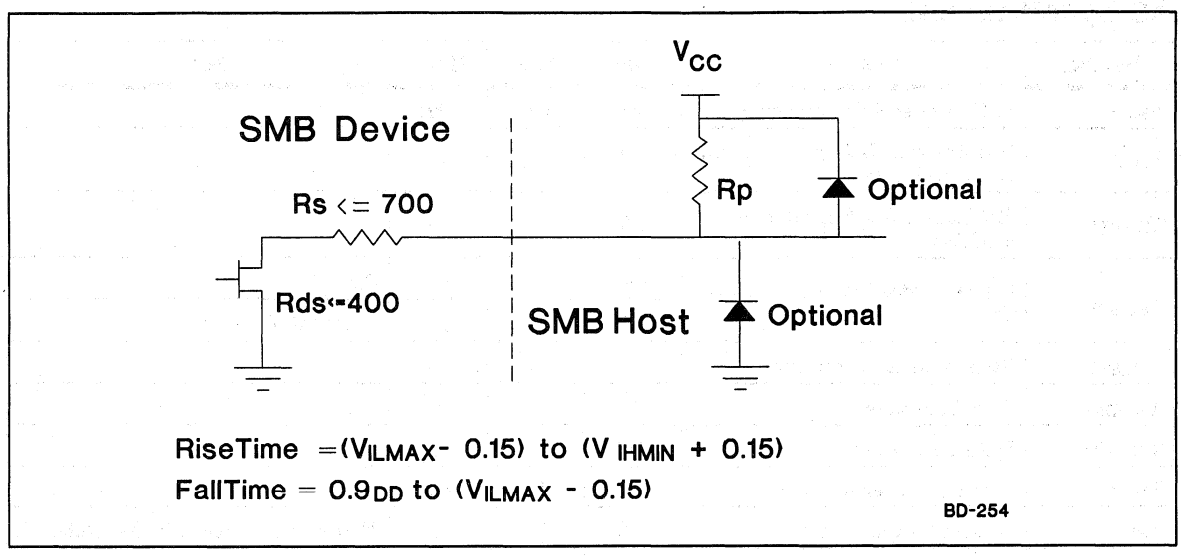


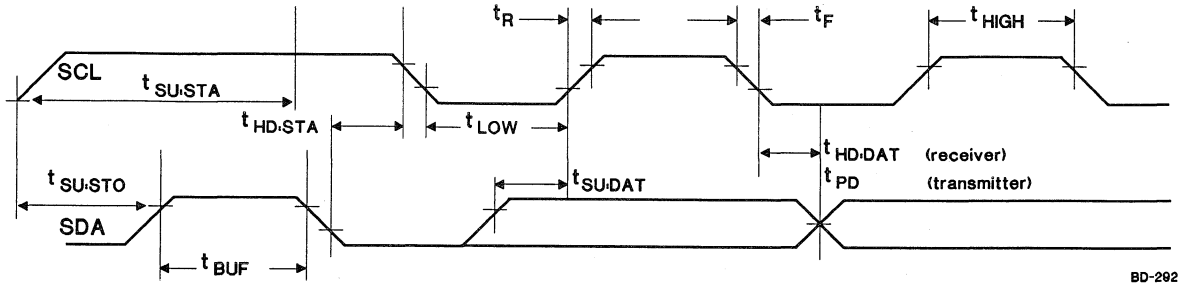
Figure 6. AC Test Conditions

AC Specifications

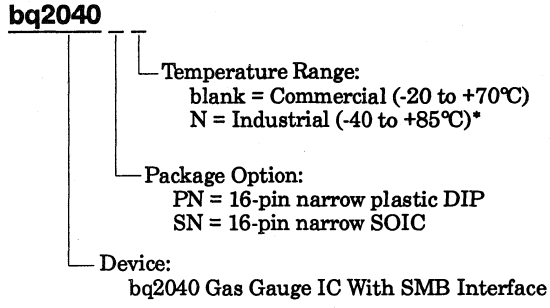
Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7		µs	
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition setup time	250		ns	SMBD
		4.7		µs	External Memory
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	0		ns	
$T_{SU:DAT}$	Data setup time	250		ns	
T_{HOG}	Message buffering time		20	ms	
T_{PD}	Data output delay time	300	3500	ns	External memory only. See Note.
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0		µs	
T_F	Clock/Data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	

Note: The external memory must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Bus Timing Data



Ordering Information



* Contact factory for availability.

Lithium Ion Power Gauge™ IC

Features

- Conservative and repeatable measurement of available capacity in Lithium Ion rechargeable batteries
- Designed for battery pack integration
  - 120µA typical standby current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow DIP or SOIC

General Description

The bq2050 Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of the battery's available capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

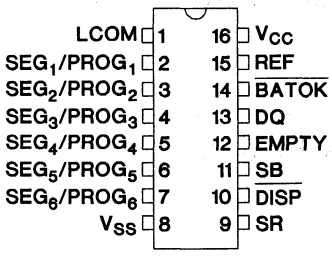
Nominal available capacity may be directly indicated using a five- or six-segment LED display. These segments are used to graphically indicate nominal available capacity.

The bq2050 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2050 outputs battery information in response to external commands over the serial link.

The bq2050 may operate directly from one cell (V_{BAT} > 3V). With the REF output and an external transistor, a simple, inexpensive regulator can be built for systems with more than one series cell.

Internal registers include available capacity, temperature, Watt-hour capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2050 power gauge data registers.

Pin Connections

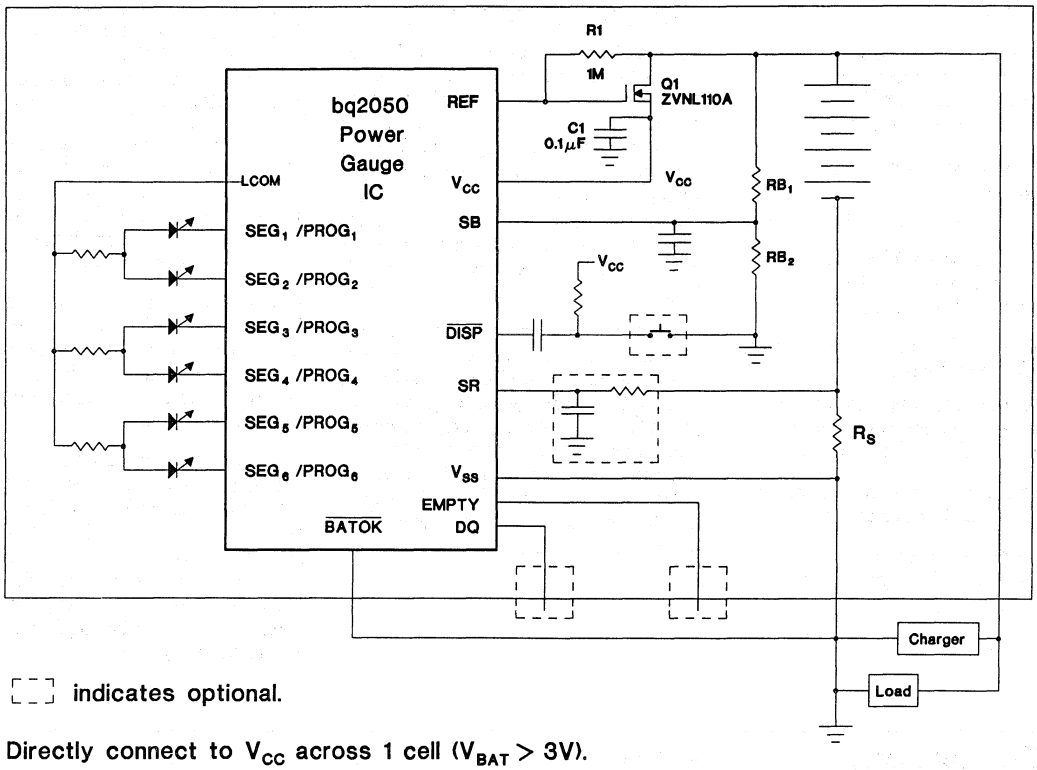


16-Pin Narrow DIP
or Narrow SOIC

PN-65

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	$\overline{BATOK}$	Battery stack OK output
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	EMPTY	Empty battery indicator output
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
$SEG_6/PROG_6$	LED segment 6/ program 6 input	SR	Sense resistor input
		V_{CC}	3.0-6.5V
		V_{SS}	System ground



[ ] indicates optional.

Directly connect to V_{CC} across 1 cell ($V_{BAT} > 3V$).

Otherwise, R1, C1, and Q1 are needed for regulation of > 1 cell.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required, application-specific.

BD-224

Figure 1. Battery Pack Application Diagram—LED Display

Lithium Ion Pack Supervisor

Features

- Protects two to four Lithium Ion series cells from overvoltage, undervoltage, and short circuit
- Designed for battery pack integration
  - Small outline package, minimal external components and space, and low cost
  - Drives external N-FET switches
- Precision internal reference adjustment
- Very low operating current, < 1µA
- 8-pin 150-mil SOIC, 300-mil DIP

General Description

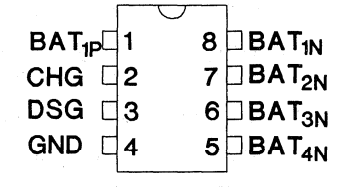
The bq2053 Lithium Ion Pack Supervisor is designed to control the charge and discharge voltage safety limits for two to four lithium ion (Li-Ion) series cells, accommodating battery packs containing series/parallel configurations. The very low operating current doesl not overdischarge the cells during periods of storage, and does not significantly increase the system discharge load. Packaged in an 8-pin narrow SOIC, the bq2053 can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2053 controls two external N-FETs to limit the charge and discharge potentials. Charging is allowed when the per cell voltage is below V_{OV} (overvoltage limit). When the cell voltage on any cell rises above V_{OV}, CHG goes active low, shutting off the charge to the battery pack. This safety feature prevents overcharge on any individual series cell stack within the battery pack.

When the battery cell voltage is below V_{OV}, discharge and charge are allowed. If the voltage across any cell falls below V_{UV} (undervoltage limit), the DSG output goes active, shutting off the battery discharge. This safety feature prevents overdischarge on any individual series cell stack within the battery pack.

V_{UV} and V_{OV} are programmed at Benchmarq. The default limits are 2.3V and 4.25V, respectively.

Pin Connections



8-Pin Narrow DIP or SOIC

PN-86

Pin Names

BAT_{1P}	Battery 1 positive input
BAT_{1N}	Battery 1 negative input
BAT_{2N}	Battery 2 negative input
BAT_{3N}	Battery 3 negative input
BAT_{4N}	Battery 4 negative input
DSG	Discharge disable
CHG	Charge disable
GND	Ground

BENCHMARQ

Advance Information **bq2054**

Lithium Ion Fast Charge IC

Features

- Safe charge of Lithium Ion battery packs
- Pulse width modulation regulator
  - Ideal for high-efficiency switch mode designs
  - Configurable for linear or gated current regulation use
- Temperature compensated voltage limits
- Pin-selectable charge controller
  - Constant voltage current limited charging profiles
  - Charging controlled by internal timer modes
- Charging qualified by temperature and voltage range limits
- Pin-selectable internal charge voltage and current thresholds reduce external components and increase accuracy
- Fast charge terminated by minimum current at the maximum voltage limit; safety termination using maximum time or temperature
- Direct-drive LED outputs display charge status and fault conditions

General Description

The bq2054 monolithic CMOS IC optimizes the charging of lithium ion (Li-Ion) chemistry batteries. The flexible pulse-width modulation regulator can be used to control constant-voltage or constant-current charging. The regulator frequency is set by external components to offer flexibility to control EMI. The switch-mode design keeps power dissipation to a minimum while delivering high efficiency for high-charge-current requirements.

The bq2054 extends battery life by using temperature-compensated voltage thresholds, which are used during constant-voltage charging. The bq2054 accurately measures battery temperature using an external probe for charge qualification and for charge voltage temperature compensation.

The bq2054 begins charging when it receives power or on battery insertion. For safety, the bq2054 inhibits charging until the battery voltage and temperature are within configured range limits. If the voltage is less than the low-voltage threshold, the bq2054 provides trickle-current conditioning of the battery. The conditioning algorithm validates charge acceptance by sensing an increase in both current and voltage. This prevents fast charging of possibly damaged or reversed cells.

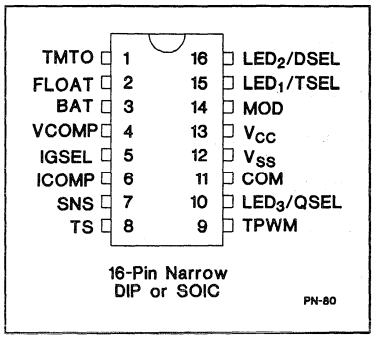
The bq2054 charge controller automatically sequences through several charge modes based on the battery voltage and charging current conditions. These include conditioning, current-limited charging, and voltage-regulation charging.

The constant-voltage charging begins with a current-limited interval that typically replenishes up to 80% of the charge, and a voltage-regulated period that returns the remaining charge.

The bq2054 controls charging by using an integrated maximum time-out (MTO) charge safety timer. The MTO timer terminates charging with one or two termination values depending on the pin-selectable charge mode. The timer timebase uses and external RC time constant that allows for timed charge control and prevents overcharging.

The bq2054 provides status indications of all charger states and faults for accurate determination of the battery and charge system conditions.

Pin Connections



16-Pin Narrow DIP or SOIC

PN-80

Pin Names

TMTO	Time-out timebase	COM	Common LED output
FLOAT	State control	LED_3/ TSEL	Charge status output 3/ charge termination select
BAT	Battery voltage	V_{SS}	System ground
VCOMP	Voltage loop	V_{CC}	5.0V ± 10% power
IGSEL	Current gain select	MOD	Modulation control
ICOMP	Current loop comp	LED_1/ TSEL	Charge status output 1/ Termination select
SNS	Sense resistor input	LED_2/ DSEL	Charge status output 2/ Display select
TS	Temperature sense		
TPWM	Regulator timebase		

Preliminary **bq2900**

Rechargeable Alkaline Charge IC

Features

- Safe charge of two rechargeable alkaline batteries such as Renewal® from Rayovac®
- Pulsed charge terminated with maximum voltage limit
- LED charge status outputs
- Pin-selectable low-battery cut-off
- Optional external FET drive
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2900 is a low-cost charger for rechargeable alkaline batteries such as Renewal® batteries from Rayovac®. The bq2900 combines sensitive, full-charge detection for two rechargeable alkaline cells, with a low-battery cut-off for cost-effective battery management.

Designed for system integration, the bq2900 can improve the service life of the rechargeable alkaline cells by individually charging each cell. The bq2900 uses a current-limited supply to generate the proper charge pulses. Each cell is individually monitored to ensure full charge and maintain cell matching.

Charge completion is indicated when both cells have individually skipped at least 16 charge pulses in a row. A status output is provided to indicate charge in progress, charge complete, or fault indication.

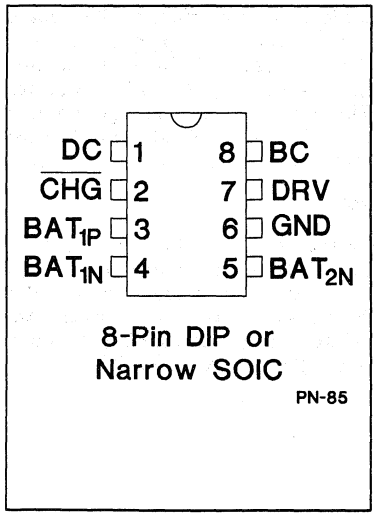
The bq2900 avoids over-depleting the battery by using the internal low-battery detection circuit. The bq2900 also eliminates the external power switching transistors needed to separately charge individual Renewal® cells.

To reduce cost, the discharge and charge control FETs are internal to the bq2900. An optional DRV pin is provided to drive an external N-FET, reducing the effective R_{DSON} for the system, if needed.

The BC pin is designed to be used with an external capacitor, provding power to the bq2900 during charge if the rechargeable alkaline cells are severely depleted.

For safety, charging is inhibited if the per-cell voltage is greater than 3.0V during charge (closed-circuit voltage), or if the cell voltage is less than 0.4V (open-circuit voltage).

Pin Connections



Pin Names

DC	Charging supply input	BAT_{2N}	Battery 2 negative input
$\overline{CHG}$	Battery status output 1	GND	Charging supply return
BAT_{1P}	Battery 1 positive input	DRV	External FET drive output
BAT_{1N}	Battery 1 negative input	BC	Backup capacitor

Pin Descriptions

DC **DC supply input**

This input is used to recharge the individual rechargeable alkaline cells and is limited to 3.0V at 300mA.

$\overline{CHG}$ **Charge status**

This open-drain output is used to signify battery charging and is valid only when DC is applied.

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 2).

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 2).

BAT_{2N} **Battery 2 negative terminal**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 2).

GND **Charging supply return**

This input is the DC ground.

DRV **External FET drive output**

This output drives an optional external FET on the ground side of the battery stack (see Figure 2).

BC **Backup capacitor**

This pin uses an external capacitor, typically a 1µf, to supply the bq2900 during periods when the DC input voltage may fall below 2.0V.

Functional Description

Figure 1 illustrates the charge control and display status during a bq2900 cycle. Table 1 outlines the various operational states and their associated conditions which are described in detail in the following section.

Charging

The bq2900 controls the current pulses to properly charge two rechargeable alkaline cells. The charge current is derived from a current-limited DC input and is pulsed at approximately 100 Hz on the BAT_{1P}, and BAT_{1N} pins. The DC current input must be limited to less than 3.0V and 300mA.

The bq2900 charge cycle is controlled by inputs from DC and $BAT_{1P,1N}$. The charge cycle begins with the application of a valid DC input. The bq2900 checks the open-circuit voltage (V_{OCV}) of each cell for an undervoltage condition (V_{MIN} < 0.4V) and begins a charge cycle if V_{OCV} is above V_{MIN}. If V_{OCV} of any cell is below V_{MIN}, the bq2900 enters a charge-pending mode and indicates a fault condition (see Table 1). The bq2900 remains in a charge-pending mode until V_{OCV} of each cell is above V_{MIN}.

The bq2900 charges the rechargeable alkaline battery by pulsing each cell individually for 5ms every 10ms. The bq2900 measures the open circuit voltage (V_{OCV}) of each battery during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ± 3%), the following pulses are skipped until the cell potential is below the V_{MAX} limit. This method allows full charge of individual cells, providing cell equalization at the end of charge.

Charging is terminated for an individual cell when greater than 16 pulses in a row are skipped. Charging is immediately terminated if V_{CCV} (closed-circuit voltage) is greater than 3.0V (V_{FLT}) and the $\overline{CHG}$ output indicates a fault condition (see Table 1). Once fast charging is terminated, the $\overline{CHG}$ output indicates charge complete (see Table 1). Charging is not re-initiated until either DC is removed and reapplied or V_{OCV} falls below 1.4V.

Low Battery Cut-off

The battery output remains valid until the single-cell voltage of either battery falls below the end-of-discharge voltage, 0.9V. If the bq2900 determines an overdischarge condition, the internal switch disconnects the battery from the discharge load. The DRV pin is also driven low to turn off an optional external FET.

Battery Protection

The bq2900 contains internal reverse cell protection; the bq2900 will not attempt to charge reversed batteries.

Note: Make sure to provide adequate system protection in case of cell reversal.

Charge Status Indication

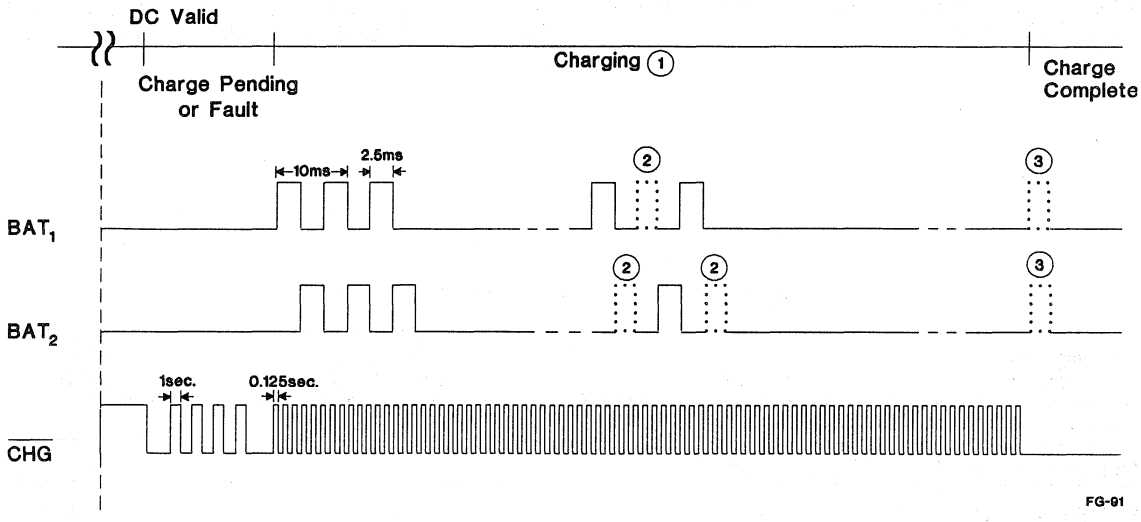
Table 1 outlines the various action states and the associated $BAT_{1P,1N}$ and $\overline{CHG}$ states. The $\overline{CHG}$ output may be connected directly to an LED indicator. In all cases, if the DC voltage at the DC pin is absent, the $\overline{CHG}$ output is held in a high-impedance condition.

2

Table 1. bq2901 Operational Summary

Charge Action State	Conditions	$BAT_{1P, 1N, 2N}$ Input/Outputs	$\overline{CHG}$ Output
DC absent	$V_{DC} = 0$	Low battery detection per V_{SEL}	Z
Charge initiation	DC applied, $V_{OCV} \leq 1.63V$[2]	-	-
Charge pending/ fault	$V_{OCV} < 0.4V$ or $V_{CCV} > 3.0V$[3]	-	1 sec = Low 1 sec = Z
Fast charging	$V_{OCV} \leq 1.63V$ before pulse	Charge pulsed @ 100Hz per Figure 1	1/8 sec = Low 1/8 sec = Z
Pulse skip	V_{OCV} remains above 1.63 during pulse cycle	Pulse skipped per Figure 1	Low
Charge complete[1]	$V_{OCV} > 1.63V$ for greater than 160ms on both cells	Charge complete	Z

Notes:
1. Charge complete when charge is completed on both batteries.
2. V_{OCV} = Open-circuit voltage of each cell between positive and negative leads.
3. V_{CCV} = Closed-circuit voltage.



Notes:
1. Charging: $0.4 < V_{OCV} \leq 1.63V$, $V_{CCV} \leq 3.0V$.
2. Pulses skipped when $V_{OCV} > 1.63V$.
3. Charge complete when $V_{OCV} \geq 1.63V$ for > 160 ms (16 pulses) for all cells.

Figure 1. bq2900 Application Diagram

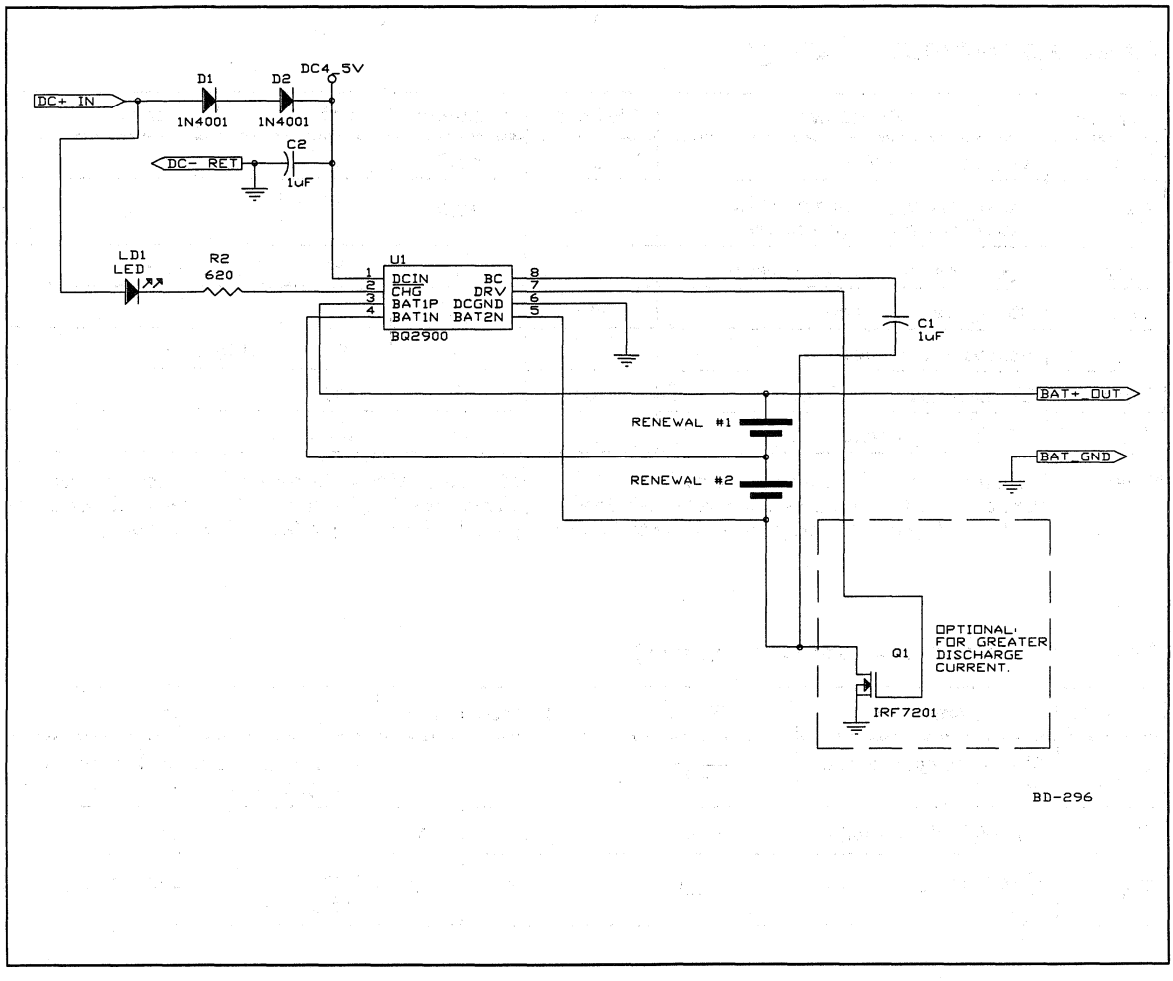


Figure 2. bq2900 Applications Example

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	
I_{DC}	DC charging current	-	400	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{DD} =4.5V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	V_{OCV} > V_{MAX} inhibits/terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90V	±5%	V	
V_{FLT}	Maximum open-circuit voltage	3.0V	±3%	V	V_{CCV} > V_{FLT} terminates charge, indicates fault

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{IH}	Logic input high	V_{CC} - 0.5	-	-	V	
V_{IL}	Logic input low	-	-	0.5	V	
V_{OL}	Logic output low	-	-	0.8	V	$\overline{CHG}$, DRV, I_{OC} = 10mA
I_{OL}	Output current	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V, $\overline{CHG}$
I_{CC}	Supply current	-	-	250	µA	Outputs unloaded, V_{DC} = 3.0V
I_{SB1}	Standby current	-	-	10	µA	V_{DC} = 0, V_{OCV} > V_{EDV}
I_{SB2}	End-of-discharge standby current	-	-	1	µA	V_{DRV} = 0
I_L	Input leakage	-	-	±1	µA	
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{CHG}$
R_{DSON}	On resistance	-	0.5	-	Ω	
V_{OH}	Gate drive output	TBD	-	-	V	DRV
I_{DC}	DC charging current	-	-	300	mA	
V_{DC}	DC charging voltage	-	3.0	-	V	

Note: All voltages relative to GND.

Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_P	Pulse timer	-	100	-	Hz	See Figure 3
t_{PW}	Pulse width	-	5	-	ms	See Figure 3

Note: Typical is at $T_A = 25°C$.

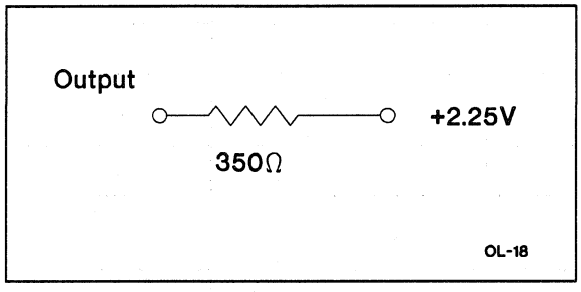


Figure 3. Output Load

Ordering Information

bq2900

- Temperature Range:
  - blank = Commercial (0 to +70°C)
  - N = Industrial (-40 to +85°C)
- Package Option:
  - PN = 8-pin narrow plastic DIP
  - SN = 8-pin narrow SOIC
- Device:
  - bq2900 Rechargeable Alkaline Charge IC

BENCHMARQ

Preliminary **bq2901**

Rechargeable Alkaline Charge IC

Features

- Safe charge of three or four rechargeable alkaline batteries such as Renewal® from Rayovac®
- Pulsed charge terminated with maximum voltage limit
- LED charge status outputs
- Pin-selectable low-battery cut-off
- Optional external FET drive
- 14-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2901 is a low-cost charger for rechargeable alkaline batteries such as Renewal® batteries from Rayovac®. The bq2901 combines sensitive, full-charge detection for three to four rechargeable alkaline cells, with a low-battery cut-off for cost-effective battery management.

Designed for system integration into a three- to four-cell system, the bq2901 can improve the service life of the rechargeable alkaline cells by individually charging each cell. The bq2901 uses a current-limited supply to generate the proper charge pulses. Each cell is individually monitored to ensure full charge and maintain cell matching.

Charge completion is indicated when all cells have individually skipped at least 16 charge pulses in a row. Status outputs are provided to indicate charge in progress, charge complete, or fault indication.

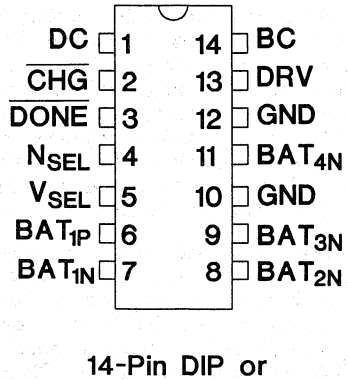
The bq2901 avoids over-depleting the battery by using the internal low-battery detection circuit. The bq2901 also eliminates the external power switching transistors needed to separately charge individual Renewal® cells.

To reduce cost, the discharge and charge control FETs are internal to the bq2901. An optional DRV pin is provided to drive an external N-FET, reducing the effective R_{DSON} for the system, if needed.

The BC pin is designed to be used with an external capacitor, provding power to the bq2901 during charge if the rechargeable alkaline cells are severely depleted.

For safety, charging is inhibited if the per-cell voltage is greater than 3.0V during charge (closed-circuit voltage), or if the cell voltage is less than 0.4V (open-circuit voltage).

Pin Connections



14-Pin DIP or Narrow SOIC

PN-81

Pin Names

DC	Charging supply input	BAT_{2N}	Battery 2 negative input
$\overline{CHG}$	Battery status output 1	BAT_{3N}	Battery 3 negative input
$\overline{DONE}$	Battery status output 2	BAT_{4N}	Battery 4 negative input
N_{SEL}	Number of cells input	GND	Charging supply return
V_{SEL}	End of discharge voltage select input	DRV	External FET drive output
		BC	Backup capacitor
BAT_{1P}	Battery 1 positive input		
BAT_{1N}	Battery 1 negative input		

Pin Descriptions

DC **DC supply input**

This input is used to recharge the individual rechargeable alkaline cells and is limited to 3.0V at 300mA.

$\overline{CHG}$ **Charge status**

This open-drain output is used to signify battery charging and is valid only when DC is applied.

$\overline{DONE}$ **Charge done**

This open-drain output is used to signify charge completion and is valid only when DC is applied.

N_{SEL} **Number of cells input**

This input selects whether the bq2901 charges 3 or 4 cells. V_{SEL} = BAT_{1P} selects 4 cells, and V_{SEL} = BAT_{4N} selects 3 cells.

V_{SEL} **End-of-discharge select input**

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2901. V_{SEL} = BAT_{1P} selects an EDV of 1.10V. V_{SEL} float selects EDV = 1.0V. V_{SEL} = BAT_{4N} selects EDV = 0.9V

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 2).

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 2).

BAT_{2N} **Battery 2 negative terminal**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 2).

BAT_{3N} **Battery 3 negative terminal**

This input connects to the negative terminal of the battery designated BAT_3 (see Figure 2).

BAT_{4N} **Battery 4 negative terminal**

This input connects to the negative terminal of the battery designated BAT_4 (see Figure 2).

GND **Charging supply return**

This input is the DC ground.

DRV **External FET drive output**

This output drives an optional external FET on the ground side of the battery stack (see Figure 2).

BC **Backup capacitor**

This pin uses an external capacitor, typically a 1µf, to supply the bq2901 during periods when the DC input voltage may fall below 2.0V.

Functional Description

Figure 1 illustrates the charge control and display status during a bq2901 cycle. Table 1 outlines the various operational states and their associated conditions which are described in detail in the following section.

Charging

The bq2901 controls the current pulses to properly charge three or four rechargeable alkaline cells. The charge current is derived from a current-limited DC input and is pulsed at approximately 100 Hz on the BAT_{1P}, BAT_{1N}, BAT_{2N}, and BAT_{3N} pins. The DC current input must be limited to less than 3.0V and 300mA.

The bq2901 charge cycle is controlled by inputs from DC and $BAT_{1P,1N,2N,3N}$. The charge cycle begins with the application of a valid DC input. The bq2901 checks the open-circuit voltage (V_{OCV}) of each cell for an undervoltage condition (V_{MIN} < 0.4V) and begins a charge cycle if V_{OCV} is above V_{MIN}. If V_{OCV} of any cell is below V_{MIN}, the bq2901 enters a charge-pending mode and indicates a fault condition (see Table 1). The bq2901 remains in a charge-pending mode until V_{OCV} of each cell is above V_{MIN}.

The bq2901 charges the rechargeable alkaline battery by pulsing each cell individually for 5ms every 10ms. The bq2901 measures the open circuit voltage (V_{OCV}) of each battery during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ± 3%), the following pulses are skipped until the cell potential is below the V_{MAX} limit. This method allows full charge of individual cells, providing cell equalization at the end of charge.

Charging is terminated for an individual cell when greater than 16 pulses in a row are skipped. Charging is immediately terminated if V_{CCV} (closed-circuit voltage) is greater than 3.0V (V_{FLT}) and the $\overline{CHG}$ output indicates a fault condition (see Table 1). Once fast charging is terminated, the $\overline{DONE}$ output becomes active. Charging is not re-initiated until either DC is removed and reapplied or V_{OCV} falls below 1.4V.

Low Battery Cut-off

The battery output remains valid until the single-cell voltage of any battery falls below the end-of-discharge voltage selected by the V_{SEL} pin. Table 2 outlines the three EDV selections for the bq2901. If the bq2901 determines an overdischarge condition, the internal switch disconnects the battery from the discharge load. The DRV pin is also driven low to turn off an optional external FET.

Table 2. bq2901 EDV Selections

End-of-Discharge Voltage	Pin Connection
1.10V	$V_{SEL} = BAT_{1P}$
1.00V	$V_{SEL} = Z$
0.90V	$V_{SEL} = BAT_{4N}$

Battery Protection

The bq2901 contains internal reverse cell protection; the bq2901 will not attempt to charge reversed batteries.

Note: Make sure to provide adequate system protection in case of cell reversal.

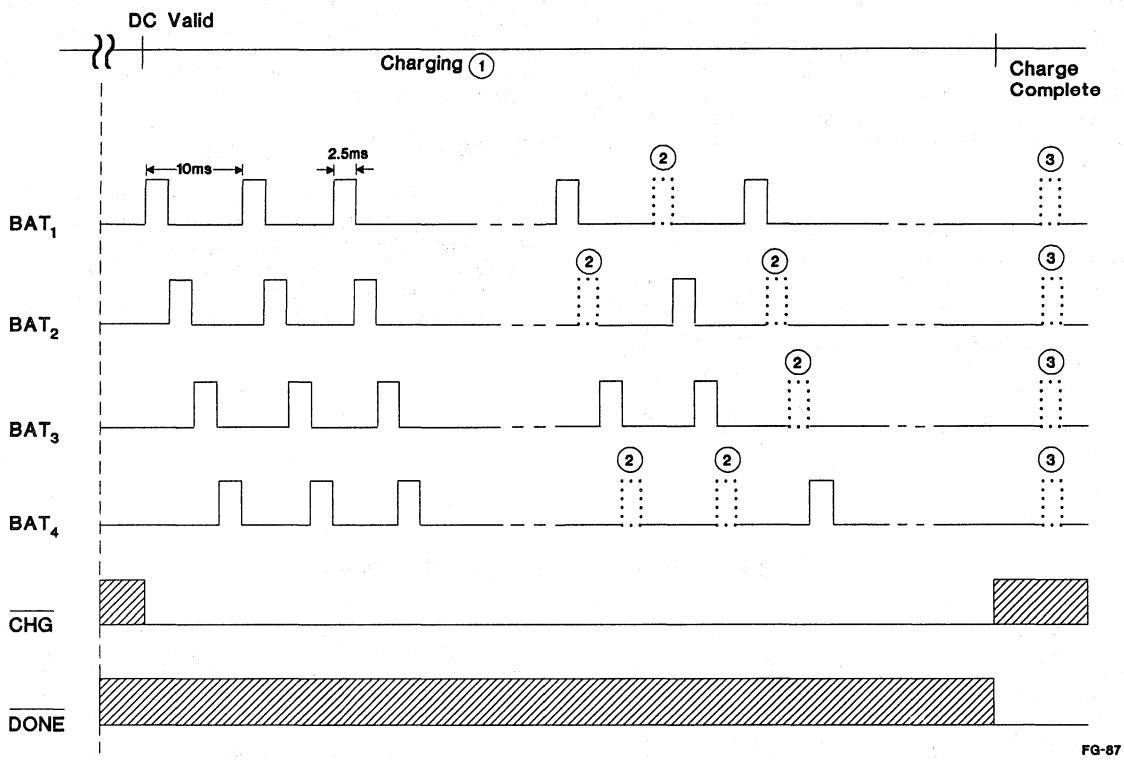
Charge Status Indication

Table 1 outlines the various action states and the associated BAT_{1P}, 1N, 2N, 3N, 4N and $\overline{CHG}$ and $\overline{DONE}$ states. The $\overline{CHG}$ and $\overline{DONE}$ outputs may be connected directly to an LED indicator. In all cases, if the DC voltage at the DC pin is absent, $\overline{CHG}$ and $\overline{DONE}$ outputs are held in a high-impedance condition.

Table 1. bq2901 Operational Summary

Charge Action State	Conditions	$BAT_{1P, 1N, 2N, 3N, 4N}$ Input/Outputs	$\overline{CHG}$ Output	$\overline{DONE}$ Output
DC absent	$V_{DC} = 0$	Low battery detection per V_{SEL}	Z	Z
Charge initiation	DC applied, $V_{OCV} \leq 1.63V$[2]	-	-	-
Charge pending/ fault	$V_{OCV} < 0.4V$ or $V_{CCV} > 3.0V$[3]	-	1/8 sec = Low 1/8 sec = Z	Z
Fast charging	$V_{OCV} \leq$ 1.63V before pulse	Charge pulsed @ 100Hz per Figure 1	Low	Z
Pulse skip	V_{OCV} remains above 1.63 during pulse cycle	Pulse skipped per Figure 1	Low	Z
Charge complete[1]	$V_{OCV} > 1.63V$ for greater than 160ms on all cells	Charge complete	Z	Low

Notes:
1. Charge complete ($\overline{DONE} = 0$) when charge is completed on all three or four batteries.
2. V_{OCV} = Open-circuit voltage of each cell between positive and negative leads.
3. V_{CCV} = Closed-circuit voltage.



Notes:
1. Charging: $0.4 < V_{OCV} \leq 1.63V$, $V_{CCV} \leq 3.0V$.
2. Pulses skipped when $V_{OCV} > 1.63V$.
3. Charge complete when $V_{OCV} \geq 1.63V$ for > 160 ms (16 pulses) for all cells.

Figure 1. bq2901 Application Diagram

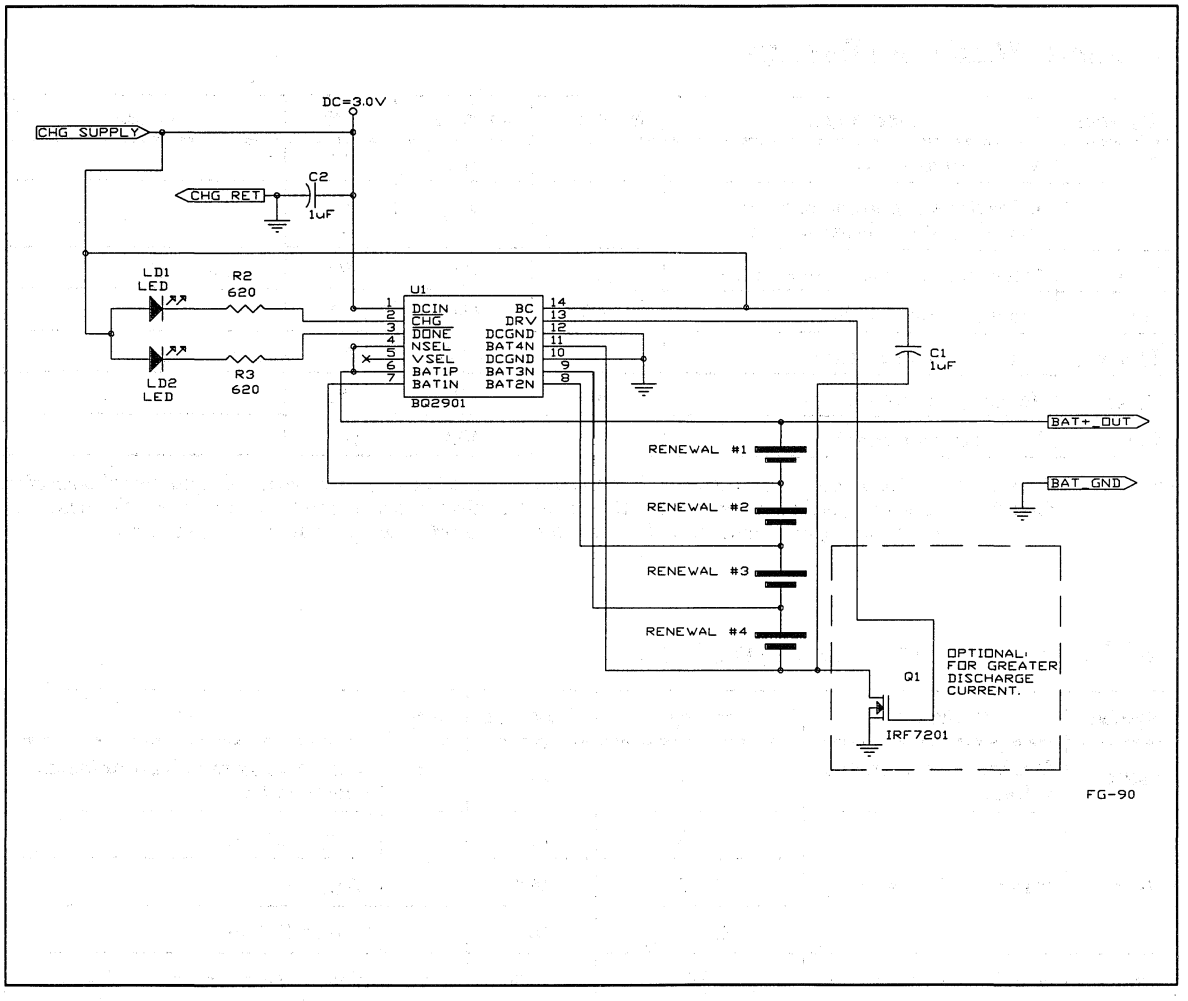


Figure 2. bq2901 Applications Example

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	
I_{DC}	DC charging current	-	400	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{DD} =4.5V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits/terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90V	±5%	V	$V_{SEL} = BAT_{4N}$
		1.0V	±5%	V	$V_{SEL} = Z$
		1.10V	±5%	V	$V_{SEL} = BAT_{1P}$
V_{FLT}	Maximum open-circuit voltage	3V	±3%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{IH}	Logic input high	V_{CC} - 0.5	-	-	V	V_{SEL}, N_{SEL}
V_{IL}	Logic input low	-	-	0.5	V	V_{SEL}, N_{SEL}
V_{OL}	Logic output low	-	-	0.8	V	$\overline{DONE}$, $\overline{CHG}$, DRV, I_{OC} = 10mA
I_{OL}	Output current	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V, $\overline{CHG}$, $\overline{DONE}$
I_{CC}	Supply current	-	-	250	µA	Outputs unloaded, V_{DC} = 3.0V
I_{SB1}	Standby current	-	-	10	µA	V_{DC} = 0, V_{OCV} > V_{EDV}
I_{SB2}	End-of-discharge standby current	-	-	1	µA	V_{DRV} = 0
I_L	Input leakage	-	-	±1	µA	NSEL
I_{OZ}	Output leakage in high-Z state	-5	-	-		$\overline{CHG}$, $\overline{DONE}$
R_{DSON}	On resistance	-	0.5	-	Ω	
I_{IL}	Logic input low	-	-	70	µA	V_{SEL}
I_{IH}	Logic input high	-70	-	-	µA	V_{SEL}
I_{IZ}	Logic input float	-2	-	2	µA	V_{SEL}
V_{OH}	Gate drive output	TBD	-	-	V	DRV
I_{DC}	DC charging current	-	-	300	mA	
V_{DC}	DC charging voltage	-	3.0	-	V	

Note: All voltages relative to GND.

Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_P	Pulse timer	-	100	-	Hz	See Figure 3
t_{PW}	Pulse width	-	2.5	-	ms	See Figure 3

Note: Typical is at $T_A = 25°C$.

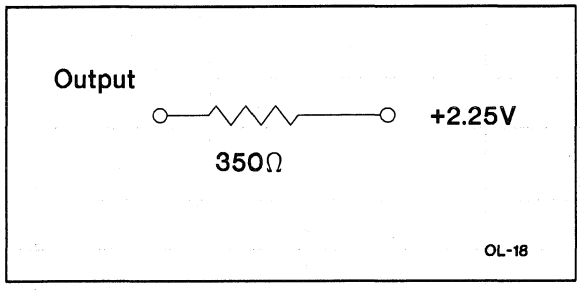


Figure 3. Output Load

Ordering Information

bq2901

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)

Package Option:
PN = 14-pin narrow plastic DIP
SN = 14-pin narrow SOIC

Device:
bq2901 Rechargeable Alkaline Charge IC

BENCHMARQ

bq2201

SRAM Nonvolatile Controller Unit

Features

- Power monitoring and switching for 3 volt battery-backup applications
- Write-protect control
- 3 volt primary cell inputs
- Less than 10 ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2201 SRAM Nonvolatile Controller Unit provides all necessary functions for converting a standard CMOS SRAM into nonvolatile read/write memory.

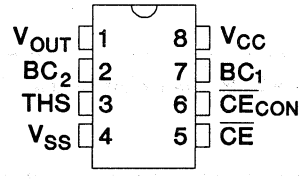
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, a conditioned chip enable output is forced inactive to write-protect any standard CMOS SRAM.

During a power failure, the external SRAM is switched from the V_{CC} supply to one of two 3V backup supplies. On a subsequent power-up, the SRAM is write-protected until a power-valid condition exists.

The bq2201 is footprint- and timing-compatible with industry standards with the added benefit of a chip enable propagation delay of less than 10 ns.

3

Pin Connections



8-Pin Narrow DIP or SOIC

PN-17

Pin Names

V_{OUT}	Supply output
BC_1-BC_2	3 volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON}$	Conditioned chip enable output
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

An external CMOS static RAM can be battery-backed using the Vout and the conditioned chip enable output pin from the bq2201. As V_{CC} slows down during a power failure, the conditioned chip enable output $\overline{CE}_{CON}$ is forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS.

If THS is tied to V_{SS}, power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the $\overline{CE}_{CON}$ output is unconditionally driven high, write-protecting the memory.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to one of the two external backup energy sources. $\overline{CE}_{CON}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the V_{CC} supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. The $\overline{CE}_{CON}$ output is held inactive for time t_{CER} (120 ms maximum) after the supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is fed through to the $\overline{CE}_{CON}$ output with a propagation delay of less than 10 ns. Nonvolatility is achieved by hardware hookup as shown in Figure 1.

Energy Cell Inputs—BC_1, BC_2

Two primary backup energy source inputs are provided on the bq2201. The BC_1 and BC_2 inputs accept a 3V primary battery, typically some type of lithium chemistry. If no primary cell is to be used on either BC_1 or BC_2, the unused input should be tied to Vss.

If both inputs are used, during power failure the V_{OUT} output is fed only by BC_1 as long as it is greater than 2.5V. If the voltage at BC_1 falls below 2.5V, an internal isolation switch automatically switches V_{OUT} from BC_1 to BC_2.

To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{CON}$ are internally isolated from BC_1 and BC_2 by either:

- Initial connection of a battery to BC_1 or BC_2, or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to the point of (0.48 to 0.52)*V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The appropriate battery is connected to V_{OUT} and $\overline{CE}_{CON}$ immediately on subsequent application and removal of V_{CC}.

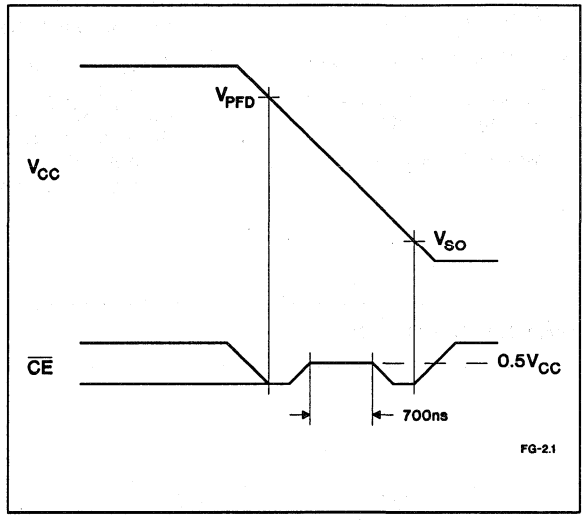


Figure 2. Battery Isolation Signal

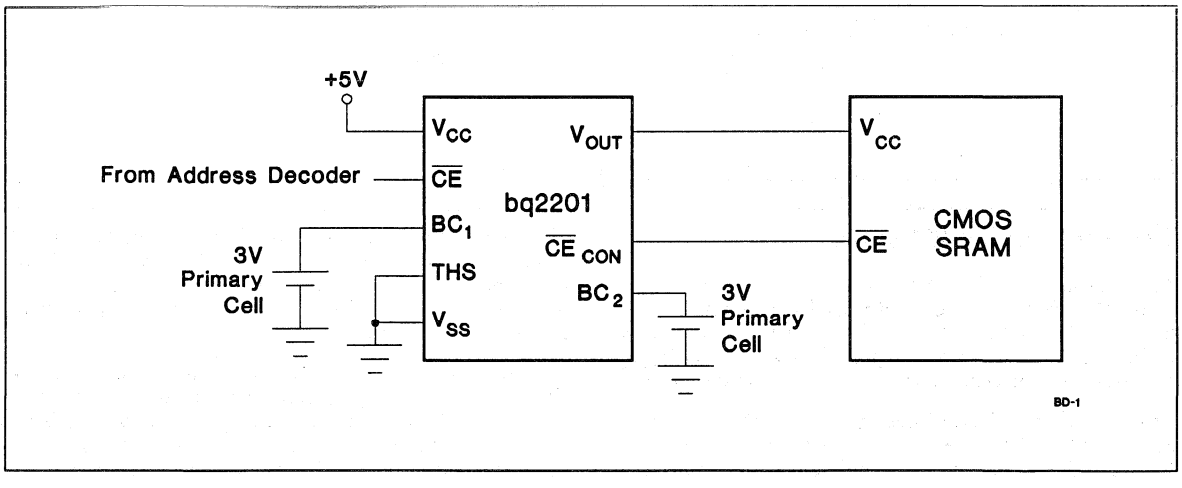


Figure 1. Hardware Hookup (5% Supply Operation)

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to 125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC1}, V_{BC2}	Backup cell voltage	2.0	-	4.0	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	3	5	mA	No load on V_{OUT} and $\overline{CE}_{CON}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	V_{OUT} data-retention current to additional memory not included.
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage	-	V_{BC2}	-	V	V_{BC1} < 2.5V
		-	V_{BC1}	-	V	V_{BC1} > 2.5V
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} > V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} > V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

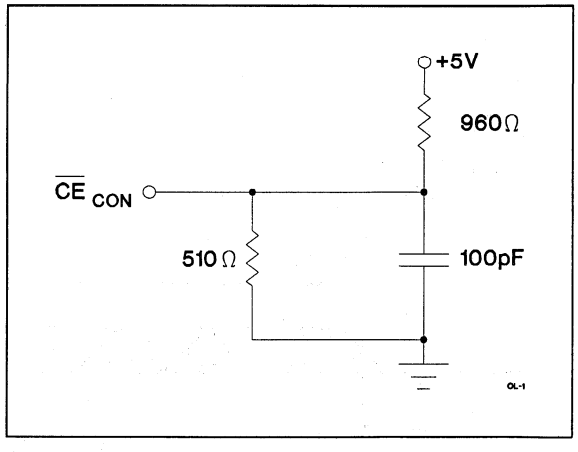


Figure 3. Output Load

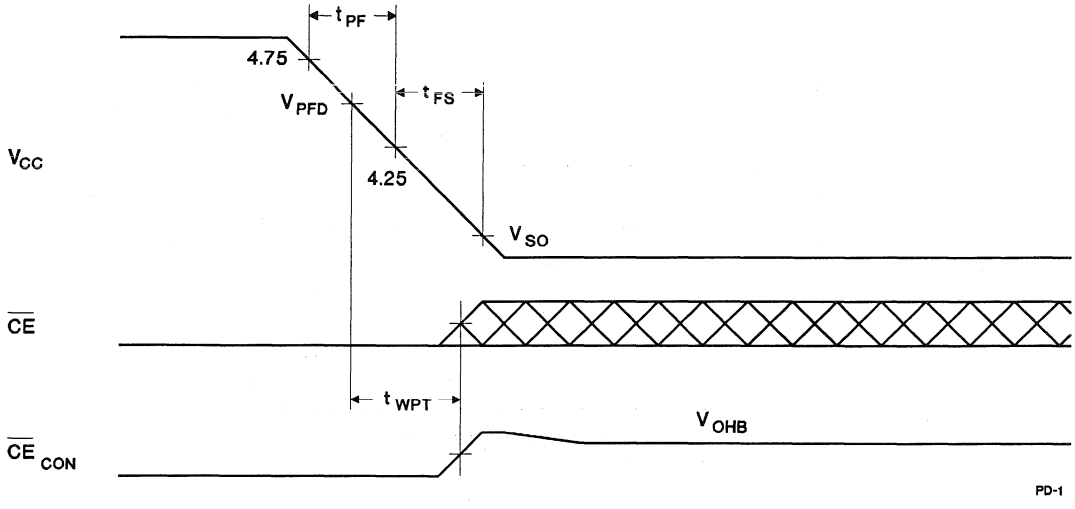
Power-Fail Control ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PF}	V_{CC} slew, 4.75V to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, 4.25V to 4.75V	0	-	-	µs	
t_{CED}	Chip enable propagation delay	-	7	10	ns	
t_{CER}	Chip enable recovery	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

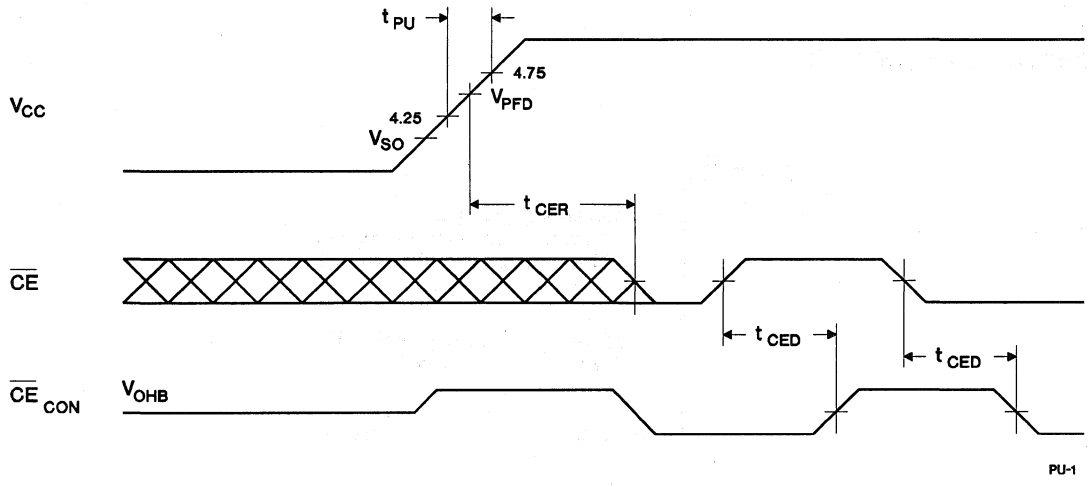
Note: Typical values indicate operation at T_A = 25°C.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down Timing



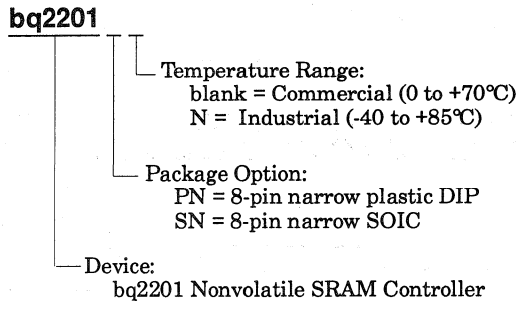
Power-Up Timing



Data Sheet Revision History (Sept. 1991 Changes From Sept. 1990)

Added industrial temperature range.

Ordering Information



BENCHMARQ

bq2202

SRAM NV Controller With Reset

Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Input decoder allows control of up to 2 banks of SRAM
- 3V primary cell input
- 3V rechargeable battery input/output
- Reset output for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2202 SRAM Nonvolatile Controller With Reset provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

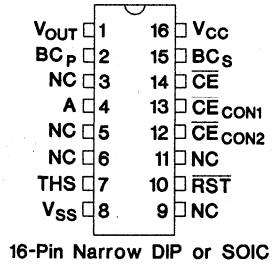
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the backup supply to the V_{CC} supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

3

Pin Connections



16-Pin Narrow DIP or SOIC

PN-22

Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank select input
BC_P	3V backup supply input
BC_S	3V rechargeable backup supply input/output
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip enable output pins from the bq2202. As the voltage input V_{CC} slows down during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µsec maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within t_{PFD} (150 µsec maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

Energy Cell Inputs—BC_P, BC_S

Two backup energy source inputs are provided on the bq2202—a primary cell BC_P and a secondary cell BC_S. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If a primary cell is not to be used, the BC_P pin should be grounded. The secondary cell input BC_S is designed to accept constant-voltage current-limited rechargeable cells.

During normal +5V power valid operation, 3.3V is output on the BC_S pin and is current-limited internally.

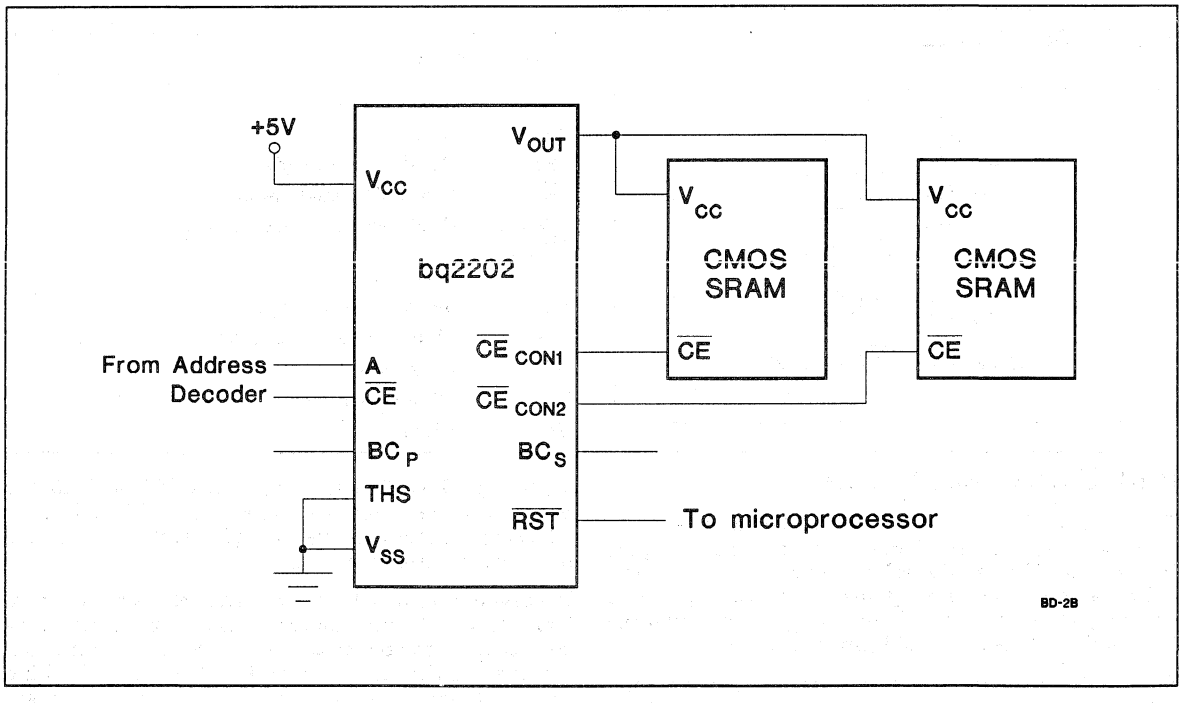


Figure 1. Hardware Hookup (5% Supply Operation)

If a secondary cell is not to be used, the BC_S pin must be tied directly to V_{SS}. If both inputs are used, during power failure the V_{OUT} and $\overline{CE}_{CON}$ outputs are forced high by the secondary cell so long as it is greater than 2.5V. Only the secondary cell is loaded by the data retention current of the SRAM until the voltage at the BC_S pin falls below 2.5V. When and if the voltage at BC_S falls below 2.5V, an internal isolation switch automatically transfers the load from the secondary cell to the primary cell.

To prevent battery drain when there is no valid data to retain, V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from BC_P and BC_S by either:

- Initial connection of a battery to BC_P or BC_S or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to V_{CC}*(0.48 to 0.52) and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds V_{CC}*0.54 at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The battery is connected to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ immediately on subsequent application and removal of V_{CC}.

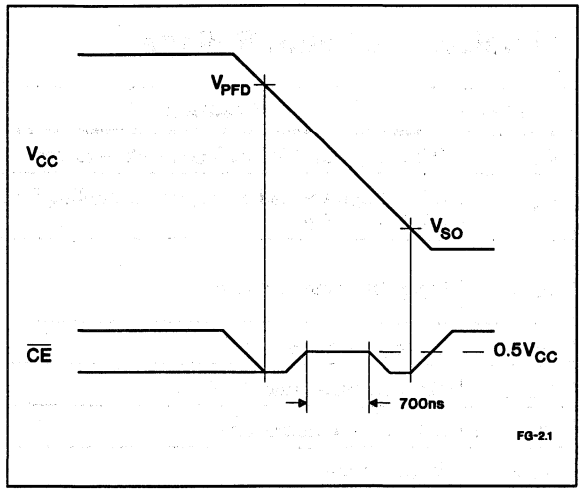


Figure 2. Battery Isolation Signal

3

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to 85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{BCP}	Backup cell input voltage	2.0	-	4.0	V	$V_{CC} < V_{BC}$
V_{BCS}		2.5	-	4.0		
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, backup supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	3	6	mA	No load on V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	No load on V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.2	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage	-	V_{BCS}	-	V	$V_{BCS} > 2.5V$
		-	V_{BCP}	-	V	$V_{BCS} < 2.5V$
R_{BCS}	BCs charge output internal resistance	500	1000	1750	Ω	$V_{BCSO} \geq 3.0V$
V_{BCSO}	BCs charge output voltage	3.0	3.3	3.6	V	$V_{CC} > V_{PFD}$, $\overline{RST}$ inactive, full charge or no load
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} \geq V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} \geq V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

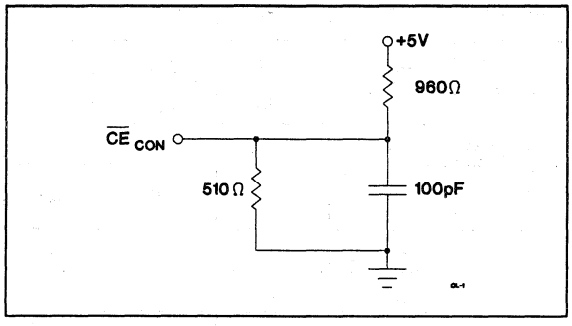


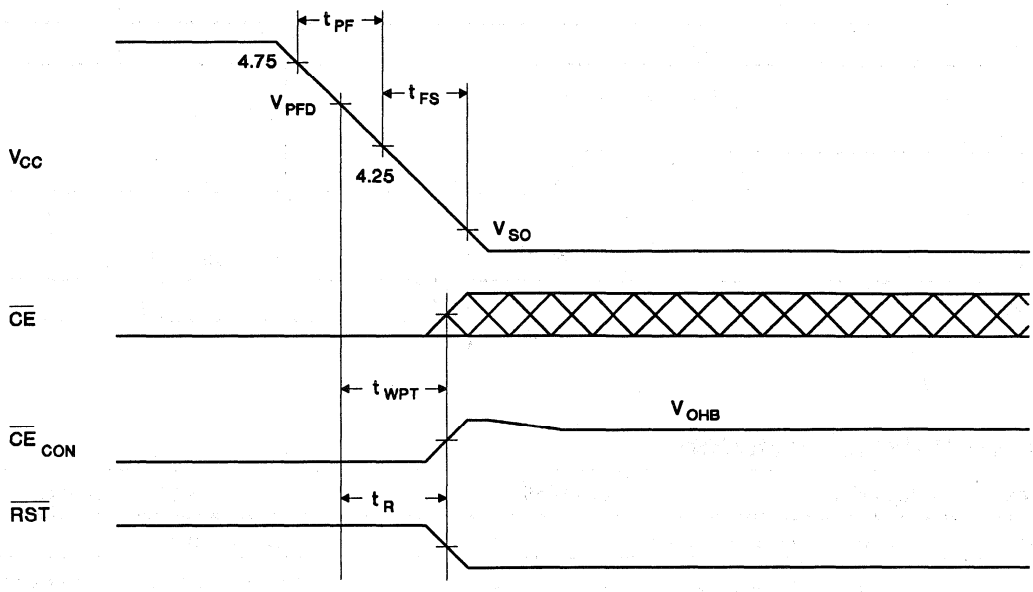
Figure 3. Output Load

Power-Fail Control ($T_A = T_{OPR}$)

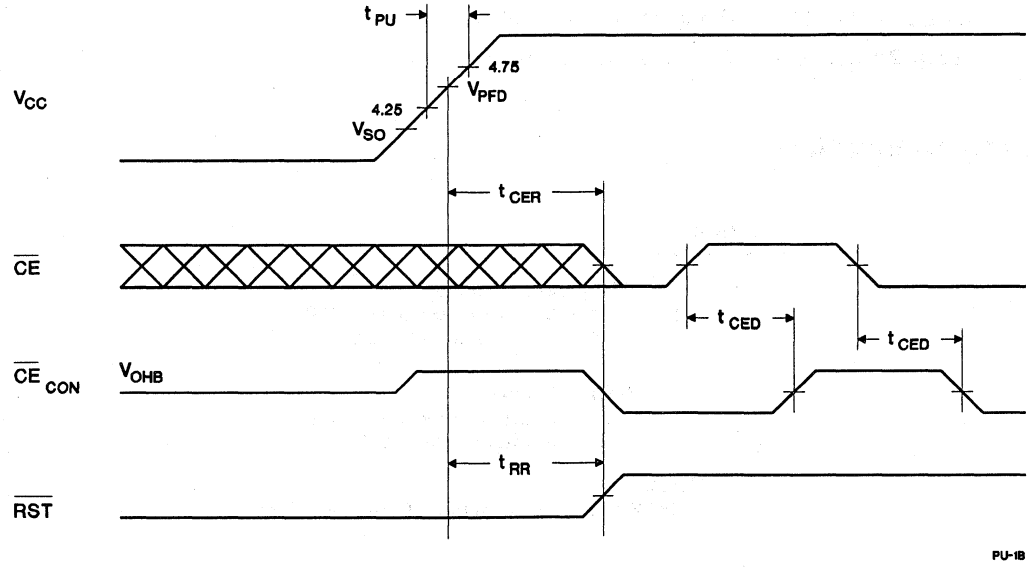
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75 V	0	-	-	µs	
t_{CED}	Chip-enable propagation delay	-	7	10	ns	
t_{CER}	Chip-enable recovery time	t_{RR}	-	t_{RR}	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	40	80	120	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0	-	-	ns	
t_{WPT}	Write-protect time	t_R	-	t_R	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

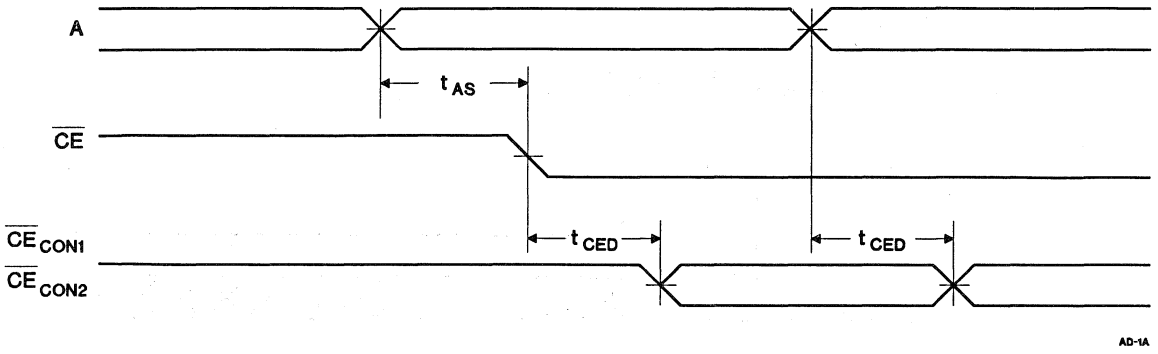
Power-Down Timing



Power-Up Timing



Address-Decode Timing



Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3-10	Deleted last sentence	Clarification
1	3-13	V_{BCSO}—BCs charge output voltage	Was 3.15 min, 3.3 typ, 3.45 max; is 3.0 min, 3.3 typ, 3.6 max
2	3-13	Maximum charge output internal resistance (R_{BCS}) changed to 1750Ω	Was 1500Ω

Note: Change 1 = Dec. 1992 B changes from Sept. 1991 A.

Change 2 = Nov. 1994 C changes from Dec. 1992 B.

Ordering Information

bq2202

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)

Package Option:
PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2202 SRAM Nonvolatile Controller With Reset

BENCHMARQ

bq2203A

NV Controller With Battery Monitor

Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Battery-low and battery-fail indicators
- Reset output for system power-on reset
- Input decoder allows control of up to 2 banks of SRAM
- 3V primary cell input
- 3V rechargeable battery input/output

General Description

The CMOS bq2203A SRAM Nonvolatile Controller With Battery Monitor provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory. The bq2203A is compatible with the Personal Computer Memory Card International Association (PCMCIA) recommendations for battery-backed static RAM memory cards.

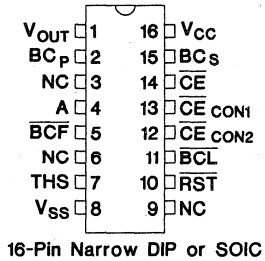
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the backup supply to the V_{CC} supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system. The battery monitor indicates battery-low and battery-fail conditions.

During power-valid operation, the input decoder selects one of two banks of SRAM.

3

Pin Connections



16-Pin Narrow DIP or SOIC

PN-26

Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank select input
$\overline{BCF}$	Battery fail push-pull output
$\overline{BCL}$	Battery low push-pull output
BC_P	3V backup supply input
BC_S	3V rechargeable backup supply input/output
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and the conditioned chip enable output pins from the bq2203A. As the voltage input V_{CC} slows down during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{CC}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µs maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within t_{PFD} (150µs maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

Energy Cell Inputs—BC_P, BC_S

Two backup energy source inputs are provided on the bq2203A—a primary cell BC_P and a secondary cell BC_S. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If a primary cell is not to be used, the BC_P pin should be tied to V_{SS}. The secondary cell input BC_S is designed to accept constant-voltage current-limited rechargeable cells.

During normal +5V power valid operation, 3.3V typical is output on the BC_S pin and is current-limited internally. Although this charging method can be used with various 3V secondary cells, it is specifically designed for a Panasonic VL (vanadium-lithium) series of rechargeable cells.

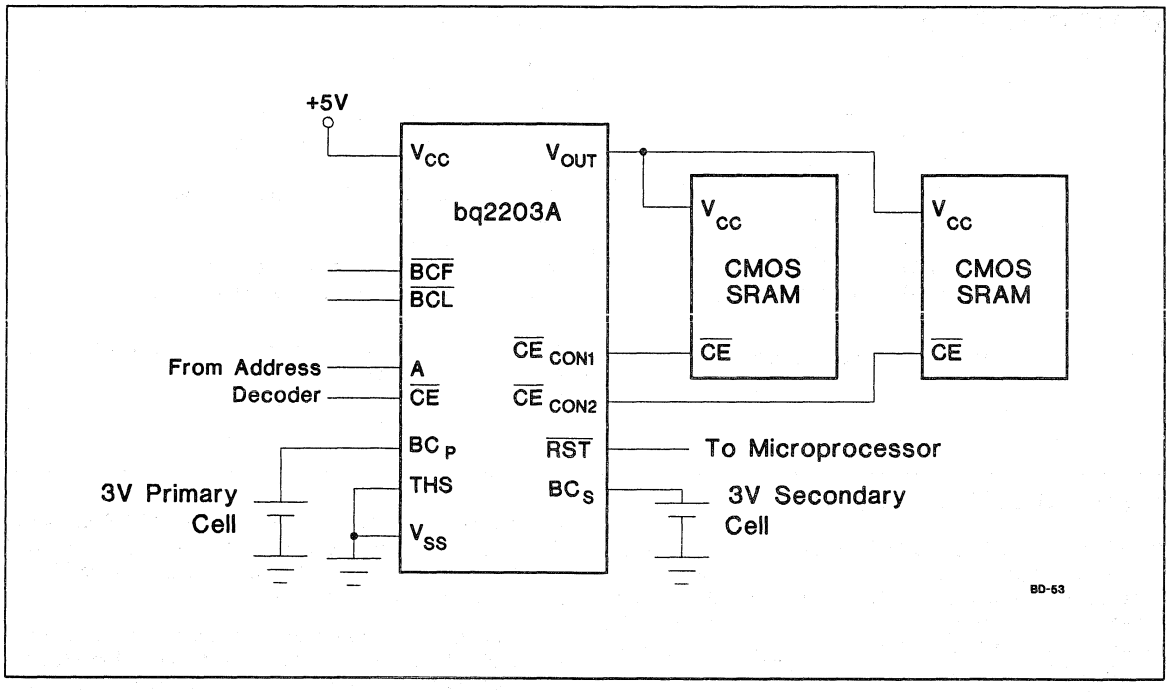


Figure 1. Hardware Hookup (5% Supply Operation)

If a secondary cell is not to be used, the BC_S pin must be tied directly to V_{SS}.

V_{CC} falling below V_{PFD} starts the comparison of BC_S and BC_P. The BC input comparison continues until V_{CC} rises above V_{SO}. Power to V_{OUT} begins with BC_S and switches to BC_P only when BC_S is less than BC_P minus V_{BSO}. The controller alternates to the higher BC voltage when the difference between the BC input voltages is greater than V_{BSO}. Alternating the backup batteries allows one-at-a-time battery replacement and efficient use of both backup batteries.

To prevent battery drain when there is no valid data to retain, V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from BC_P and BC_S by either:

- Initial connection of a battery to BC_P or BC_S (V_{CC} grounded) or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to V_{CC}*(0.48 to 0.52) and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds V_{CC}*0.54 at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The isolation function is terminated and the appropriate battery is connected to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ by powering V_{CC} up through V_{PFD}.

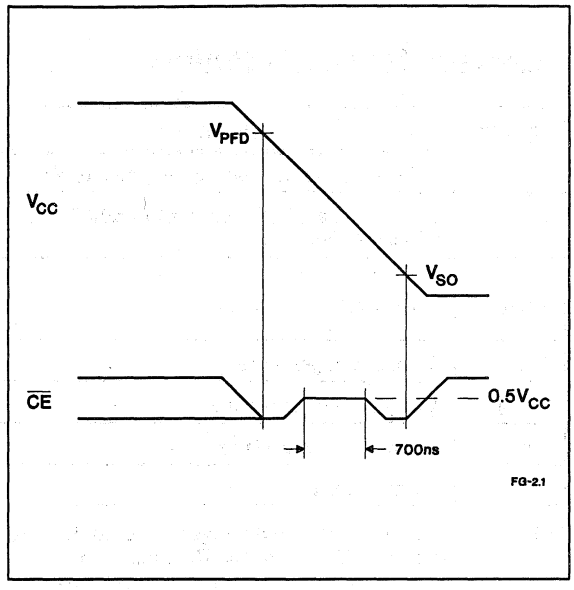


Figure 2. Battery Isolation Signal

Battery Monitor—$\overline{BCL}$, $\overline{BCF}$

As V_{CC} rises past V_{PFD}, the battery voltage on BC_P is compared with a dual voltage reference. The result of this comparison is latched internally, and output after t_{BC} when V_{CC} rises past V_{PFD}. If the battery voltage on BC_P is below V_{BL}, then $\overline{BCL}$ is asserted low. If the battery is below V_{BF}, then $\overline{BCL}$ and $\overline{BCF}$ are asserted low. The results of this comparison remain latched until V_{CC} falls below V_{PFD}.

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	Commercial
		-40 to +85	°C	"N" Industrial
T_{STG}	Storage temperature	-55 to 125	°C	
T_{BIAS}	Temperature under bias	-40 to 85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{CC}
V_{BCP}	Backup cell input voltage	2.0	-	4.0	V	$V_{CC} < V_{BC}$
V_{BCS}		2.0	-	4.0	V	$V_{CC} < V_{BC}$
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	$V_{CC} + 0.3$	V	
THS	Threshold select	-0.3	-	$V_{CC} + 0.3$	V	

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, backup supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	3	6	mA	No load on outputs
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{CC}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	No load on outputs
V_{BC}	Active backup cell voltage	-	V_{BCS}	-	V	$V_{BCS} > V_{BCP} + V_{BSO}$
		-	V_{BCP}	-	V	$V_{BCP} > V_{BCS} + V_{BSO}$
V_{BSO}	Battery switch-over voltage	0.25	0.4	0.6	V	
R_{BCS}	BC_S charge output internal resistance	500	1000	1750	Ω	$V_{BCSO} \geq 3.0V$
V_{BCSO}	BC_S charge output voltage	3.15	3.3	3.5	V	$V_{CC} > V_{PFD}$, $\overline{RST}$ inactive, full charge or no load
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} \geq V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} \geq V_{BC}$ - 0.2V
V_{BL}	Voltage battery low	2.3	-	2.5	V	BC_P input only
V_{BF}	Voltage battery fail	2.0	-	2.2	V	BC_P input only

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

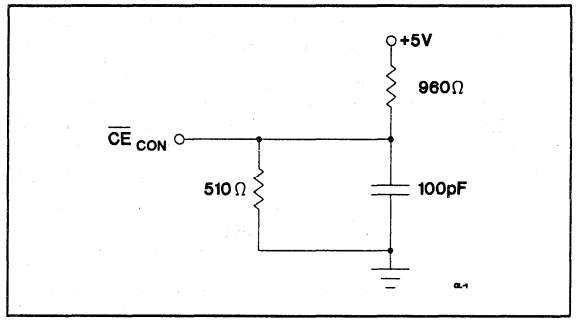


Figure 3. Output Load

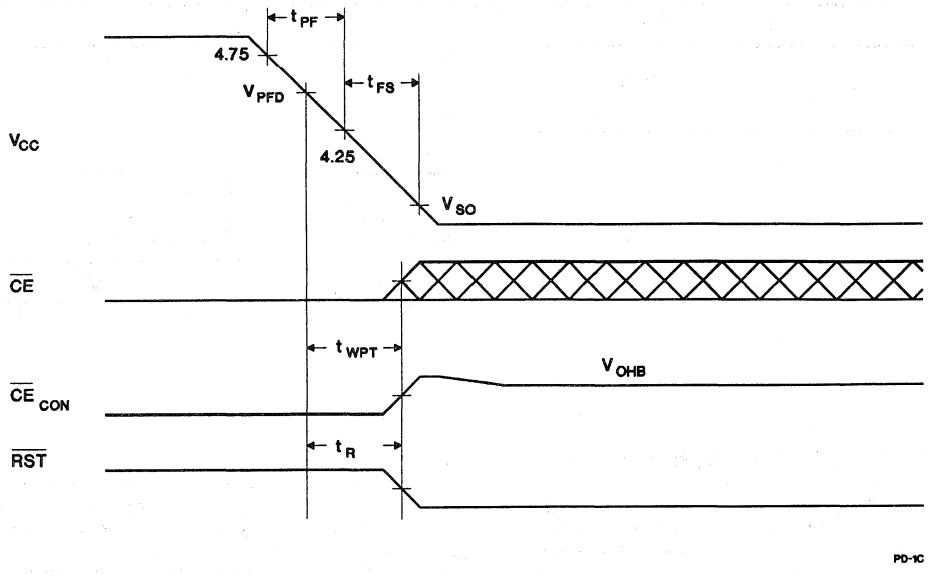
Power-Fail Control (T_A = T_{OPR})

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75 V	0	-	-	µs	
t_{CED}	Chip-enable propagation delay		7	10	ns	
t_{CER}	Chip-enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	t_{CER}	-	t_{CER}	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0	-	-	ns	
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	t_{WPT}	-	t_{WPT}	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active
t_{BC}	V_{PFD} to $\overline{BCL}$/$\overline{BCF}$ active	t_{CER}	-	t_{CER}	ms	Delay after V_{CC} slews up past V_{PFD} before $\overline{BCL}$ or $\overline{BCF}$ is active

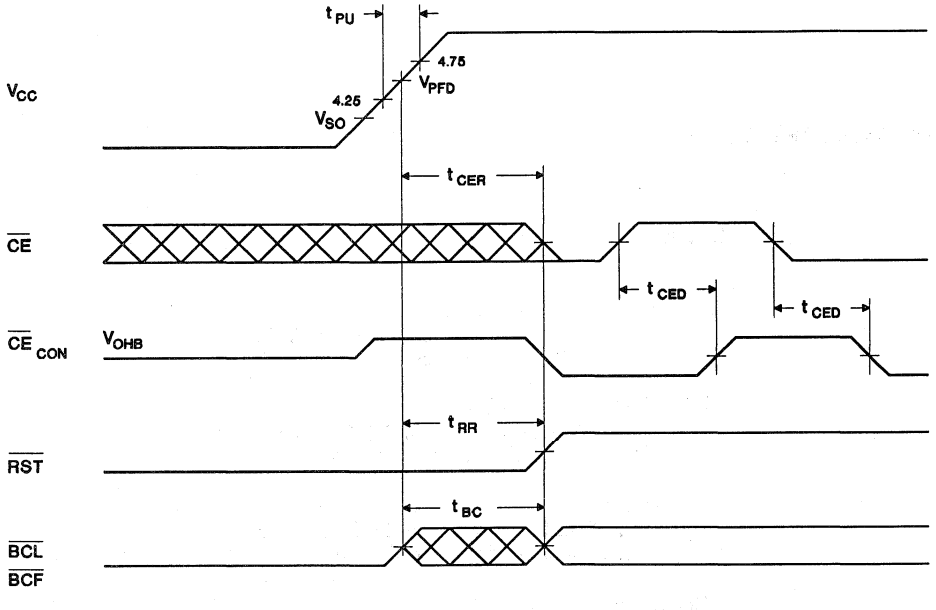
Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

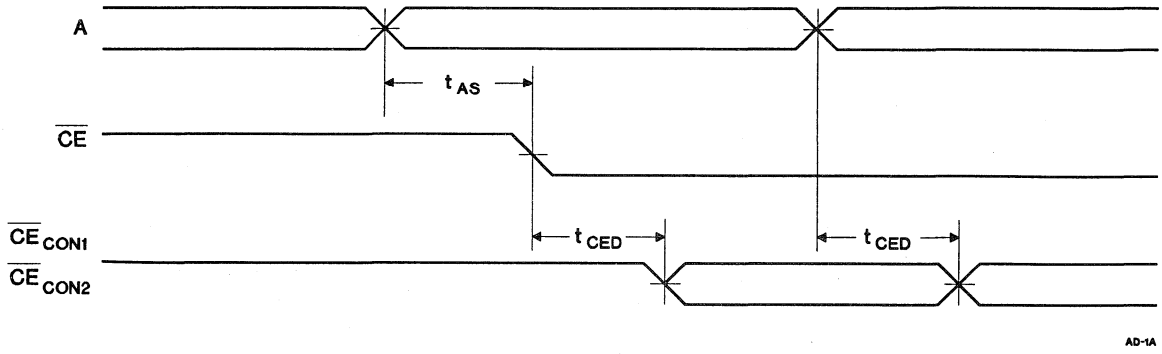
Power-Down Timing



Power-Up Timing



Address-Decode Timing



Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	-	Data sheet changed from "Preliminary" to "Final"	
1	3-21	Maximum charge output internal resistance (R_{BCS}) changed to 1750Ω	Was 1500Ω

Note: Change 1 = Nov. 1994 B changes from Dec. 1992.

Ordering Information

bq2203A _ _

- Temperature Range:
  - blank = Commercial (0 to +70°C)
  - N = Industrial (-10 to +85°C)*
- Package Option:
  - PN = 16-pin plastic DIP Narrow
  - SN = 16-pin SOIC Narrow
- Device:
  - bq2203A SRAM Nonvolatile Controller With Battery Monitor and Reset

*Contact factory for availability.

BENCHMARQ

bq2204A

X4 SRAM Nonvolatile Controller Unit

Features

- Power monitoring and switching for 3 volt battery-backup applications
- Write-protect control
- 2-input decoder allows control for up to 4 banks of SRAM
- 3 volt primary cell inputs
- Less than 10 ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2204A SRAM Nonvolatile Controller Unit provides all necessary functions for converting up to four banks of standard CMOS SRAM into nonvolatile read/write memory.

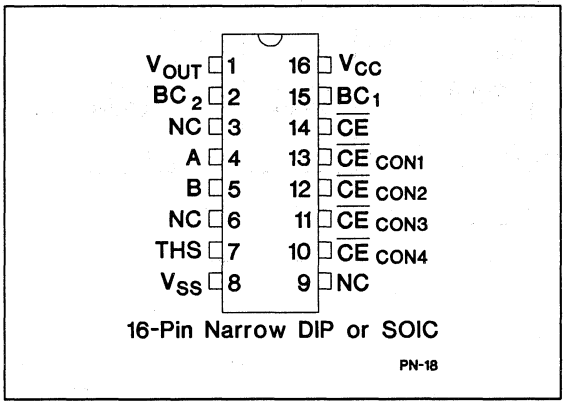
A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the four conditioned chip enable outputs are forced inactive to write-protect up to four banks of SRAM.

During a power failure, the external SRAMs are switched from the V_{CC} supply to one of two 3V backup supplies. On a subsequent power-up, the SRAMs are write-protected until a power-valid condition exists.

During power-valid operation, a two-input decoder transparently selects one of up to four banks of SRAM.

3

Pin Connections



16-Pin Narrow DIP or SOIC

PN-18

Pin Names

V_{OUT}	Supply output
BC_1-BC_2	3 volt primary backup cell inputs
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$-$\overline{CE}_{CON4}$	Conditioned chip enable outputs
A-B	Decoder inputs
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Up to four banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip enable output pins from the bq2204A. As V_{CC} slows down during a power failure, the conditioned chip enable outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection at 4.62V typical for 5% supply operation. If THS is tied to V_{CC}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process to any of the four external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, all four chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to one of the two external backup energy sources. $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ through $\overline{CE}_{CON4}$ are held inactive for time t_{CER} (120 ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the four $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input is output on one of the four $\overline{CE}_{CON}$ output pins depending on the level of the decode inputs at A and B as shown in the Truth Table.

The A and B inputs are usually tied to high-order address pins so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

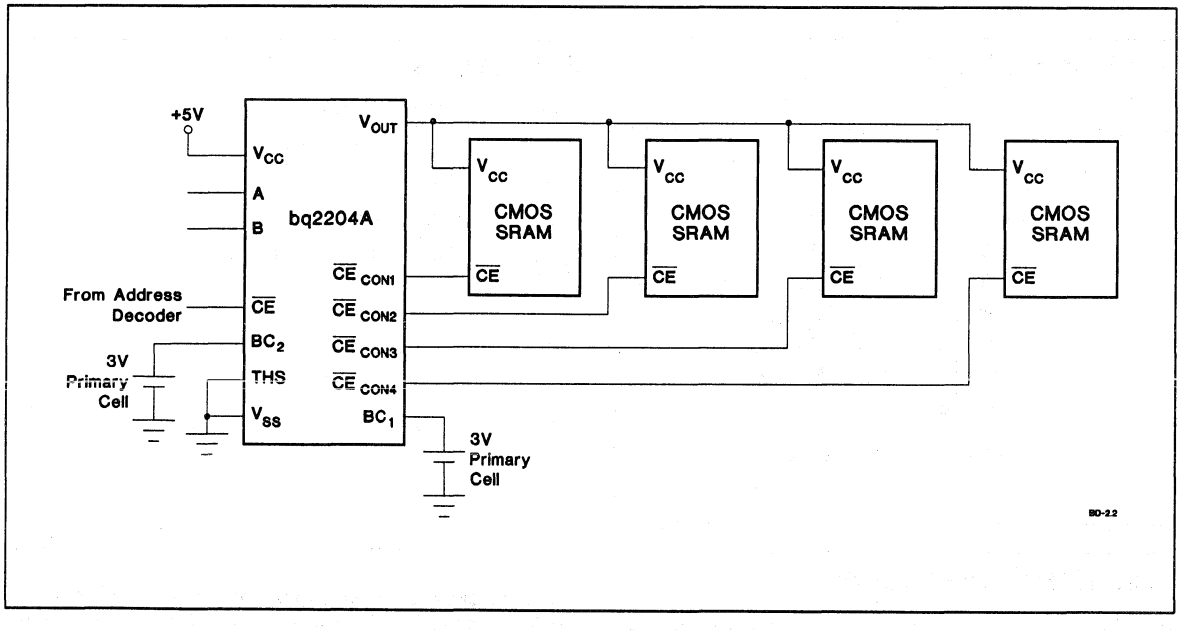


Figure 1. Hardware Hookup (5% Supply Operation)

Energy Cell Inputs—BC_1, BC_2

Two backup energy source inputs are provided on the bq2204A. The BC_1 and BC_2 inputs accept a 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If no primary cell is to be used on either BC_1 or BC_2, the unused input should be tied to Vss.

V_{CC} falling below V_{PFD} starts the comparison of BC_1 and BC_2. The BC input comparison continues until V_{CC} rises above V_{SO}. Power to V_{OUT} begins with BC_1 and switches to BC_2 only when V_{BC1} is less than V_{BC2} minus V_{BSO}. The controller only alternates to the higher BC voltage when the difference between the BC input voltages is greater than V_{BSO}. Alternating the backup batteries allows one-at-a-time battery replacement and efficient use of both backup batteries.

To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{CON1-4}$ are internally isolated from BC_1 and BC_2 by either:

- Initial connection of a battery to BC_1 or BC_2, or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to the point of (0.48 to 0.52)*V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The appropriate battery is connected to V_{OUT} and $\overline{CE}_{CON1-4}$ immediately on subsequent application and removal of V_{CC}.

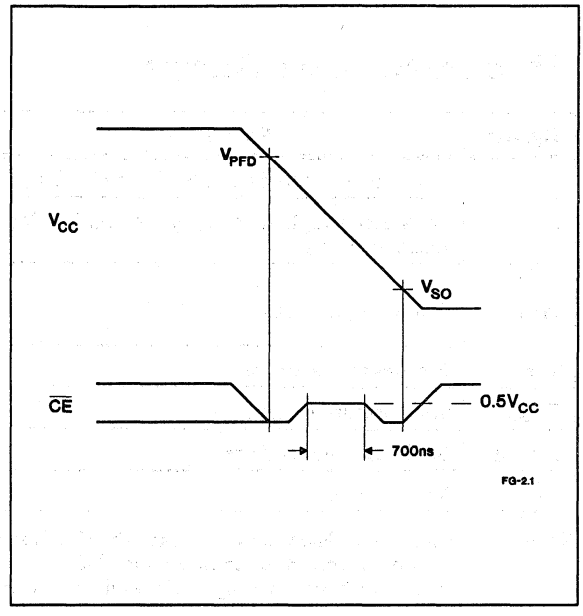


Figure 2. Battery Isolation Signal

Truth Table

Inputs			Outputs			
$\overline{CE}$	A	B	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$	$\overline{CE}_{CON3}$	$\overline{CE}_{CON4}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{CC}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC1}, V_{BC2}	Backup cell voltage	2.0	-	4.0	V	$V_{CC} < V_{BC}$
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	3	6	mA	No load on outputs.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{CC}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	V_{OUT} data-retention current to additional memory not included.
V_{BC}	Active backup cell voltage	-	V_{BC1}	-	V	$V_{BC1} > V_{BC2} + V_{BSO}$
		-	V_{BC2}	-	V	$V_{BC2} > V_{BC1} + V_{BSO}$
V_{BSO}	Battery switch-over voltage	0.25	0.4	0.6	V	
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} > V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} > V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

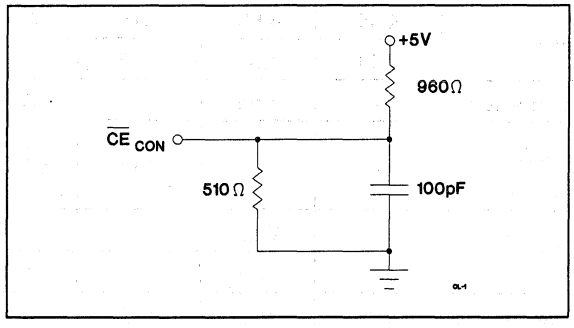


Figure 3. Output Load

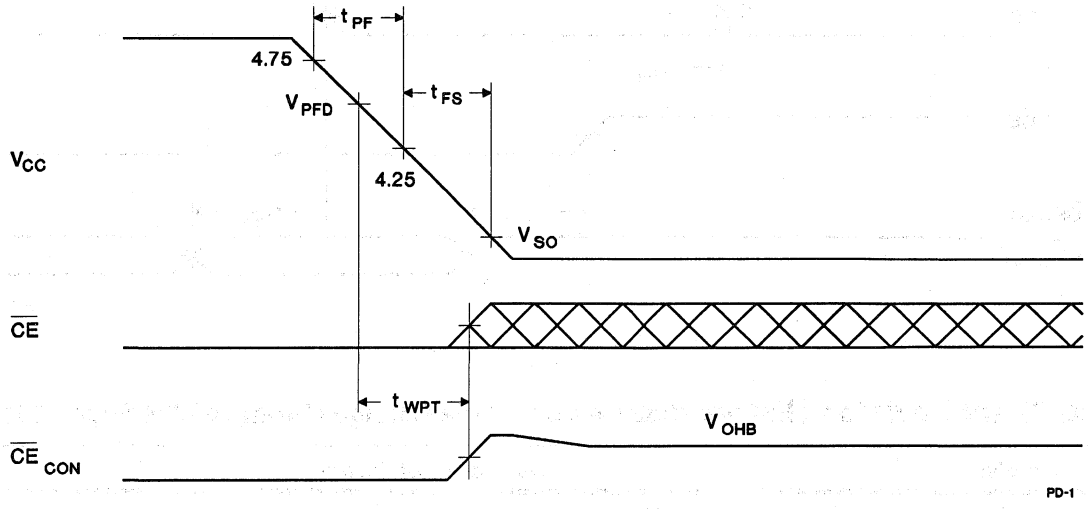
Power-Fail Control ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PF}	V_{CC} slew, 4.75V to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, 4.25V to 4.75V	0	-	-	µs	
t_{CED}	Chip enable propagation delay	-	7	10	ns	
t_{AS}	A,B set up to $\overline{CE}$	0	-	-	ns	
t_{CER}	Chip enable recovery	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

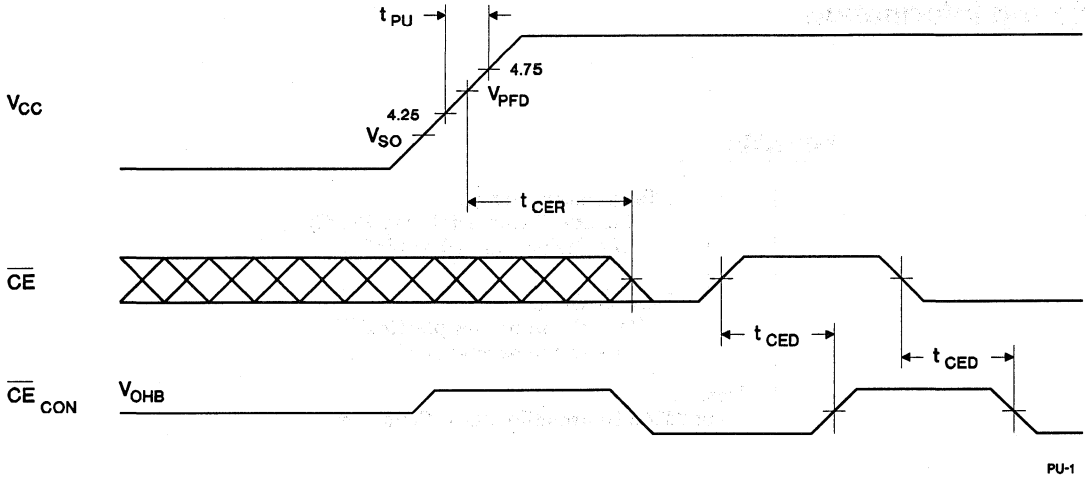
Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

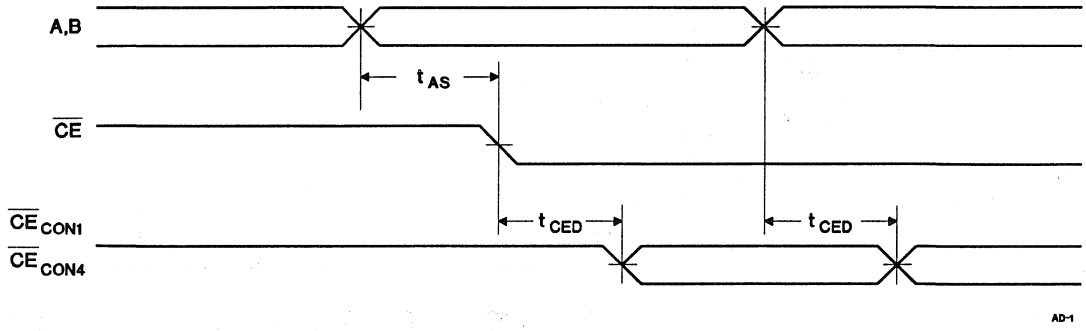
Power-Down Timing



Power-Up Timing



Address-Decode Timing



Data Sheet Revision History (bq2204A Dec. 1992 Changes From bq2204 Sept. 1991)

Page No.	Description of Change
All	bq2204A replaces bq2204.
3-25, 3-28, 3-29	10% tolerance requires the THS pin to be tied to V_{CC}, not V_{OUT}.
3-27	Energy cell input selection process alternates between BC_1 and BC_2.

Ordering Information

bq2204A _ _

- Temperature Range:
  - blank = Commercial (0 to +70°C)
  - N = Industrial (-40 to +85°C)
- Package Option:
  - PN = 16-pin narrow plastic DIP
  - SN = 16-pin narrow SOIC
- Device:
  - bq2204A Nonvolatile SRAM Controller

BENCHMARQ

bq2212

X2 PSRAM Nonvolatile Controller

Features

- Power monitoring and switching for battery-backup of pseudo-static RAMs
- Complete nonvolatile and refresh control of pseudo-static RAMs
- Power-fail write-protection
- Controls up to 2 banks of PSRAM
- Nonrechargeable and rechargeable backup battery inputs
- Battery isolation pin for long storage periods
- Reset output for processor power-on reset
- Battery-fail flag indicates a low battery voltage condition
- 3V rechargeable battery input/output

General Description

The CMOS bq2212 PSRAM Nonvolatile Controller provides all necessary functions for converting up to two banks of standard 3V CMOS pseudo-static RAM into nonvolatile read/write memory.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When an out-of-tolerance condition is detected, the two conditioned chip enable outputs are forced inactive to write-protect the two banks of PSRAM.

When an out-of-tolerance condition is detected and V_{CC} falls below the battery voltage, the external energy source is switched on to sustain the memory until V_{CC} returns valid. After V_{CC} returns valid, the eight start-up cycles required by the PSRAMs are handled automatically during the chip enable recovery time.

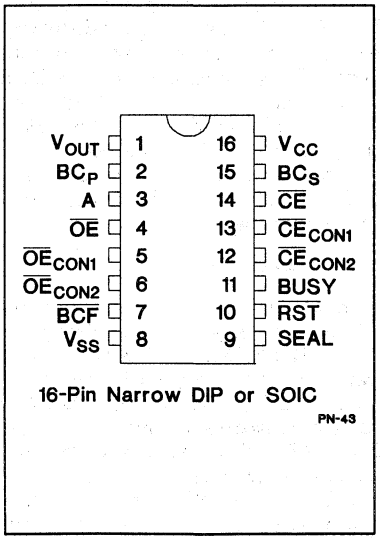
An internal voltage regulator steps down V_{OUT} voltage to approximately 3.0V. The regulator is bypassed when battery power is being used.

Because a read/write access might be requested during an internal refresh interval, a BUSY pin is provided to indicate when the selected device is busy with an internal refresh.

The controller handles all PSRAM refresh functions. During power-valid operation, the controller refreshes the PSRAMs using automatic refresh cycles. During power-fail operation, the PSRAMs are placed in self-refresh mode.

3

Pin Connections



16-Pin Narrow DIP or SOIC

PN-43

Pin Names

V_{OUT}	Regulated supply output	SEAL	Battery isolation signal
BC_P	Nonrechargeable backup supply input	$\overline{RST}$	Reset output
BC_S	Rechargeable backup supply input/output	BUSY	Read/write cycle acknowledge open-drain output
$\overline{BCF}$	Battery fail output	$\overline{CE}_{CON1}$-$\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank-select input	$\overline{CE}$	Chip enable active low input
$\overline{OE}$	Output enable input	V_{CC}	+5 volt supply input
$\overline{OE}_{CON1}$-$\overline{OE}_{CON2}$	Conditioned output enable outputs	V_{SS}	Ground

Pin Descriptions

V_{OUT} **Supply output**

V_{OUT} supplies power to the external PSRAMs from one of several sources. If V_{CC} is above V_{BCS} (valid V_{CC}), then internally regulated power, derived from V_{CC}, is applied to V_{OUT}. The regulated power voltage is at 3.0V (±10%). If V_{CC} falls below V_{BCS}, then the rechargeable battery BC_S is applied to V_{OUT}. If the rechargeable battery voltage falls below about 2.5V, then V_{OUT} is supplied from the nonrechargeable battery BC_P. As V_{CC} returns valid, V_{OUT} is switched from the backup supply back to the V_{CC} supply. Hysteresis is built in around the switch-over voltages to prevent excessive bouncing between different power sources. If there is no need to retain data after V_{CC} is removed, V_{OUT} can be isolated from both backup inputs by using the SEAL input.

BC_P **Nonrechargeable backup supply input**

The BC_P input is an external energy source connection that is not rechargeable. This backup can be a battery or a board-level backup system. The voltage input on this pin should be between 2.5V and 3.4V. This backup is used during a power-fail condition and when the backup system connected to BC_S is below about 2.5V. This input should be tied to V_{SS} if no battery is used.

BC_S **Rechargeable backup supply input/output**

The BC_S input is to be used with 3V rechargeable vanadium-lithium batteries such as Panasonic's VL1220. This input supplies V_{OUT} if V_{CC} falls below the BC_S voltage. During valid V_{CC} operation, this pin sources a current-limited 3.3V to keep the batteries charged and ready for use. If no rechargeable battery is used, then this input should be tied to V_{SS}.

$\overline{BCF}$ **Battery fail output**

If V_{CC} and BC_P are below their minimum valid voltage levels on power-up, the $\overline{BCF}$ output goes low and stays low on subsequent valid V_{CC} to alert the user that data inside the PSRAMs may be corrupted.

A **Bank select address input**

Two banks of PSRAMs can be controlled by the bq2212, and these banks are selected by the "A" address input. For "A" low, $\overline{CE}_{CON1}$ and $\overline{OE}_{CON1}$ are activated. For "A" high, $\overline{CE}_{CON2}$ and $\overline{OE}_{CON2}$ are activated. Address setup time is measured to $\overline{CE}$, but address hold time is measured starting when BUSY goes low.

$\overline{OE}$ **Output enable input**

During an active cycle, the $\overline{OE}$ input is passed directly onto $\overline{OE}_{CON1}$ or $\overline{OE}_{CON2}$, depending on the state of address "A," but is inhibited during $\overline{CE}$ inactive. $\overline{OE}$ is an active low input.

$\overline{OE}_{CON1}$/ $\overline{OE}_{CON2}$ **Conditioned output enable outputs**

$\overline{OE}_{CON1}$ is connected to the $\overline{OE}/\overline{RFSH}$ inputs of the first bank of PSRAMs, and $\overline{OE}_{CON2}$ is connected to the $\overline{OE}/\overline{RFSH}$ inputs of the second bank. Either $\overline{OE}_{CON1}$ or $\overline{OE}_{CON2}$ is driven directly from the $\overline{OE}$ input during an active access, depending on the input address "A." During $\overline{CE}$ inactive, the bq2212 controls both the $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$ outputs to handle the refresh requirements of both banks of PSRAMs simultaneously. During $\overline{CE}$ inactive, both outputs are held high until a bq2212 internal timer requests that an automatic refresh be done (about every 15µs).

To reduce instantaneous power demand, the refresh of the two banks is interlaced. Therefore, an auto-refresh operation occurs every 7.5µs.

If one of the banks is being accessed when the refresh is requested by the internal timer, the refresh is postponed until the end of that active cycle. During a power-fail condition, both $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$ are held low until valid power is restored. Therefore, during a power-fail condition, and the control of refresh cycles for the PSRAMs passes from the bq2212 to the PSRAM internal circuitry, allowing the PSRAMs to self-refresh. Both outputs are active low.

SEAL **Battery isolation signal**

If data retention is not needed, unnecessary battery drain can be avoided by using the SEAL pin. If the SEAL input is taken high during valid V_{CC}, the external batteries are disconnected from V_{OUT} after V_{CC} falls below V_{PFD}. After a subsequent valid V_{CC} level is detected, the SEAL function is removed, and battery backup occurs normally on all power failures until SEAL is activated again. This function is useful after an initial test but

before the device is actually used. All devices are sealed after manufacturing and testing.

$\overline{RST}$ **Reset output**

The $\overline{RST}$ output goes active (low) during a power-fail condition and remains low up to 120ms after valid V_{CC} rises above V_{PFD}. This output can be used as the power-on reset for a microprocessor. Access to the PSRAMs is available after $\overline{RST}$ returns inactive (high).

BUSY **Read/write cycle acknowledge open-drain output**

The BUSY output is an open-drain output that goes low to tell the user that the requested $\overline{CE}$ cycle has started in the PSRAMs. BUSY is low when either $\overline{CE}_{CON1}$ or $\overline{CE}_{CON2}$ is low. Because the bq2212 independently handles the automatic refresh function of the PSRAMs, if the user requests a $\overline{CE}$ cycle during an automatic refresh, the $\overline{CE}$ cycle is delayed until the end of the refresh cycle. The BUSY output remains high until the refresh cycle is completed, and then goes low as the $\overline{CE}$ access is initiated in the selected PSRAM.

The refresh cycle takes less than 500ns and occurs about once every 7.5µs, so there is less than a 6% probability that the access will be delayed by some portion of an automatic refresh cycle. The BUSY output can be used as an input to a wait-state generator for the microprocessor.

$\overline{CE}$ **Chip enable input**

The $\overline{CE}$ input is an active low input used to initiate a read or write cycle to the PSRAMs. Under typical operation, the $\overline{CE}$ pin is passed to either $\overline{CE}_{CON1}$ or $\overline{CE}_{CON2}$, depending on the state of address "A." If the bq2212 is performing an automatic refresh on the PSRAMs when $\overline{CE}$ goes low, then neither $\overline{CE}_{CON1}$ nor $\overline{CE}_{CON2}$ is allowed to go low until the refresh cycle is completed.

$\overline{CE}_{CON1}$/ $\overline{CE}_{CON2}$ **Conditioned chip enable outputs**

$\overline{CE}_{CON1}$ is connected to the $\overline{CE}$ inputs of the first bank of PSRAMs, and $\overline{CE}_{CON2}$ is connected to the $\overline{CE}$ inputs of the second bank. During a user-requested $\overline{CE}$ access, either $\overline{CE}_{CON1}$ or $\overline{CE}_{CON2}$ is driven directly from the $\overline{CE}$ input, depending on the address "A." During $\overline{CE}$ inactive, during a power-fail condition, or during an automatic refresh, both $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ outputs are held high until the end of that condition. Both outputs are active low.

V_{CC} **+5 volt supply input**

A valid V_{CC} condition exists when V_{CC} is above V_{PFD}, typically 4.37V. If V_{CC} falls below this level, a power-fail condition is detected. V_{CC} should not be allowed to fall faster than about 1V/600µs as it passes through the power-fail detection voltage, V_{PFD}. A faster rise time for V_{CC} returning valid is allowed. During valid V_{CC} operation, the bq2212 passes access requests on to the two banks of PSRAMs through the $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, $\overline{OE}_{CON1}$, and $\overline{OE}_{CON2}$ outputs. Also during V_{CC} valid operation, the bq2212 handles the PSRAM refresh requirements through $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$.

During a power-fail condition, both banks of PSRAMs are write-protected and are unavailable for reads. Also during a power-fail condition, refresh control is passed to the PSRAMs by holding $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ high while holding $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$ low, placing the PSRAMs in self-refresh mode.

V_{SS} **Ground**

V_{SS} is the system ground pin. All bq2212 voltages are defined relative to this pin.

Functional Description

Two banks of CMOS pseudo-static RAM can be battery-backed using the V_{OUT} and conditioned chip enable outputs from the bq2212. As the voltage input V_{CC} slows down past V_{PFD} during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external PSRAM as V_{CC} falls below an out-of-tolerance threshold V_{PFD}. Power-fail detection occurs typically at 4.37V.

If a memory access is in progress to any of the two external banks of PSRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µs maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled PSRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to an external backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the regulated supply as V_{CC} rises above the backup cell input voltage

(V_{BCSO}) sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input asserts one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within t_{PFD} (150µs maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

Energy Cell Inputs—BC_P, BC_S

Two backup energy source inputs are provided on the bq2212—a nonrechargeable cell BC_P and a rechargeable cell BC_S. The nonrechargeable cell input is designed to accept any nonrechargeable battery, typically some type of lithium chemistry. If a nonrechargeable cell is not used, the BC_P pin should be grounded. The rechargeable cell input BC_S is designed to accept constant-voltage, current-limited rechargeable vanadium-lithium cells such as Panasonic's VL1220.

During normal +5V power valid operation, 3.2V is output on the BC_S pin and is current-limited internally.

If a rechargeable cell is not used, the BC_S pin must be grounded. If both inputs are used, during power failure the V_{OUT} and $\overline{CE}_{CON}$ outputs are forced high by the rechargeable cell so long as it is greater than 2.5V. Only the rechargeable cell is loaded by the data-retention current of the SRAM until the voltage at the BC_S pin falls below 2.5V. If the voltage at BC_S falls below 2.5V, an internal isolation switch automatically transfers the load from the rechargeable cell to the nonrechargeable cell.

To prevent battery drain when there is no valid data to retain, V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from BC_P and BC_S by either:

- Initial connection of a battery to BC_P or BC_S or
- Taking the SEAL pin high during power-valid operation. The battery is connected to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ immediately on subsequent application and removal of V_{CC}.

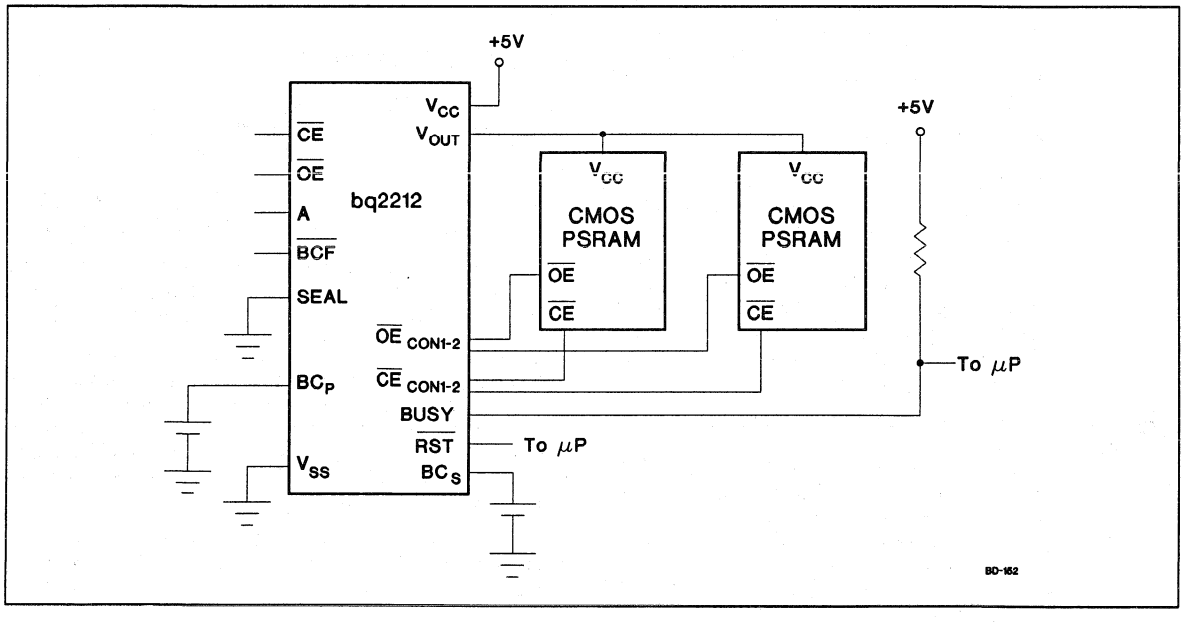


Figure 1. Hardware Hookup

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

3

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to 85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	300	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.50	5.0	5.5	V	
V_{BCP}	Backup cell input voltage	2.5	-	3.4	V	
V_{BCS}		2.5	-	3.4		
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, backup supply	V_{BC} - 0.2	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	3	6	mA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, $\overline{OE}_{CON1}$, $\overline{OE}_{CON2}$, $\overline{RST}$, $\overline{BCF}$, and BUSY
V_{PFD}	Power-fail detect voltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, $\overline{OE}_{CON1}$, $\overline{OE}_{CON2}$, $\overline{RST}$, $\overline{BCF}$, and BUSY
V_{OUT1}	V_{OUT} voltage	2.7	3.0	3.3	V	$V_{CC} > V_{BC}$; when V_{CC} falls below 3.3V, V_{OUT1} tracks V_{CC} until battery switch-over occurs
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.2	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 140µA
V_{BC}	Active backup cell voltage	-	V_{BCS}	-	V	V_{BCS} > 2.5V
		-	V_{BCP}	-	V	V_{BCS} < 2.5V
R_{BCS}	BCs charge output internal resistance	500	1000	1500	Ω	$V_{BCSO} \geq$ 3.0V
V_{BCSO}	BCs charge output voltage	3.1	3.2	3.3	V	$V_{CC} > V_{PFD}$, $\overline{RST}$ inactive, full charge or no load
V_{BCF}	Battery-fail voltage	2.5	-	-	V	
I_{OUT1}	V_{OUT} current	-	-	80	mA	$V_{CC} \geq V_{PFD}$
I_{OUT2}	V_{OUT} current	-	140	-	µA	$V_{CC} < V_{PFD}$

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 2

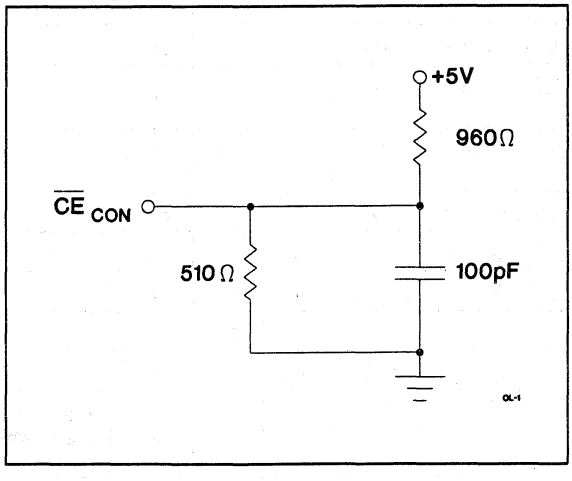


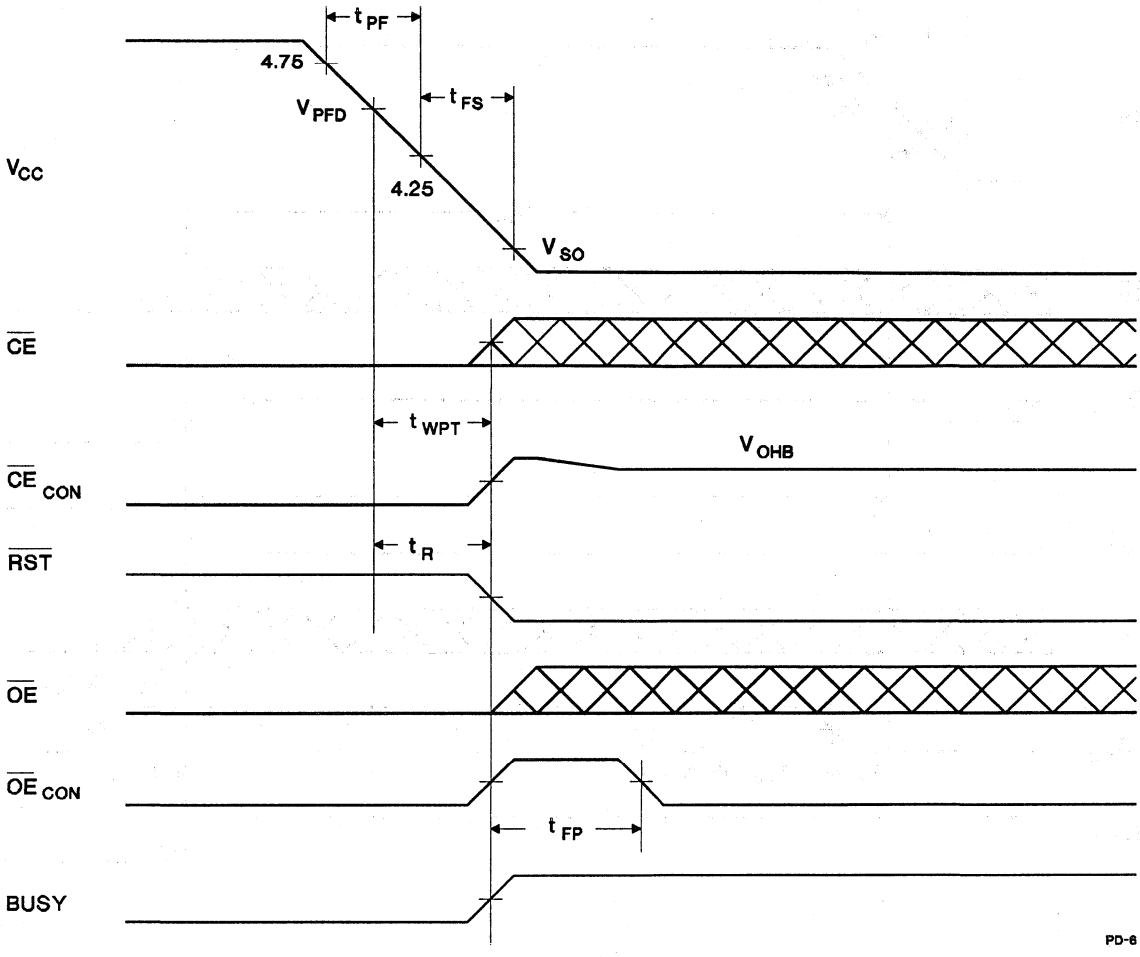
Figure 2. Output Load

Power-Fail Control and Operation ($T_A = T_{OPR}$)

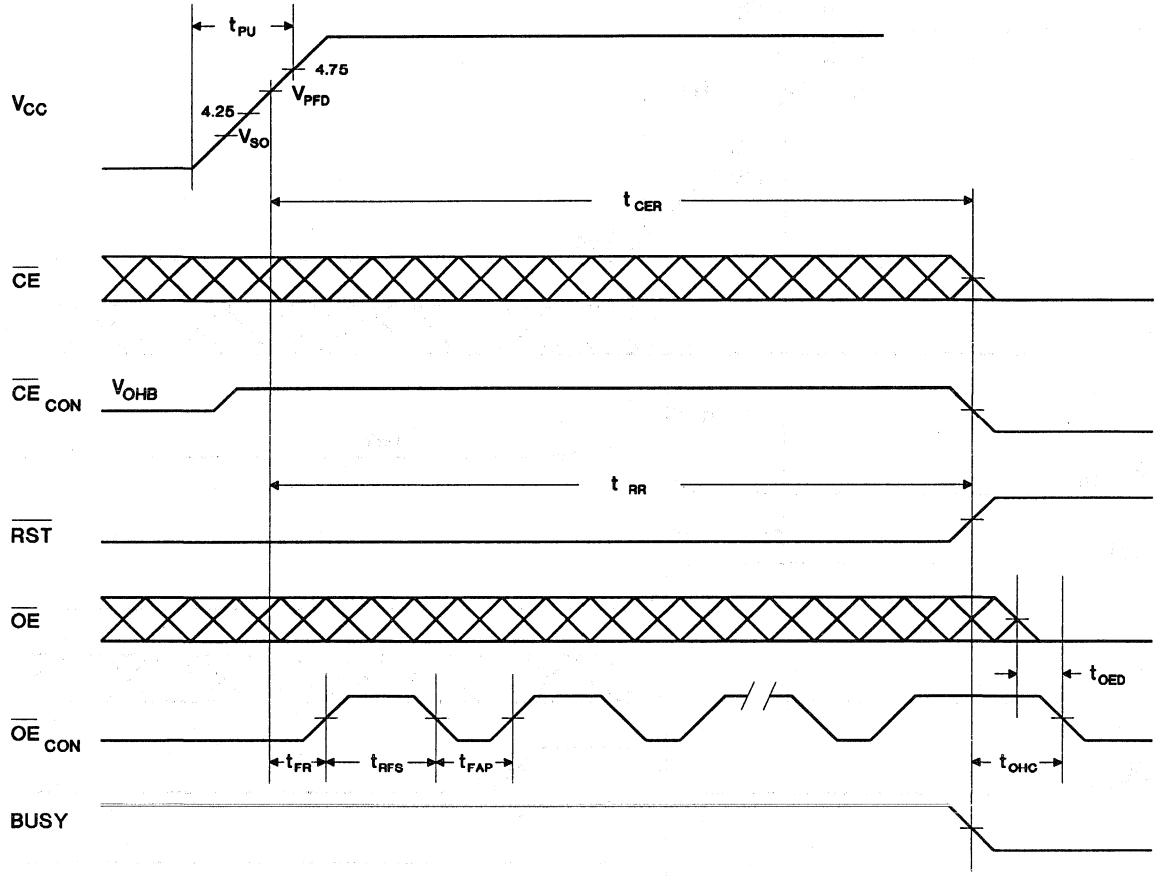
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	300	-	-	µs	
t_{PU}	V_{CC} slew 0 to 4.75 V	300	-	-	µs	
t_{CED}	Chip-enable propagation delay	-	7	10	ns	
	Chip-enable propagation delay if requested during a refresh cycle	-	-	500	ns	t_{CED} has a <6% probability of being longer than 10ns due to the bq2212 finishing an internal refresh cycle.
t_{BSD}	$\overline{CE}$ low to BUSY low	t_{CED}	-	t_{CED}	ns	
t_{CE}	$\overline{CE}$ hold past BUSY	80	-	-	ns	Minimum $\overline{CE}$ pulse width starting with BUSY low
t_P	$\overline{CE}$ precharge time	40	-	-	ns	
t_{AS}	Input A set up to $\overline{CE}$	0	-	-	ns	
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	t_{CER}	t_{CER}	t_{CER}	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is inactive
t_{CER}	Chip-enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{AH}	Input A hold time	20	-	-	ns	Address hold from busy low
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active
t_{WPT}	Write-protect time	t_R		t_R	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_{FP}	$\overline{PSRAM}$ refresh precharge time	40	-	60	ns	
t_{FR}	PSRAM data-retention recovery time	5	-	-	ms	
t_{RFS}	PSRAM self-refresh recovery time	-	-	15	µs	
t_{FAP}	PSRAM automatic refresh	80	-	-	ns	
t_{OHC}	$\overline{CE}_{CON}$ low to $\overline{OE}_{CON}$ low delay	20	-	-	ns	
t_{OF}	$\overline{CE}_{CON}$ high to $\overline{OE}_{CON}$ high	-	-	15	ns	
t_{OED}	$\overline{OE}$ to $\overline{OE}_{CON}$ delay	-	-	15	ns	
t_{SEAL}	Minimum seal pulse width	50	-	-	µs	
t_{SPT}	Seal protect time	t_{CER}	-	t_{CER}	ms	Time during which SEAL input is ignored after V_{CC} passes V_{PFD} on power-up.

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

Power-Down Timing

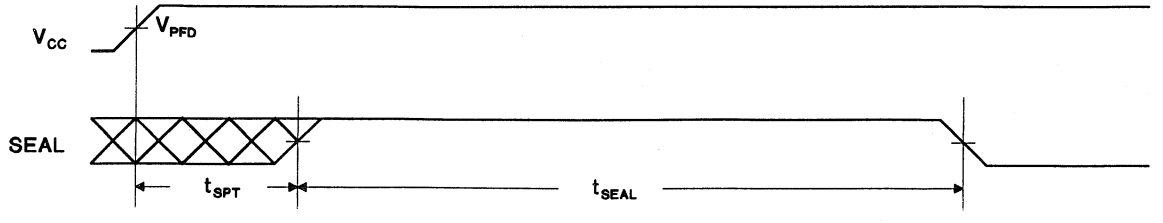


Power-Up Timing



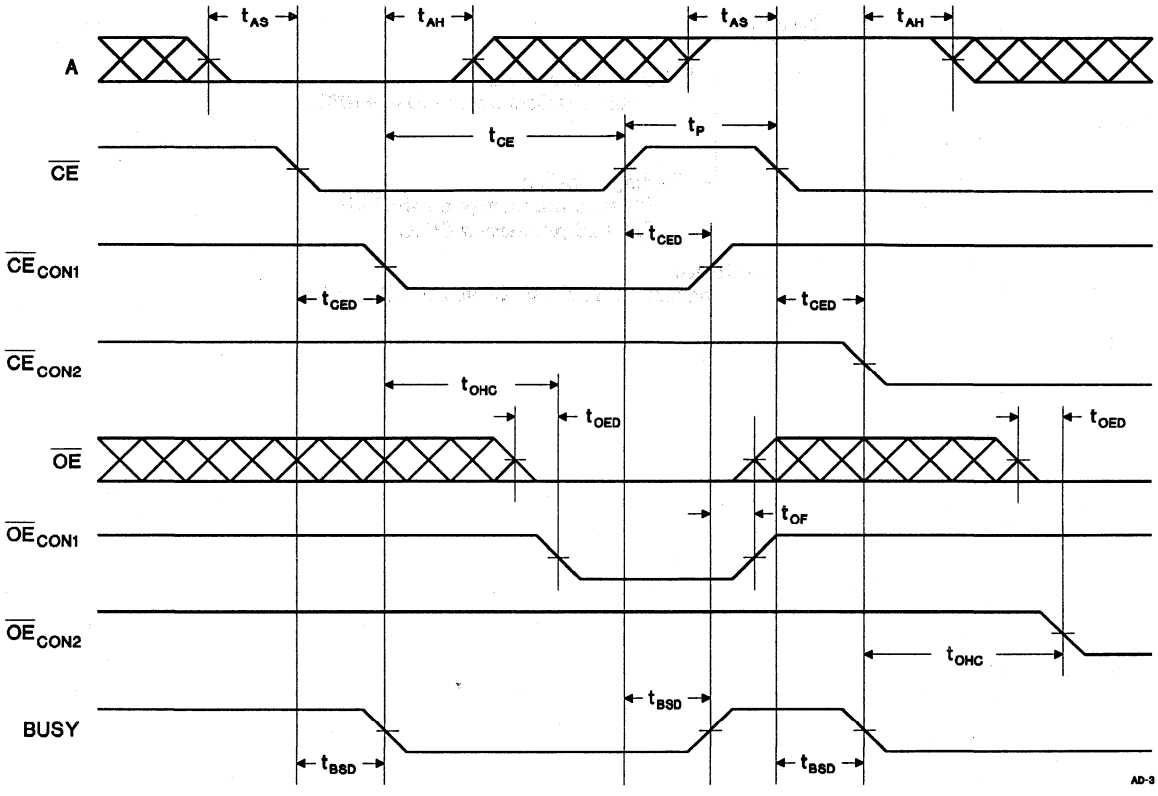
PU-10

SEAL Timing



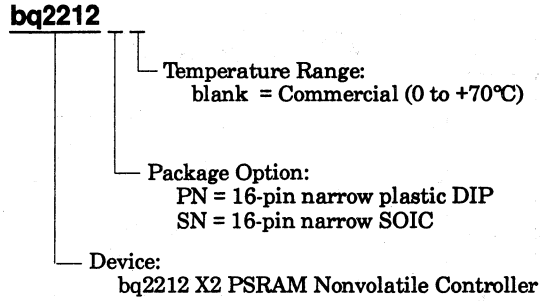
SL-1

Address-Decode Timing



3

Ordering Information



BENCHMARQ

bq2502

Integrated Backup Unit

Features

- Power monitoring, backup supply, and switching for 3V battery-backup applications
- Write-protect control
- Input decoder allows control of up to 2 banks of SRAM
- 3V backup power output
- Internal 130mAh lithium coin cell
- Reset output for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2502 Integrated Backup Unit provides all the necessary functions for converting one or two banks of standard CMOS SRAM into non-volatile read/write memory.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the internal battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the internal lithium supply to the V_{CC} supply.

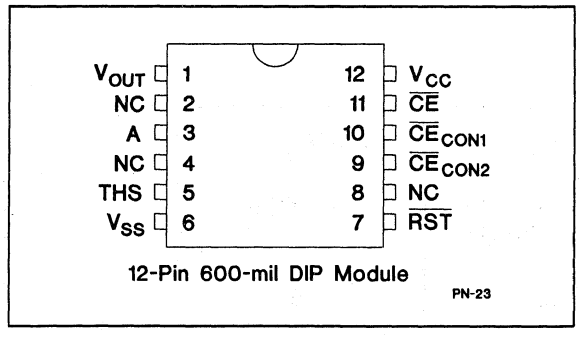
The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

The internal lithium cell is initially electrically isolated, protecting the battery from accidental discharge. Connection to the battery is made only after the first application of V_{CC}.

3

Pin Connections



12-Pin 600-mil DIP Module

PN-23

Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank select input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip enable output pins from the bq2502. As the voltage input V_{CC} slows down during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation. If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µsec maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

The reset output ($\overline{RST}$) goes active within t_R (150 µsec maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The internal lithium cell is capable of supplying 3V on V_{OUT} for an extended period of time. The cumulative length of time that the external SRAMs retain data in the absence of power is a function of the data-retention current of the SRAMs used. The initial capacity of the internal lithium cell is 130mAh. Typically, if the data-retention currents for two external SRAMs are 1µA per SRAM at room temperature, nonvolatility is calculated to be for more than 7 years. If only one external SRAM is used, the data-retention time increases to more than 13 years.

The bq2502 battery life is a function of the time spent in battery-backed mode and the data-retention current of the external SRAM. For example, office equipment is generally powered on for 8 hours and powered off for 16 hours. Under these conditions, a single bq2502 provides SRAMs drawing 2µA total data-retention current with more than 10 years of nonvolatility.

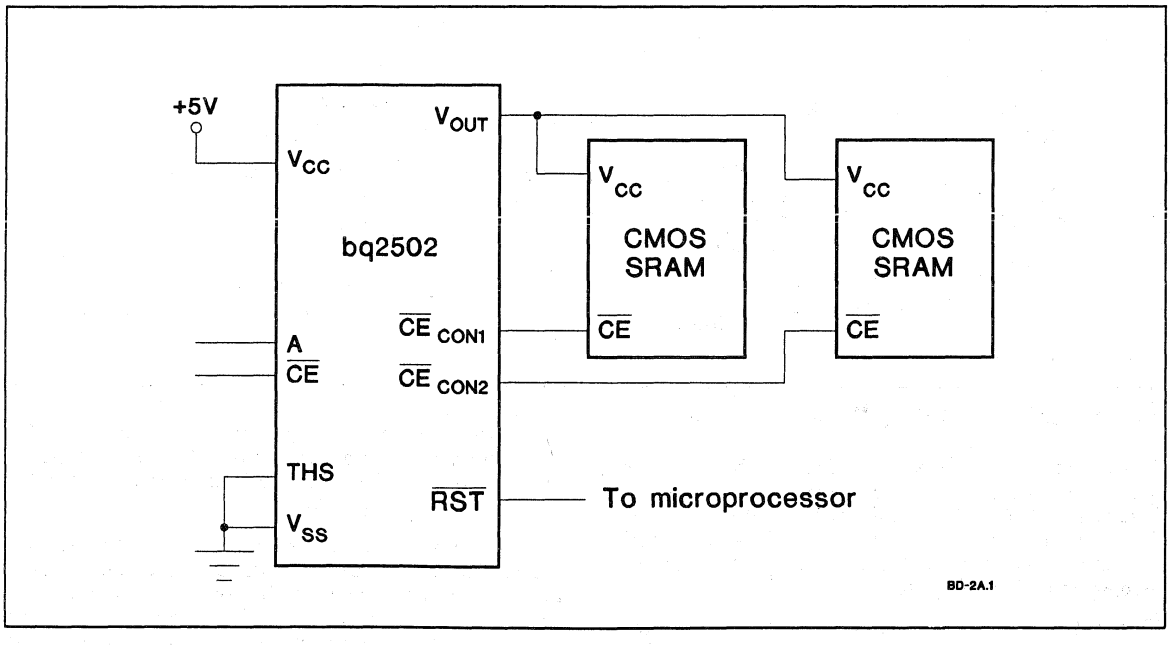


Figure 1. Hardware Hookup (5% Supply Operation)

As shipped from Benchmarq, the internal lithium cell is electrically isolated from V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$. Self-discharge in this condition is less than .5% per year at 20°C.

Note: Following the first application of V_{CC}, this isolation is broken, and the backup cell provides power to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ for the external SRAM.

Caution:

Care should be taken to avoid inadvertent discharge through V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ after battery isolation has been broken.

This isolation can be reestablished by applying a valid isolation signal to the bq2502. This signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. Between these two points in time, $\overline{CE}$ must be brought to (0.48 to 0.52) * V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}. See Figure 2.

The battery is connected to V_{OUT} immediately on subsequent application and removal of V_{CC}.

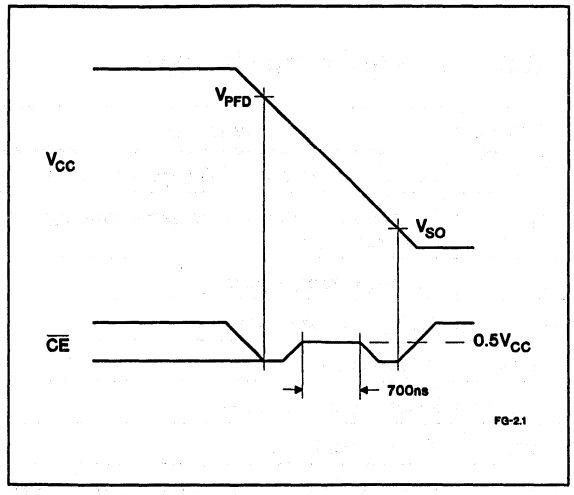


Figure 2. Battery Isolation Signal

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	
T_{STG}	Storage temperature	-40 to 70	°C	
T_{BIAS}	Temperature under bias	-10 to 70	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BAT}.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity	-	130	-	mAhr	Refer to graphs in Typical Battery Characteristics section.
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, backup supply	V_{BAT} - 0.3	-	-	V	V_{BAT} > V_{CC}, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
V_{BAT}	Internal battery voltage	-	2.9	-	V	Refer to graphs in Typical Battery Characteristics section.
I_{CC}	Operating supply current	-	3	6	mA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, and $\overline{RST}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage	-	2.9	-	V	
I_{CCDR}	Data-retention mode current from internal battery	-	-	100	nA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, and $\overline{RST}$.
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	V_{CC} > V_{BAT}, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	V_{CC} > V_{BAT}, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage from internal battery	V_{BAT} - 0.2	-	-	V	V_{CC} < V_{BAT}, I_{OUT} = 100µA, from internal battery
I_{OUT1}	V_{OUT} current	-	-	160	mA	V_{OUT} ≥ V_{CC} - 0.3V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BAT}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 V to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

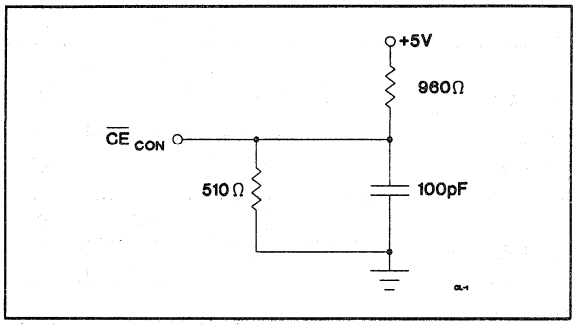
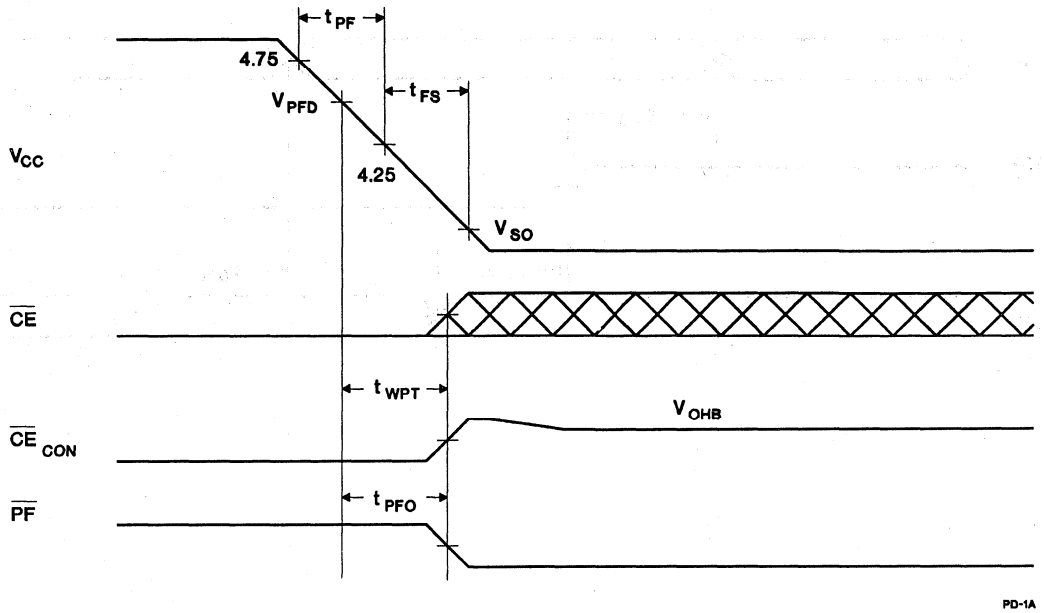


Figure 3. Output Load

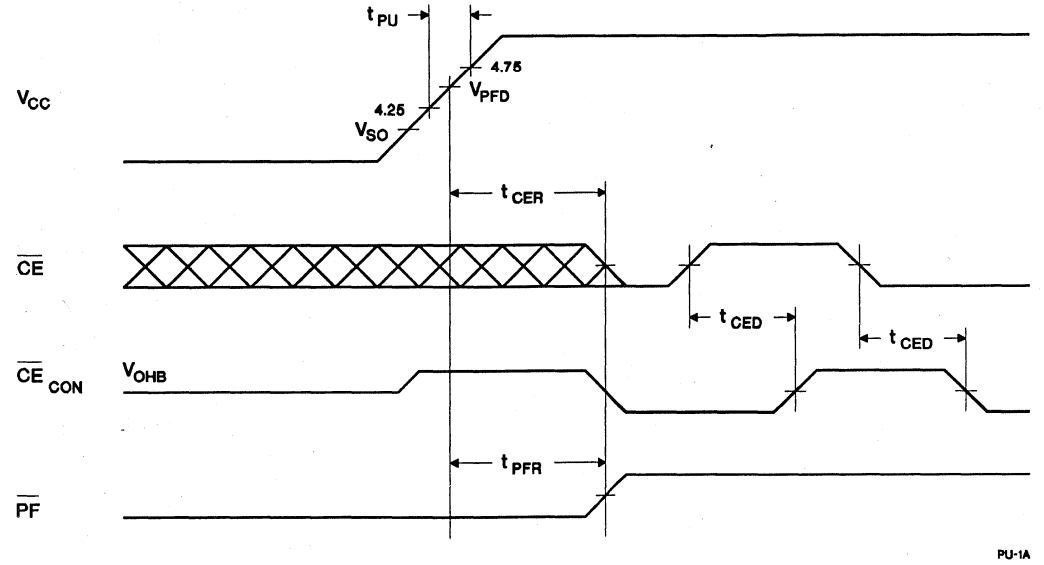
Power-Fail Control (T_A = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75 V	0	-	-	µs	
t_{CED}	Chip-enable propagation delay	-	7	10	ns	
t_{CER}	Chip-enable recovery time	t_{RR}	-	t_{RR}	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	40	80	120	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0	-	-	ns	
t_{WPT}	Write-protect time	t_R	-	t_R	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active

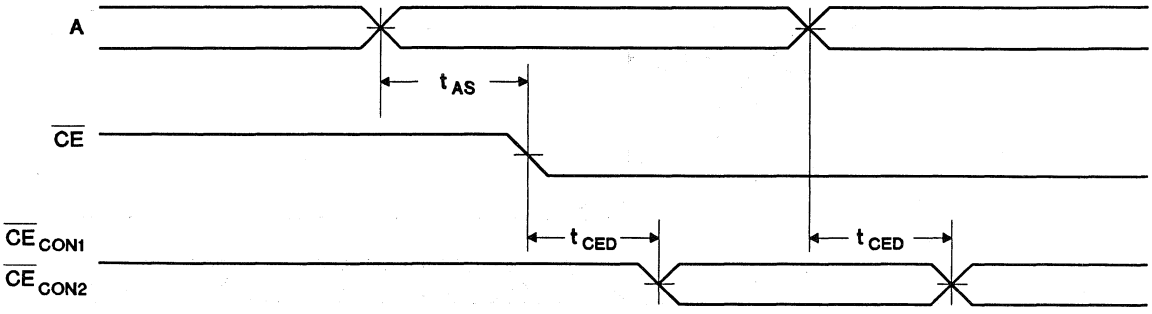
Power-Down Timing



Power-Up Timing



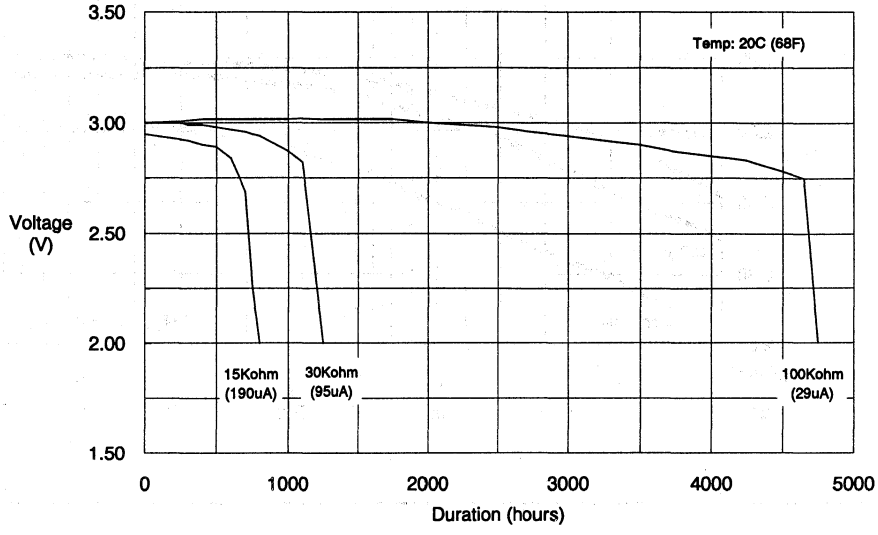
Address-Decode Timing



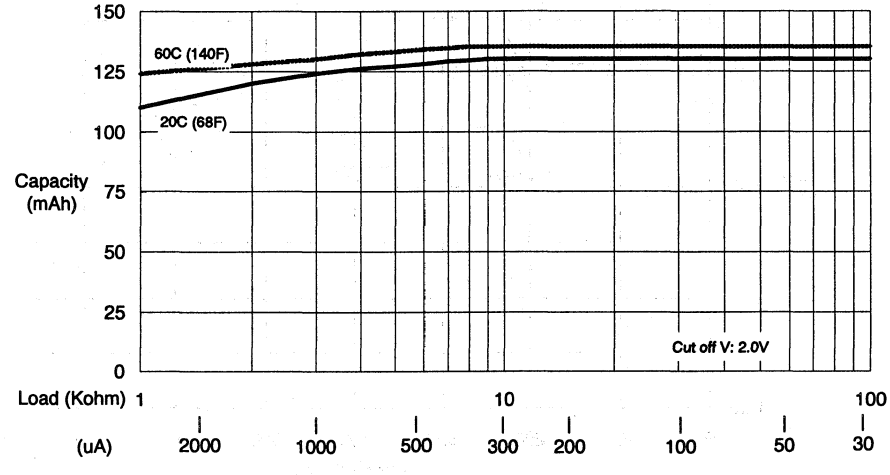
AD-1A

Typical Battery Characteristics (source = Panasonic)

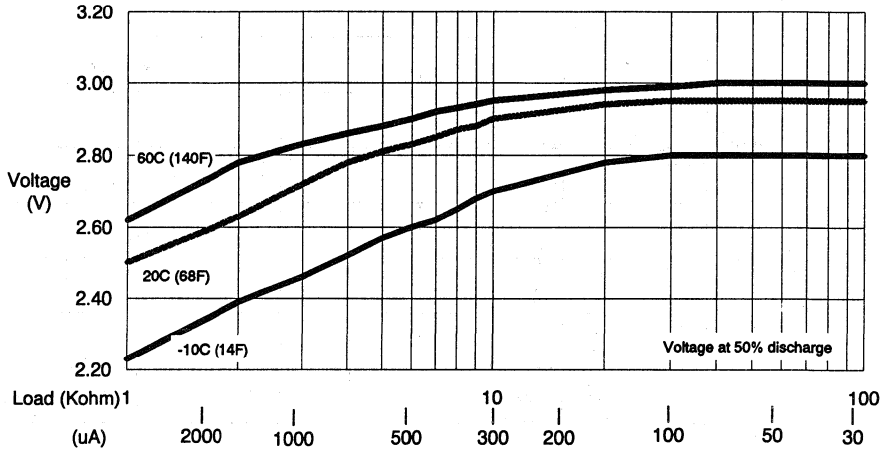
CR1632 Load Characteristics



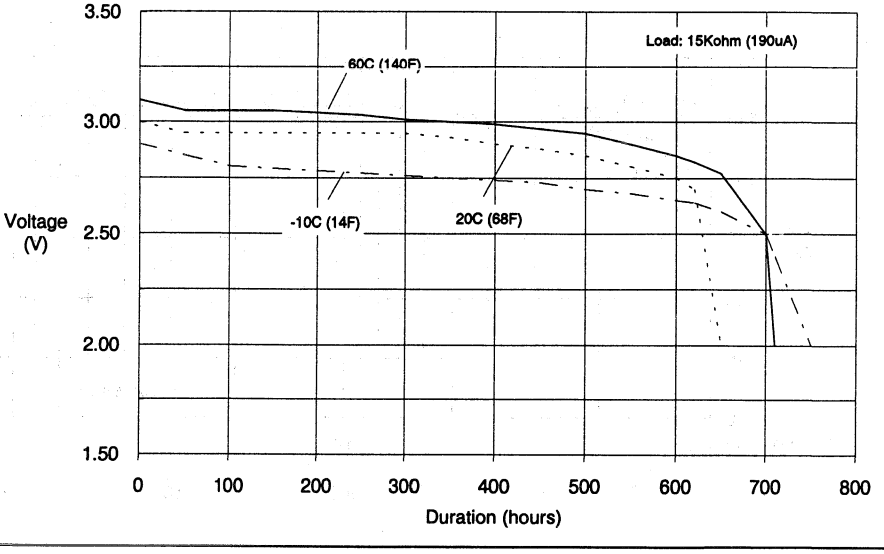
CR1632 Capacity vs. Load Resistance



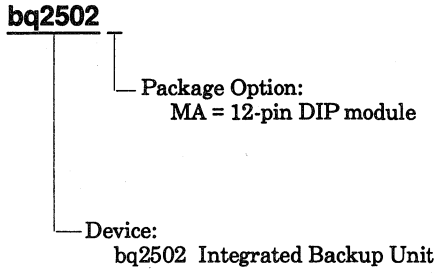
CR1632 Operating Voltage vs. Load Resistance



CR1632 Temperature Characteristics



Ordering Information



Notes

BENCHMARQ

bq3285

Real-Time Clock (RTC)

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 114 bytes of general nonvolatile storage
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing
- Less than 0.5 µA load under battery operation
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

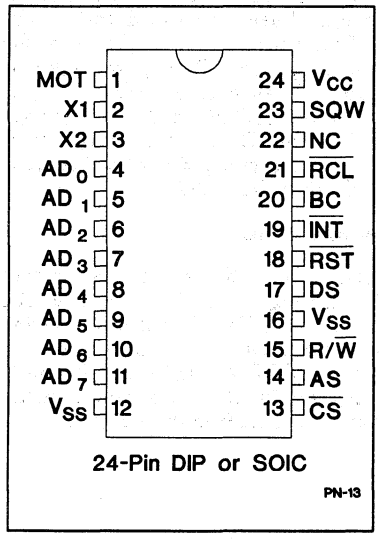
The CMOS bq3285 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

The bq3285 write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285 is a fully compatible real-time clock for IBM AT compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

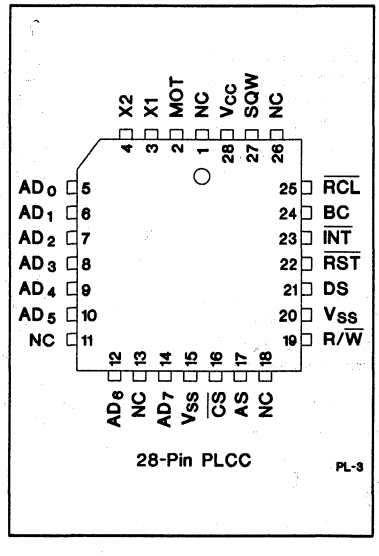
4

Pin Connections



24-Pin DIP or SOIC

PN-13



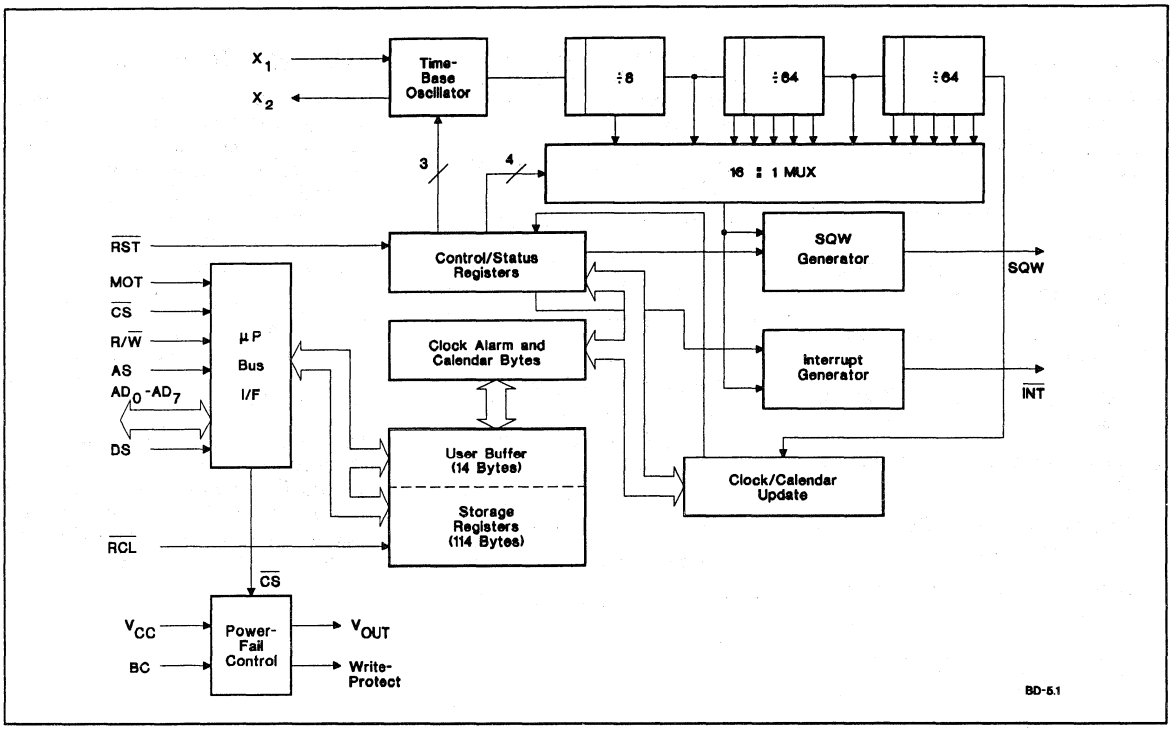
28-Pin PLCC

PL-3

Pin Names

AD0–AD7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{RCL}$	RAM clear input
BC	3V backup cell input
X1, X2	Crystal inputs
NC	No connect
VCC	+5V supply
VSS	Ground

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20KΩ resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/output**

The bq3285 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq3285 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP, SOIC, and PLCC packages with MOT = V_{CC}, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3285 bus cycle. During a read cycle, the bq3285 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3285.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW **Square-wave output**

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

$\overline{RCL}$ **RAM clear input**

A low level on the $\overline{RCL}$ pin causes the contents of each of the 114 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 125ms in the presence of V_{CC} when the oscillator is running. Using RAM clear does not affect the battery load.

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of power. When V_{CC} slows down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

$\overline{RST}$ **Reset input**

The bq3285 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq3285 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

X1, X2 **Crystal input**

The X1, X2 inputs are provided for an external 32.768Khz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

In the absence of a crystal, an oscillated output of 32.768kHz can be fed into the X1 input.

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Functional Description

Address Map

The bq3285 provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285.

Update Period

The update period for the bq3285 is one second. The bq3285 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

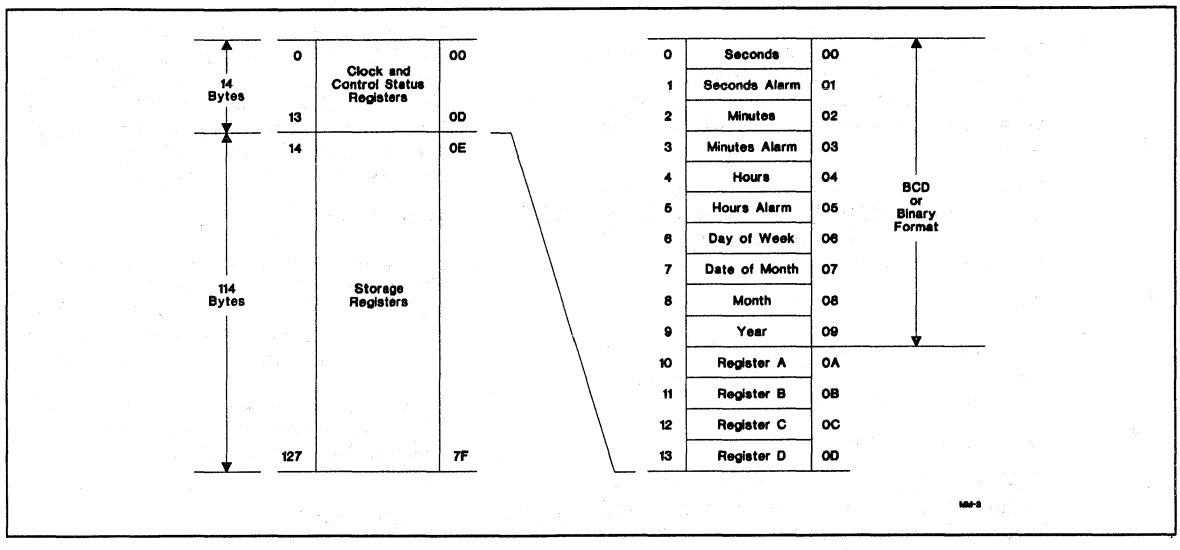

Figure 1. Address Map

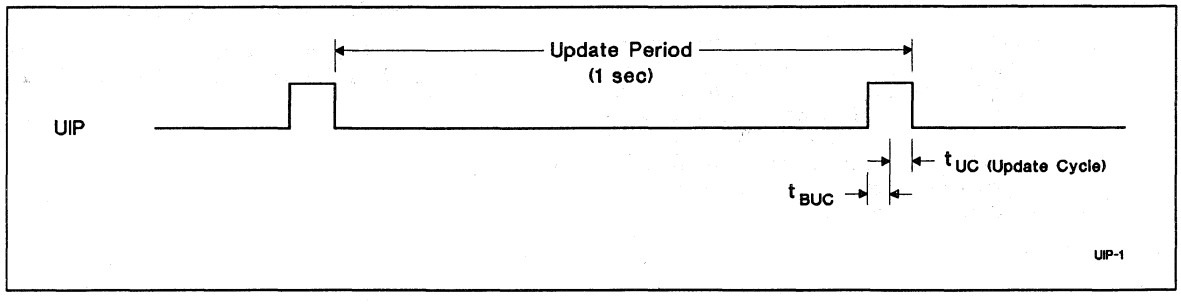

Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

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Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq3285 divides the 32.768kHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B.

Interrupts

The bq3285 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122µs to 500ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of each update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3285 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	4.096	kHz	244.141	µs
0	1	0	1	2.048	kHz	488.281	µs
0	1	1	0	1.024	kHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3).

Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285 and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

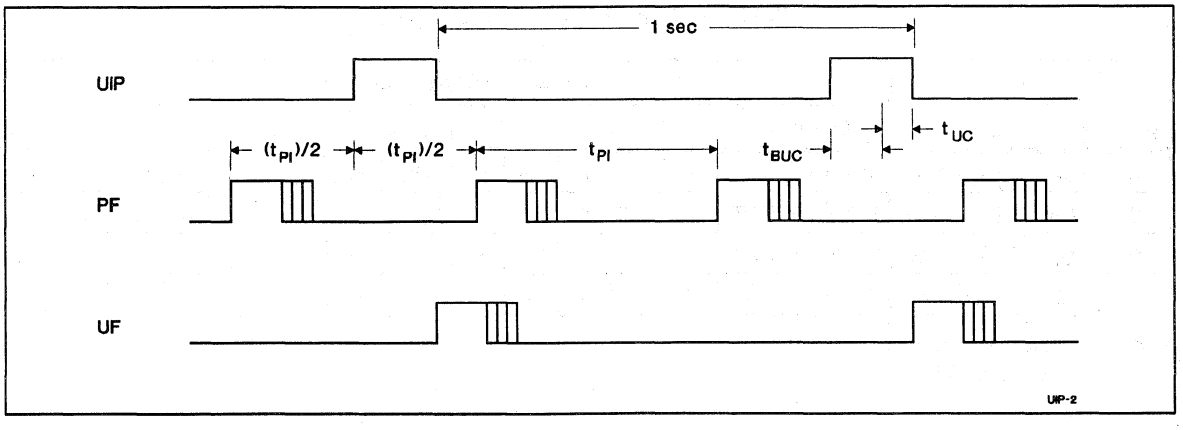

Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3285 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3285 write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285 are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.
1. Except bit 7.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

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Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.5	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = Vss to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, V_{OUT} = Vss to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL}$ = Vss.	-	-	275	µA	Internal 20K pull-up
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-275	µA	Internal 20K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

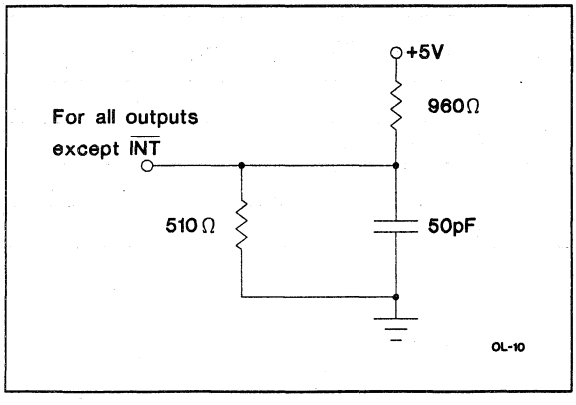


Figure 4. Output Load A

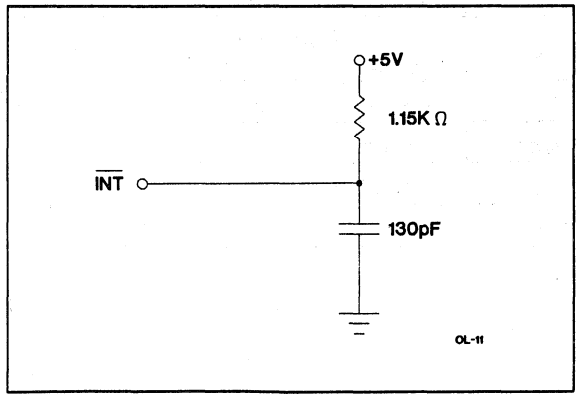
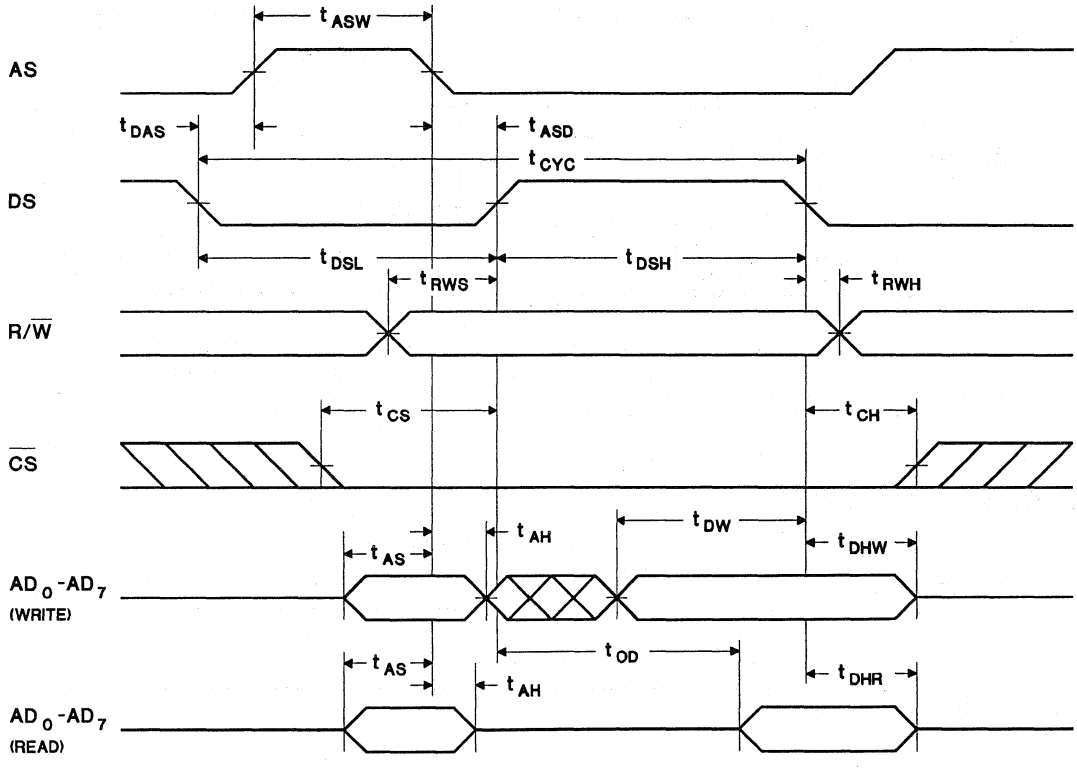


Figure 5. Output Load B

Read/Write Timing (TA = TOPR, VCC = 5V ± 10%)

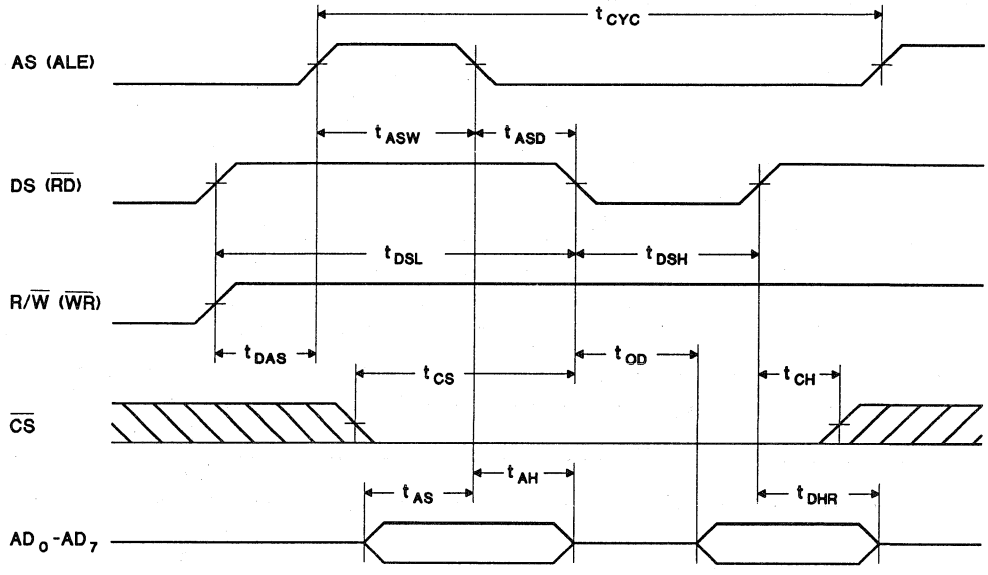
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns	
t_{ASW}	Pulse width, AS high	30	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

Motorola Bus Read/Write Timing



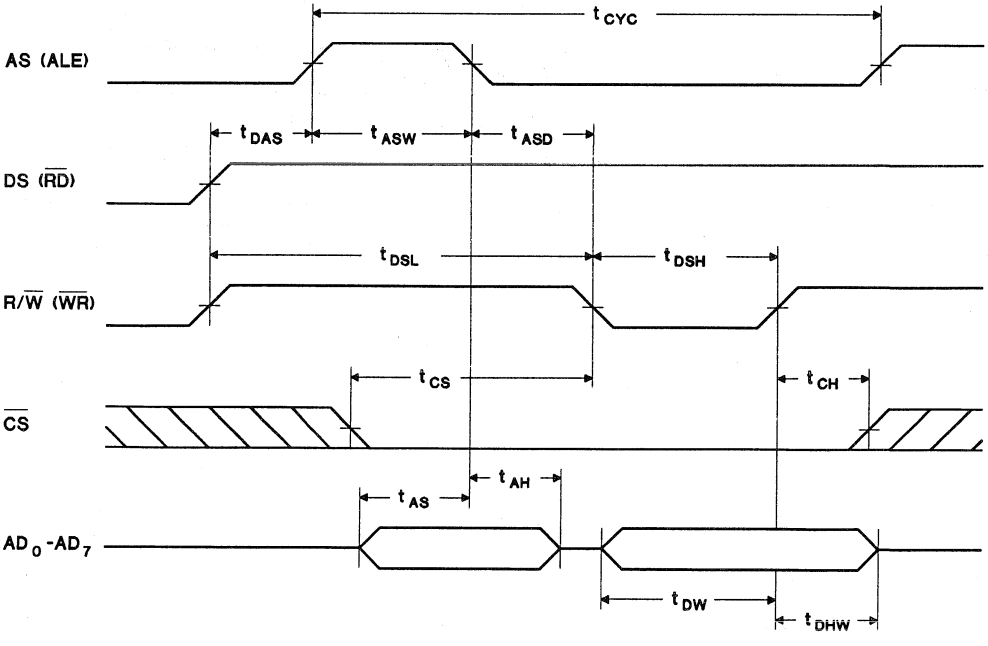
4

Intel Bus Read Timing



RC-5

Intel Bus Write Timing



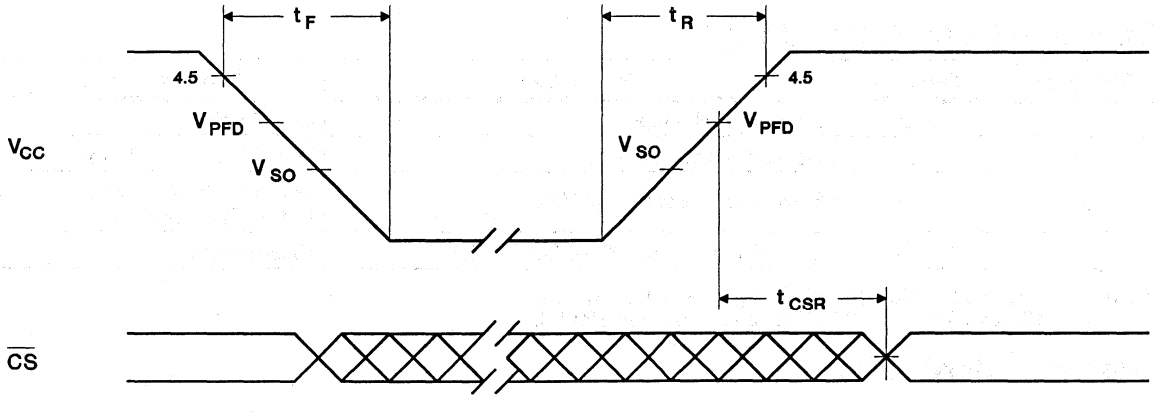
WC-5

Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing

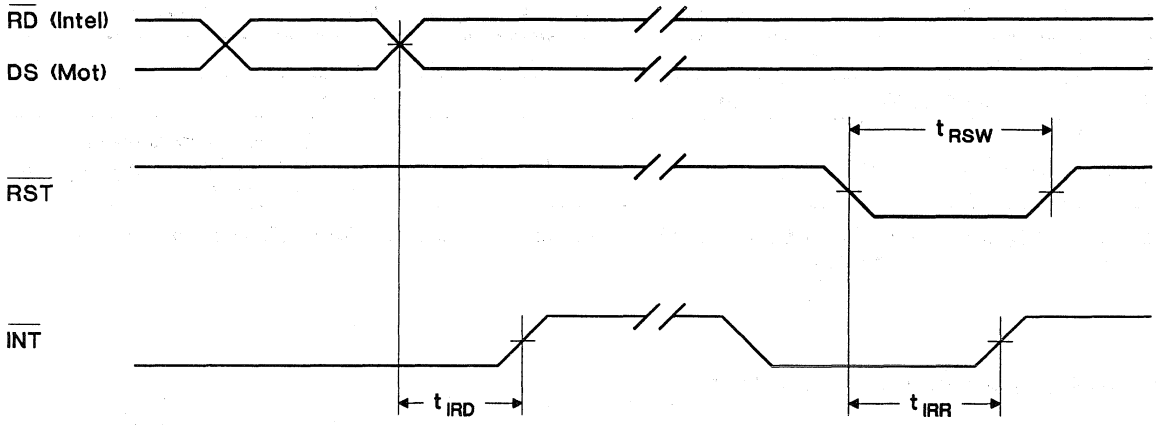


PD-4A

Interrupt Delay Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)	-	-	2	µs

Interrupt Delay Timing



INT-1

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4-2	Address strobe input	Clarification
1	4-11	Backup cell voltage V_{BC}	Was 2.0 min; is 2.5 min
1	4-12	Power-fail detect voltage V_{PFD}	Was 4.1 min, 4.25 max; is 4.0 min, 4.35 max
2	4-3, 4-12	Crystal type Daiwa DT-26 (not DT-26S)	Clarification

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.

Ordering Information

bq3285 _ -

- Temperature:
  blank = Commercial (0 to +70°C)
- Package Option:
  P = 24-pin plastic DIP (0.600)
  S = 24-pin SOIC (0.300)
  Q = 28-pin quad PLCC
- Device:
  bq3285 Real-Time Clock with 114 bytes of general storage

bq3285E/L

Real-Time Clock (RTC)

Features

- System wake-up capability—alarm interrupt output active in battery-backup mode
- 2.7–3.6V operation (bq3285L); 4.5–5.5V operation (bq3285E)
- 242 bytes of general nonvolatile storage
- 32.768KHz output for power management
- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- Less than 0.5 µA load under battery operation
- Selectable Intel or Motorola bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP, SOIC, or SSOP and 28-pin PLCC

General Description

The CMOS bq3285E/L is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. The bq3285L supports 3V systems. Other bq3285E/L features include three maskable interrupt sources, square-wave output, and 242 bytes of general nonvolatile storage.

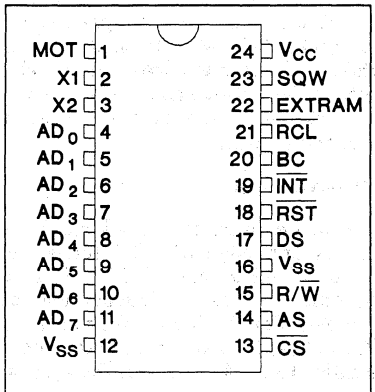
A 32.768KHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode.

The bq3285E/L write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285E/L is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

4

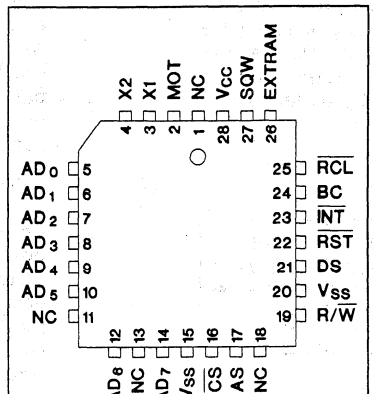
Pin Connections



24-Pin DIP or SOIC/SSOP

PN-41

Pin Names

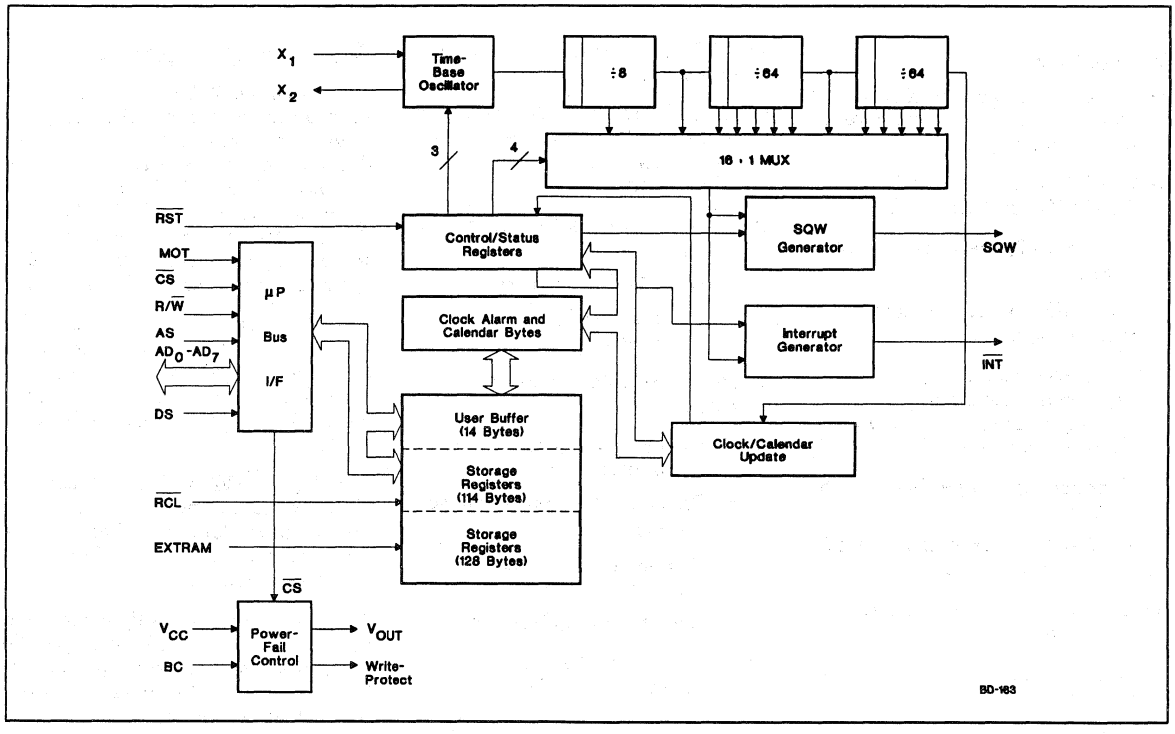


28-Pin PLCC

PL-10

$\overline{AD_0}$-AD_7	Multiplexed address/ data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
EXTRAM	Extended RAM enable
$\overline{RCL}$	RAM clear input
BC	3V backup cell input
X1, X2	Crystal inputs
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 30KΩ resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/output**

The bq3285E/L bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 and EXTRAM is latched into the bq3285E/L on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7 and EXTRAM. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP and SOIC packages with MOT = V_{SS}, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3285E/L bus cycle. During a read cycle, the bq3285E/L drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3285E/L.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285E/L.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. This allows alarm $\overline{INT}$ to be valid in battery-backup mode. To use this feature, $\overline{INT}$ must be connected to a power supply other than V_{CC}. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW **Square-wave output**

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

A 32.768kHz output is enabled by setting the SQWE bit in register B to 1 and the 32KE bit in register C to 1 after setting OSC2–OSC0 in register A to 011 (binary).

EXTRAM **Extended RAM enable**

Enables 128 bytes of additional nonvolatile SRAM. It is connected internally to a 30KΩ pull-down resistor. To access the RTC registers, EXTRAM must be low.

$\overline{RCL}$ **RAM clear input**

A low level on the $\overline{RCL}$ pin causes the contents of each of the 242 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 125ms in the presence of V_{CC}. Using RAM clear does not affect the battery load. This pin is connected internally to a 30KΩ pull-up resistor.

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of system power. When V_{CC} slows down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

$\overline{RST}$ **Reset input**

The bq3285E/L is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high impedance, and the bq3285E/L is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

X1, X2 **Crystal input**

The X1, X2 inputs are provided for an external 32.768kHz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

In the absence of a crystal, a 32.76 waveform can be fed into the X1 input.

4

Functional Description

Address Map

The bq3285E/L provides 14 bytes of clock and control/status registers and 242 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285E/L.

Update Period

The update period for the bq3285E/L is one second. The bq3285E/L updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285E/L copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

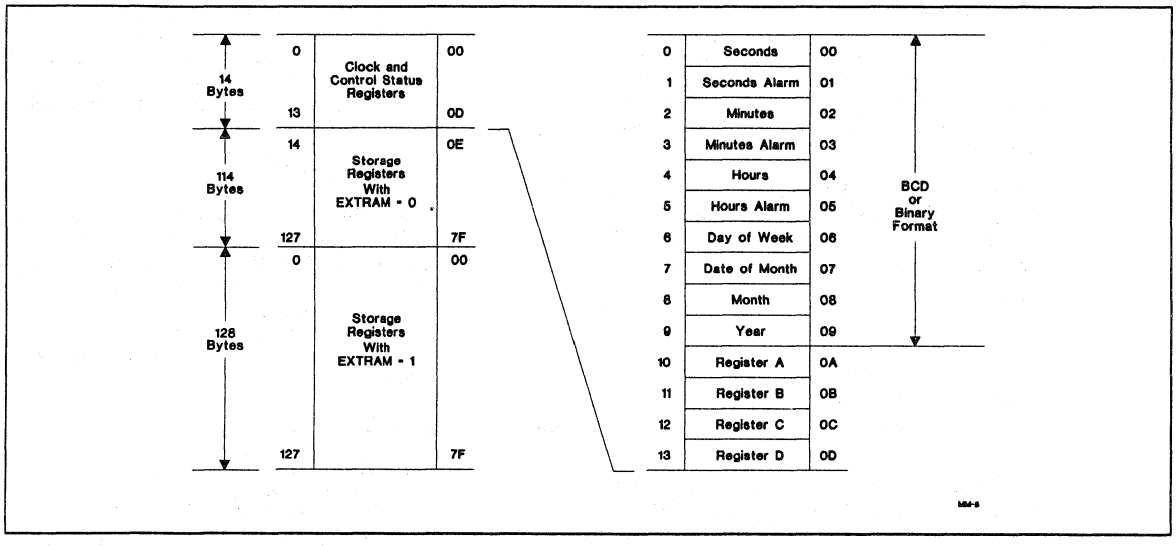


Figure 1. Address Map

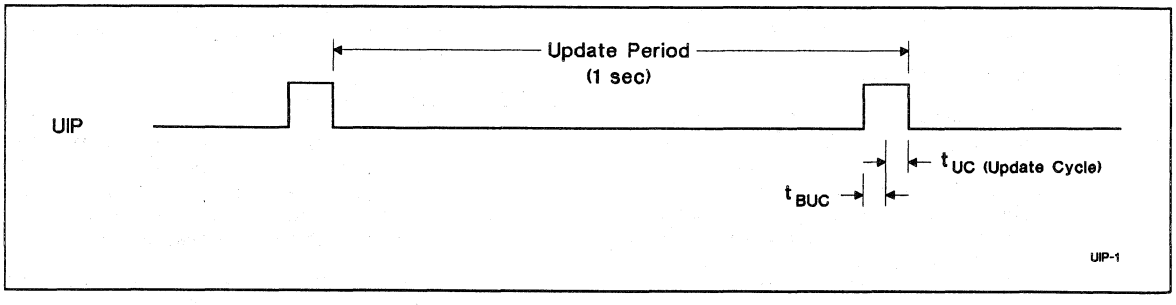


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

4

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq3285E/L divides the 32.768kHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B. A 32.768kHz output may be selected by setting OSC2–OSC0 in register A to 011 while SQWE = 1 and 32KE = 1.

Interrupts

The bq3285E/L allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a "wake-up" feature.
- The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3285E/L interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits							Square Wave		Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	1	0	0	0	0	0	None		None	
0	1	0	0	0	0	1	256	Hz	3.90625	ms
0	1	0	0	0	1	0	128	Hz	7.8125	ms
0	1	0	0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	1	0	0	4.096	kHz	244.141	µs
0	1	0	0	1	0	1	2.048	kHz	488.281	µs
0	1	0	0	1	1	0	1.024	kHz	976.5625	µs
0	1	0	0	1	1	1	512	Hz	1.953125	ms
0	1	0	1	0	0	0	256	Hz	3.90625	ms
0	1	0	1	0	0	1	128	Hz	7.8125	ms
0	1	0	1	0	1	0	64	Hz	15.625	ms
0	1	0	1	0	1	1	32	Hz	31.25	ms
0	1	0	1	1	0	0	16	Hz	62.5	ms
0	1	0	1	1	0	1	8	Hz	125	ms
0	1	0	1	1	1	0	4	Hz	250	ms
0	1	0	1	1	1	1	2	Hz	500	ms
0	1	1	X	X	X	X	32.768	kHz	same as above defined by RS3–RS0	

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3). Setting OSC2–OSC0 in register A to 011 does not affect the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt is active in battery-backup mode, providing a "wake-up" capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

The EXTRAM pin must be low to access the RTC registers. Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285E/L and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns

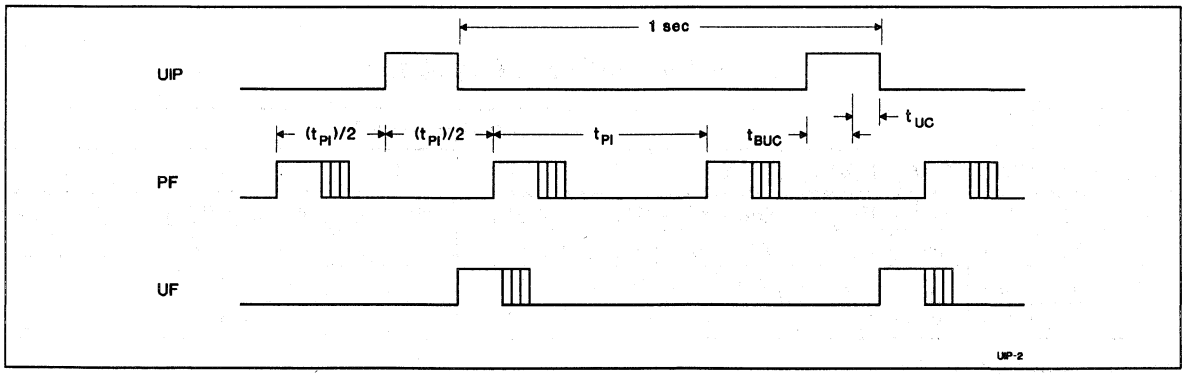


Figure 3. Update-Ended/Periodic Interrupt Relationship

the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

Power-Down/Power-Up Cycle

The bq3285E and bq3285L power-up/power-down cycles are different. The bq3285L continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (2.53V typical), the bq3285L write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

The bq3285E continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3285E write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285E/L are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.
2. Read/write only when OSC2–OSC0 in register A is 011 (binary).

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285E/L increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0

Register C is the read-only event status register.

Bits 0, 1, 3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	-	0	0

These bits are always set to 0.

32KE - 32kHz Enable Output

7	6	5	4	3	2	1	0
-	-	-	-	-	32KE	-	-

This bit may be set to a 1 only when the OSC2–OSC0 bits in register A are set to 011. Setting OSC2–OSC0 to anything other than 011 clears this bit. If SQWE in register B and 32KE are set, a 32.768kHz waveform is output on the square wave pin.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings—bq3285E

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

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Absolute Maximum Ratings—bq3285L

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 6.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 6.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions—bq3285E ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.5	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Recommended DC Operating Conditions—bq3285L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	2.7	3.15	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.6	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.4	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Crystal Specifications—bq3285E/L (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

DC Electrical Characteristics—bq3285E (T_A = TOPR, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = Vss to Vcc
I_{LO}	Output leakage current	-	-	± 1	µA	AD0–AD7, $\overline{INT}$, and SQW in high impedance, V_{OUT} = Vss to Vcc
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current	-	300	-	µA	V_{IN} = Vss or Vcc, $\overline{CS}$ ≥ Vcc - 0.2
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL}$ = Vss.	-	-	185	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = Vcc	-	-	-185	µA	Internal 30K pull-down
	Input current when MOT = Vss	-	-	0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = Vcc	-	-	-185	µA	Internal 30K pull-down
	Input current when EXTRAM = Vss	-	-	0	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, Vcc = 5V or V_{BC} = 3V.

4

DC Electrical Characteristics—bq3285L (T_A = TOPR, V_{CC} = 3.15V ±0.45V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = Vss to Vcc
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7 and $\overline{INT}$ in high impedance, V_{OUT} = Vss to Vcc
V_{OH}	Output high voltage	2.2	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.0 mA
I_{CC}	Operating supply current	-	5	9	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current	-	100	-	µA	V_{IN} = Vss or Vcc, $\overline{CS}$ ≥ Vcc - 0.2
V_{SO}	Supply switch-over voltage	-	V_{PFD}	-	V	V_{BC} > V_{PFD}
		-	V_{BC}	-	V	V_{BC} < V_{PFD}
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, Vcc < V_{BC}
V_{PFD}	Power-fail-detect voltage	2.4	2.53	2.65	V	
I_{RCL}	Input current when $\overline{RCL}$ = Vss.	-	-	120	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = Vcc	-	-	-120	µA	Internal 30K pull-down
	Input current when $\overline{MOT}$ = Vss	-	-	0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = Vcc	-	-	-120	µA	Internal 30K pull-down
	Input current when EXTRAM = Vss	-	-	0	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, Vcc = 3V.

Capacitance—bq3285E/L (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested. It does not include the X1 or X2 pin.

AC Test Conditions—bq3285E

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

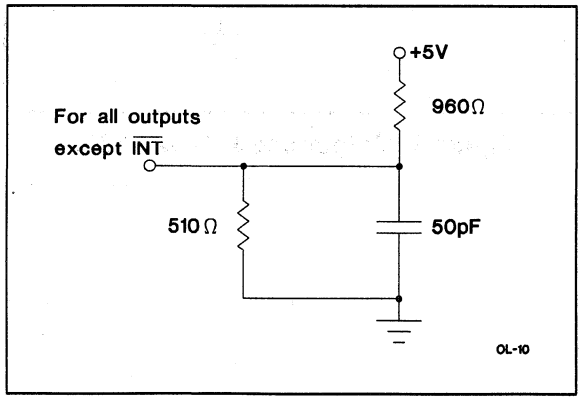

Figure 4. Output Load A—bq3285E

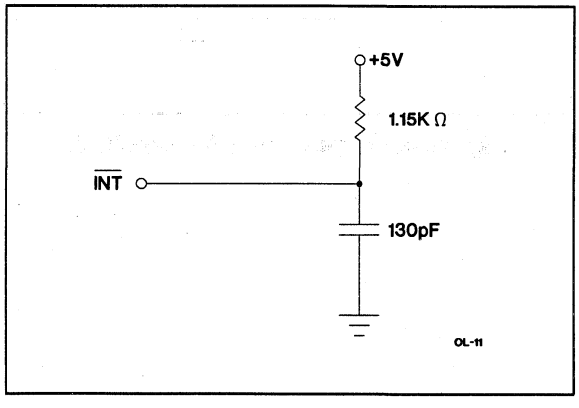

Figure 5. Output Load B—bq3285E

AC Test Conditions—bq3285L

Parameter	Test Conditions
Input pulse levels	0 to 2.3 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.2 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 6 and 7

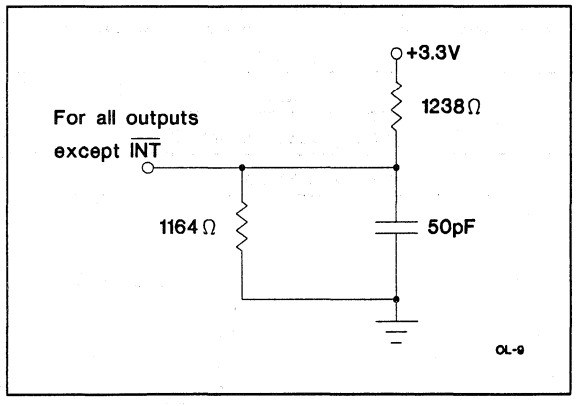

Figure 6. Output Load A—bq3285L

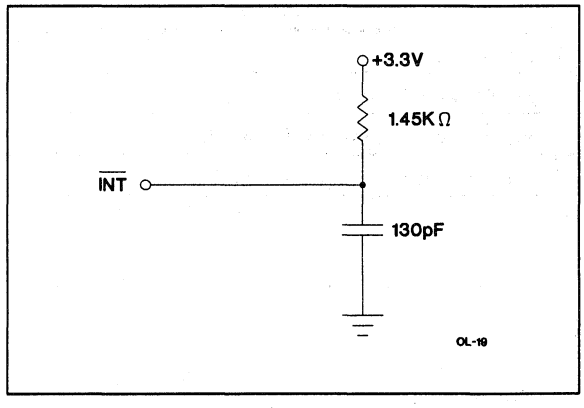

Figure 7. Output Load B—bq3285L

Read/Write Timing—bq3285E ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns	
t_{ASW}	Pulse width, AS high	30	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

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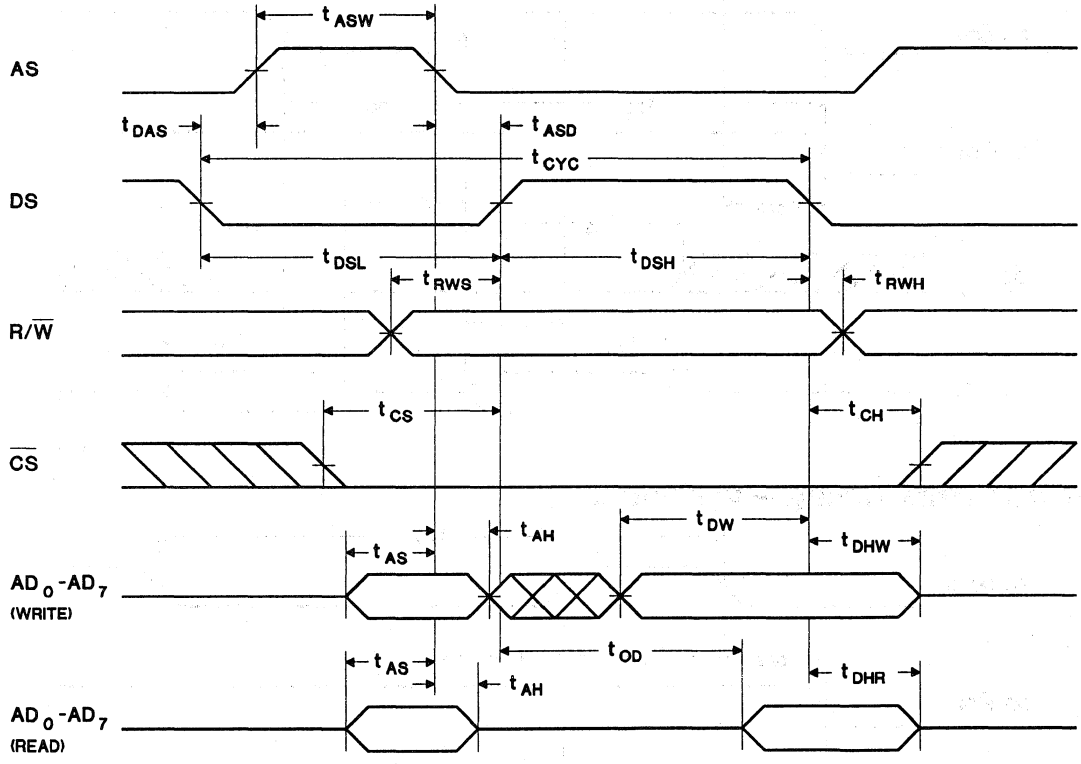
Read/Write Timing—bq3285L (T_A = TOPR, V_{CC} = 3.15V ± 0.45V)

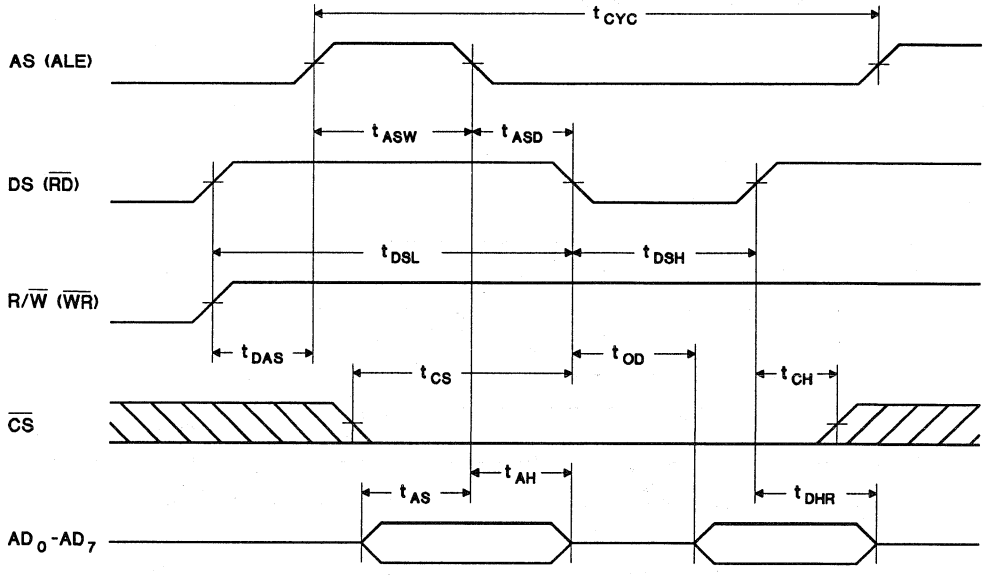
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	270	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	135	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	90	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	15	-	-	ns	
t_{CS}	Chip select setup time	8	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	40	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	30	-	-	ns	
t_{AH}	Address hold time	15	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	15	-	-	ns	
t_{ASW}	Pulse width, AS high	50	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	55	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	100	ns	
t_{DW}	Write data setup time	50	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

Motorola Bus Read/Write Timing—bq3285E/L



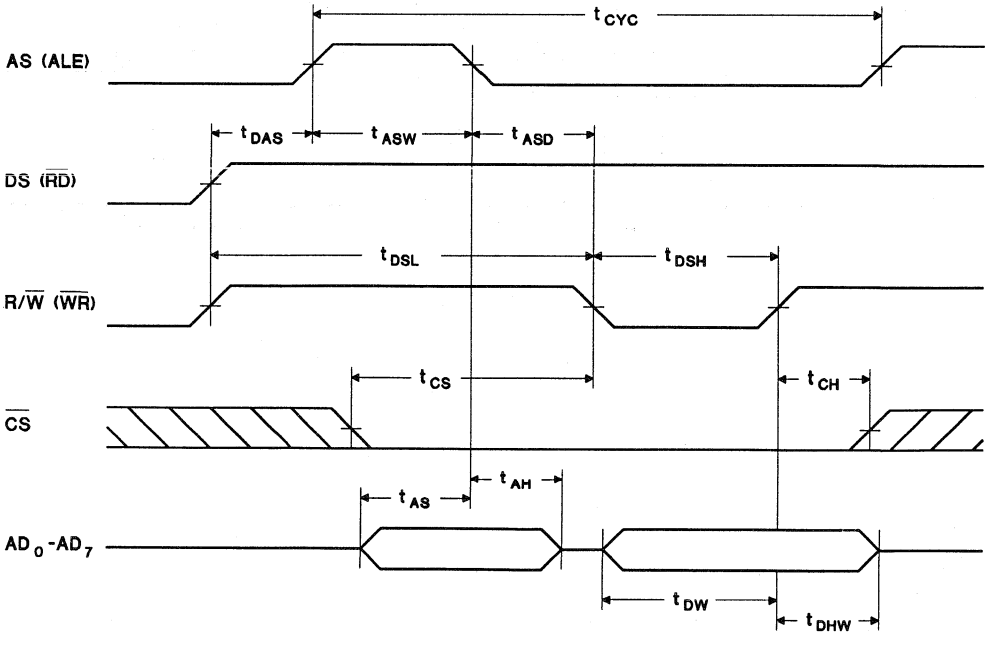
RC-4

Intel Bus Read Timing—bq3285E/L



RC-5

Intel Bus Write Timing—bq3285E/L



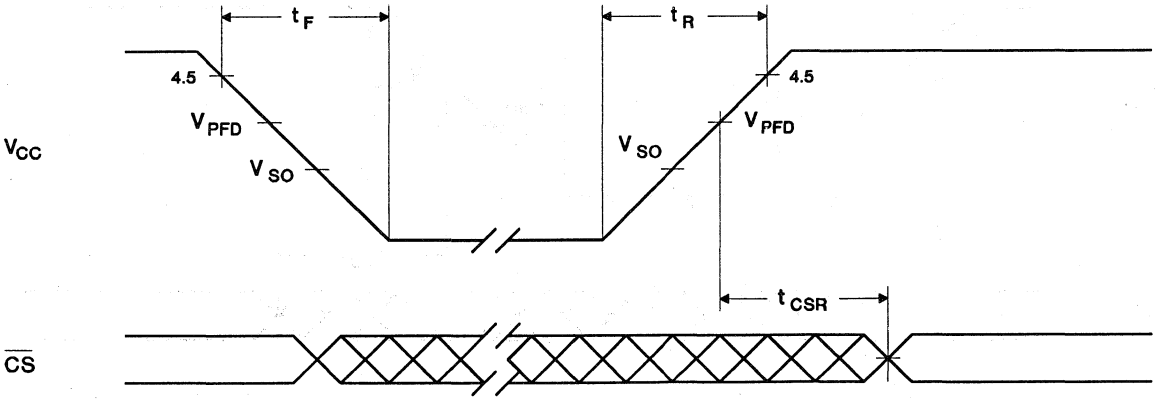
WC-5

Power-Down/Power-Up Timing—bq3285E ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing—bq3285E



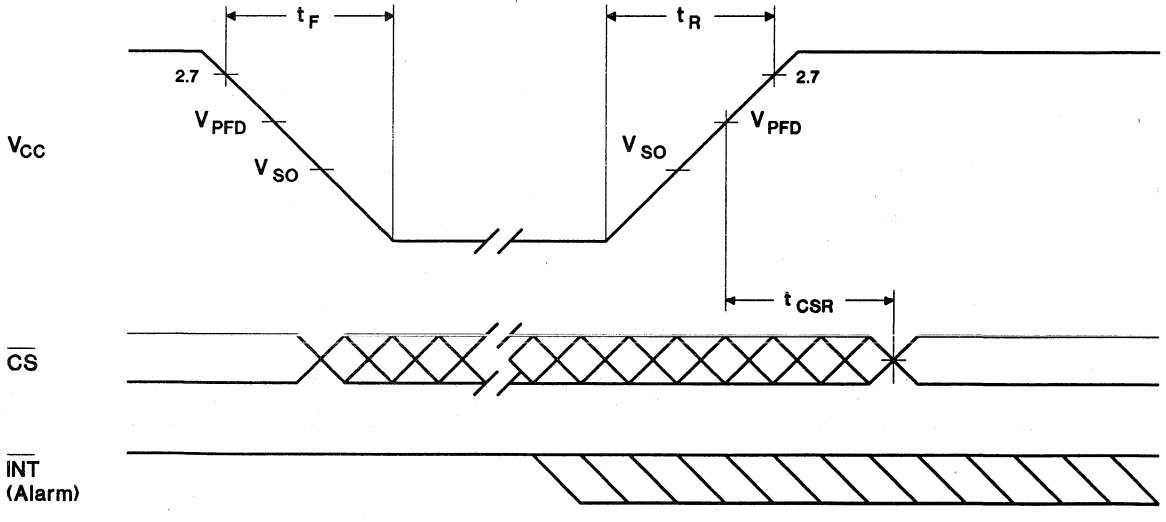
PD-4A

Power-Down/Power-Up Timing—bq3285L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 2.7V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 2.7V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing—bq3285L

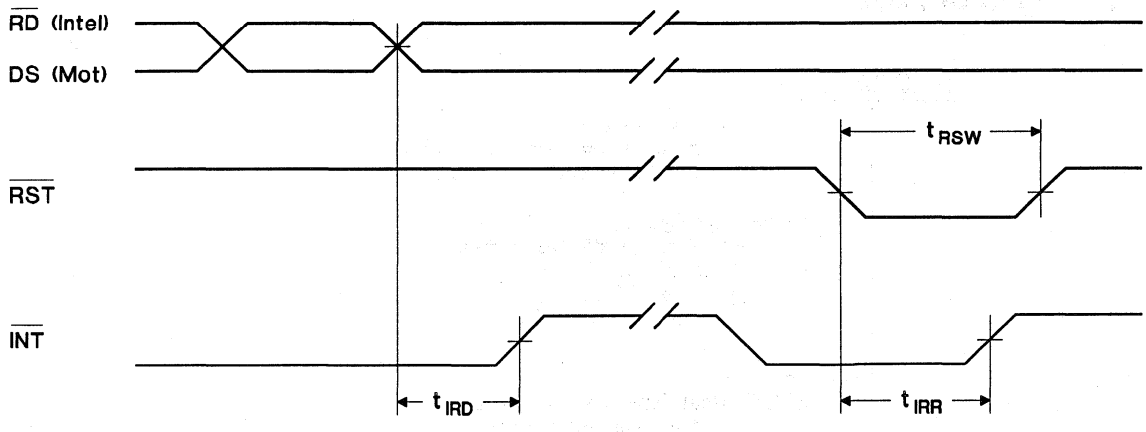


PD-5

Interrupt Delay Timing—bq3285E/L (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS	-	-	2	µs

Interrupt Delay Timing—bq3285E/L



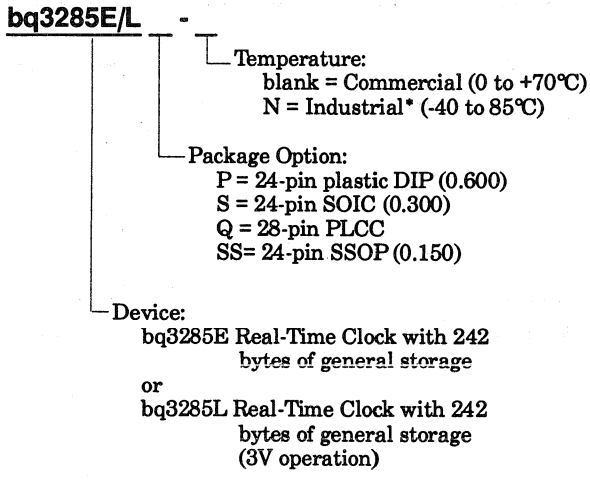
INT-1

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4-26	Register C, bit 2	Was 0; is na (not affected)
1	4-36	Output data delay time t_{OD}	Was 80 ns max; is 100 ns max

Note: Change 1 = Apr. 1994 B "Final" changes from Dec. 1993 A "Preliminary."

Ordering Information



*bq3285E Q package only

BENCHMARQ

bq3287/bq3287A

Real-Time Clock (RTC) Module

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1287/DS1287A and MC146818A
- 114 bytes of general nonvolatile storage
- Integral lithium cell and crystal
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Calendar in day of the week, day of the month, months, and years with automatic leap-year adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

General Description

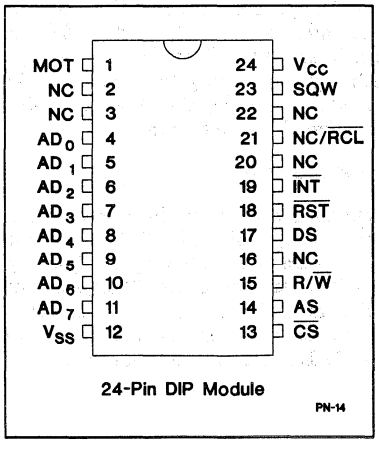
The CMOS bq3287/bq3287A is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square-wave output, and 114 bytes of general nonvolatile storage. The bq3287A version is identical to the bq3287, with the addition of the RAM clear input.

The bq3287 is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The bq3287 write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

As shipped from Benchmarq, the real time clock is turned off to maximize battery capacity for in-system operation.

4

Pin Connections



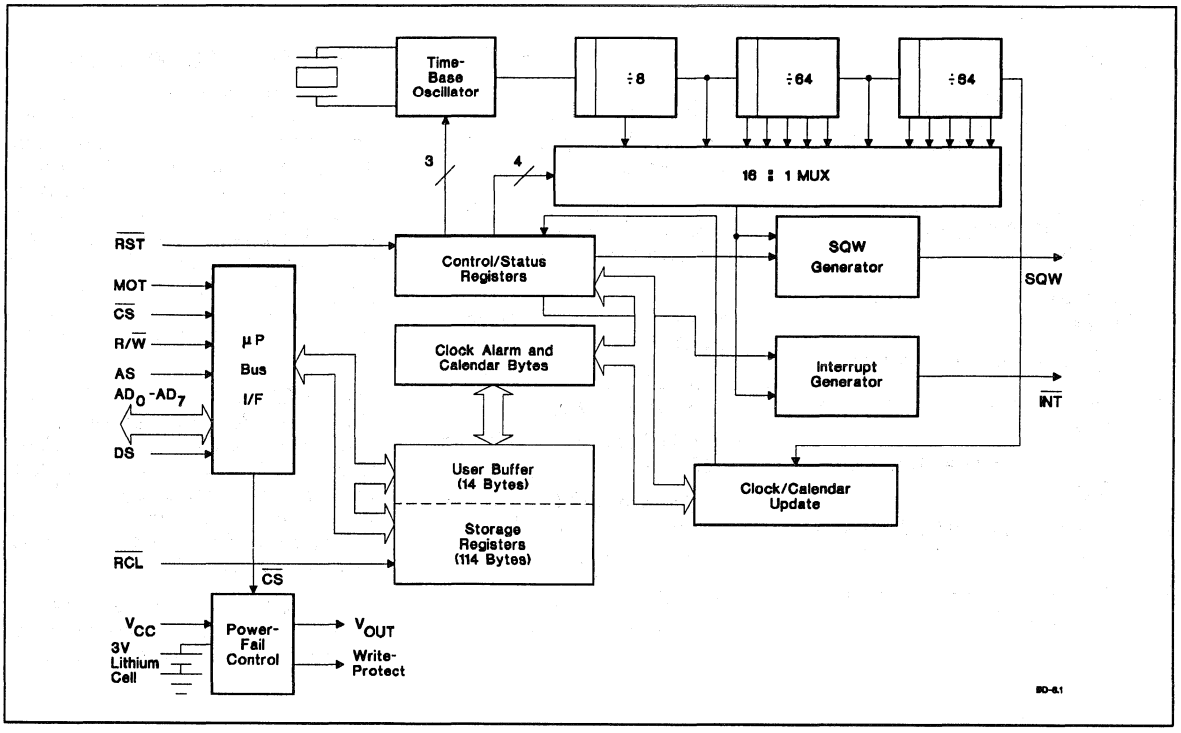
24-Pin DIP Module

PN-14

Pin Names

AD0–AD7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
NC	No connect
$\overline{RCL}$	RAM clear input (bq3287A only)
Vcc	+5V supply
Vss	Ground

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20KΩ resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/output**

The bq3287 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq3287 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins act as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP, SOIC, and PLCC packages with MOT = V_{CC}, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3287 bus cycle. During a read cycle, the bq3287 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3287.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3287.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW **Square-wave output**

SQW may output a programmable frequency square wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

$\overline{RCL}$ **RAM clear input** (bq3287A only)

A low level on the $\overline{RCL}$ pin causes the contents of each of the 114 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ is recognized when held low for at least 125 ms in the presence of V_{CC} when the oscillator is running. Using RAM clear does not affect the battery load. This pin is a no connect on the bq3287.

$\overline{RST}$ **Reset input**

The bq3287 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq3287 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

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Functional Description

The bq3287A differs from the bq3287 only by the presence of $\overline{RCL}$ on pin 21. Otherwise, the two devices are identical.

Address Map

The bq3287 provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3287.

Update Period

The update period for the bq3287 is one second. The bq3287 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3287 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes is frozen, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

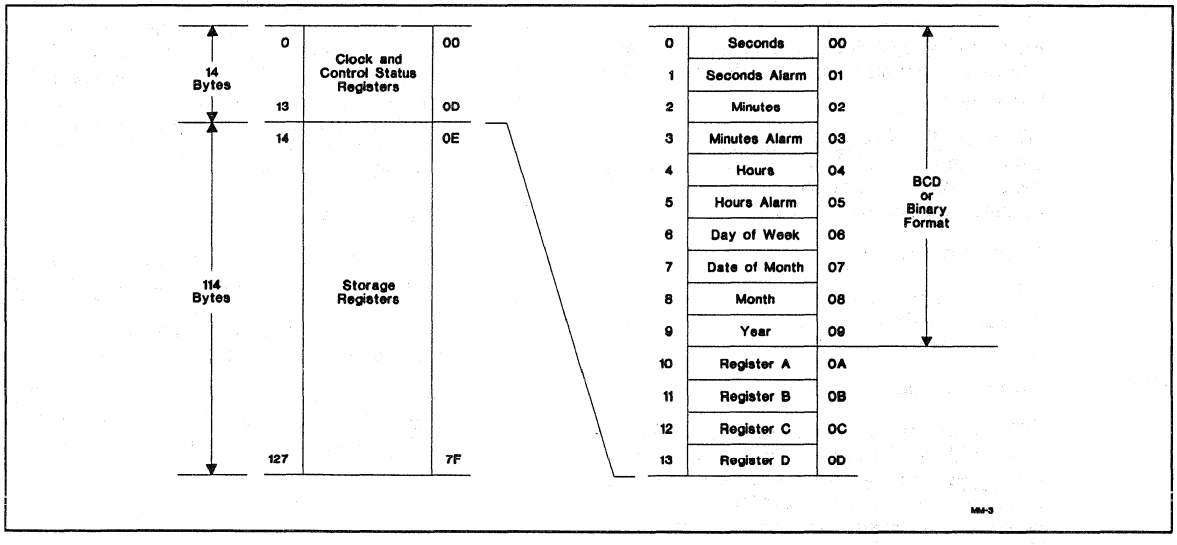

Figure 1. Address Map

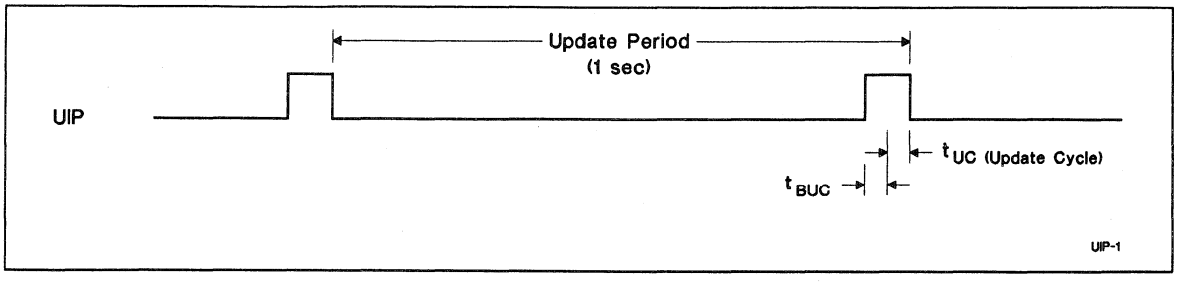

Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format bit (DF) to select BCD or binary format for all clock and calendar bytes.
   c. Write the appropriate value to the hour format bit (HR).
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

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Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq3287 divides the 32.768kHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B.

Interrupts

The bq3287 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of an RTC update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3287 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	4.096	kHz	244.141	µs
0	1	0	1	2.048	kHz	488.281	µs
0	1	1	0	1.024	kHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122μs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3).

Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar readings during an update cycle may be in error. Three methods to access the RTC bytes without ambiguity are available:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler finishes accessing the clock bytes in $t_{PI}/2$ + t_{BUC} time (see Figure 3).

Oscillator Control

The bq3287 is shipped from Benchmarq with its internal oscillator turned off. The internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

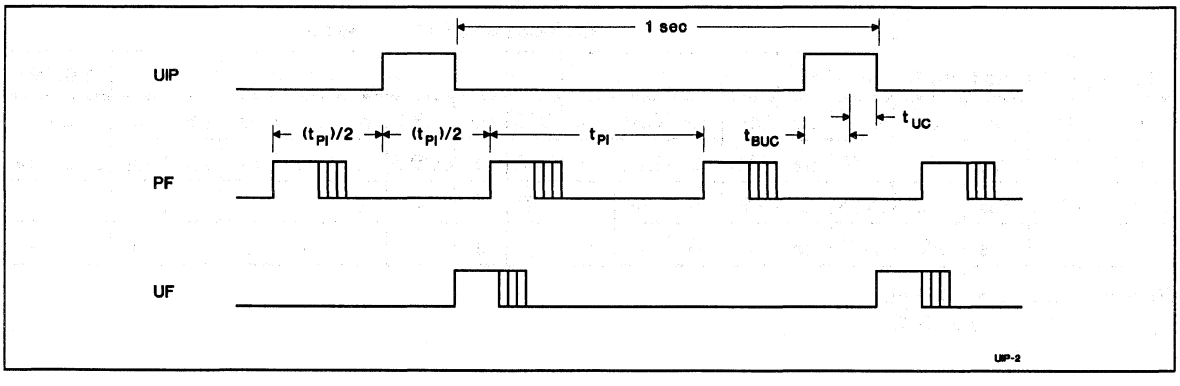


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3287 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3287 write-protects the clock and storage registers. When V_{CC} is below V_{SO} (3V typical), the power source is switched to the internal lithium cell. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{SO}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3287 are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. The bq3287 is shipped from Benchmarq with its oscillator turned off. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.
1. Except bit 7.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3287 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update-Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-20 to +70	°C	Extended "I"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +70	°C	Extended "I"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-20 to +70	°C	Extended "I"
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

4

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	3.0	-	V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL} = V_{SS}$	-	-	275	µA	Internal 20K pull-up (bq3287A only)
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-275	µA	Internal 20K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

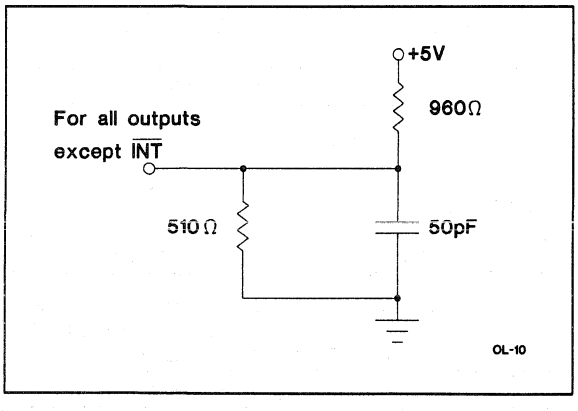


Figure 4. Output Load A

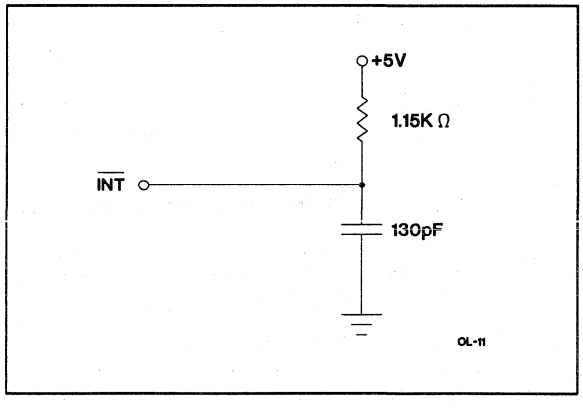


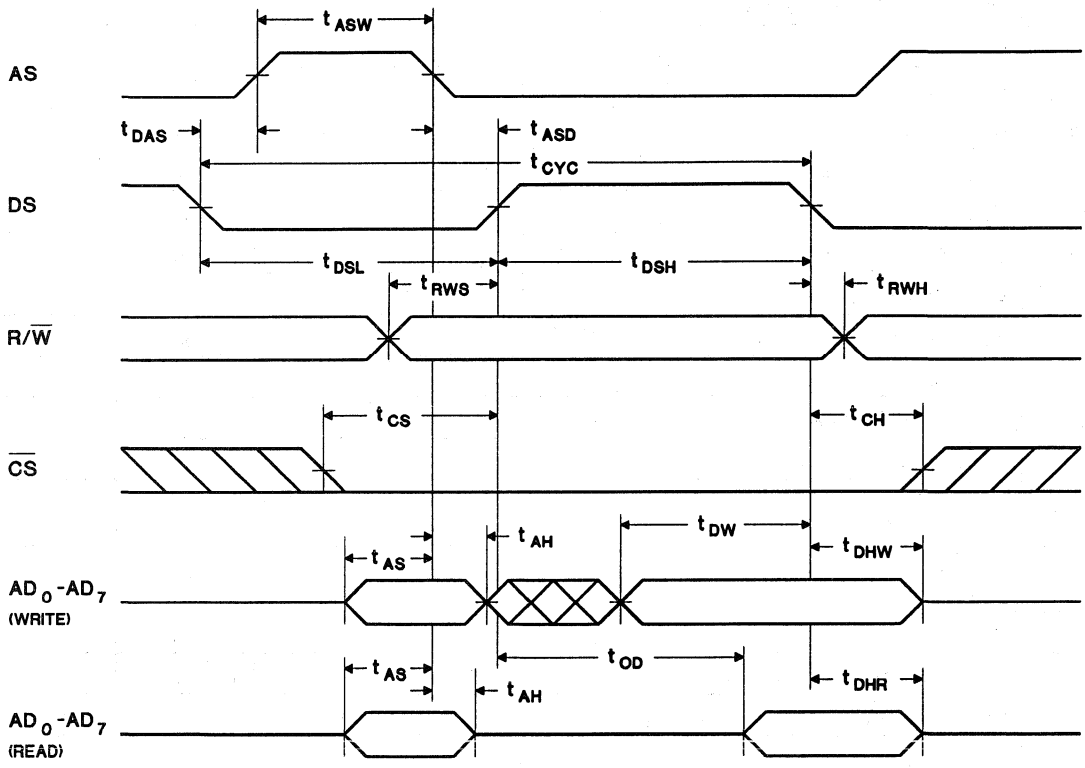
Figure 5. Output Load B

Read/Write Timing (TA = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns	
t_{ASW}	Pulse width, AS high	30	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

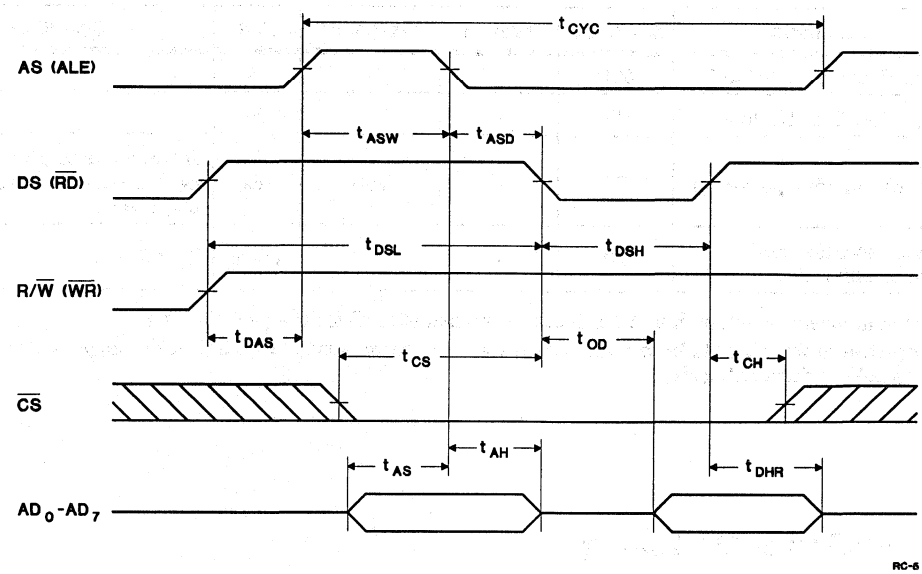
4

Motorola Bus Read/Write Timing

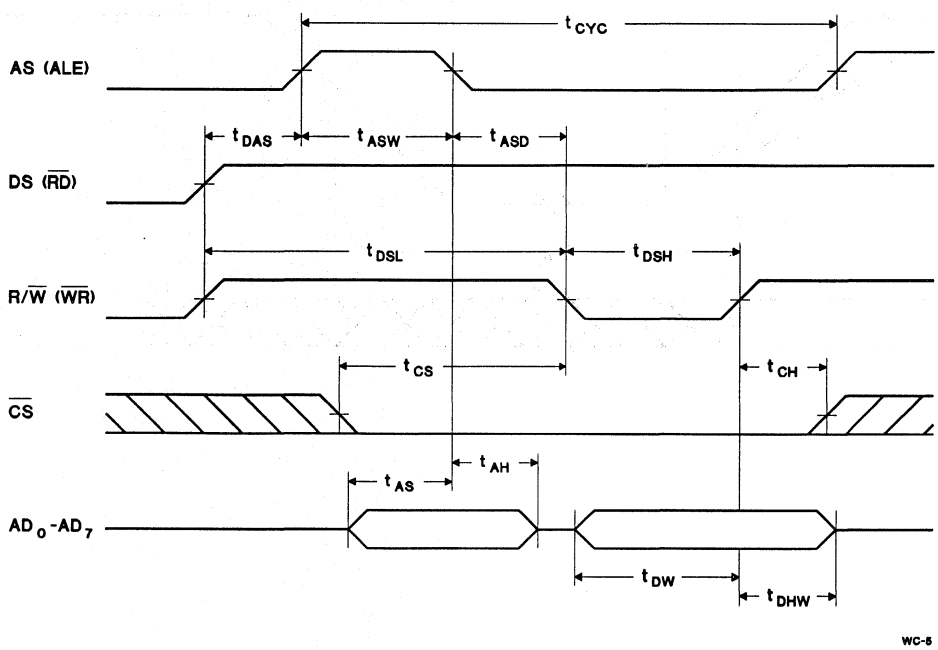


RC-4

Intel Bus Read Timing



Intel Bus Write Timing



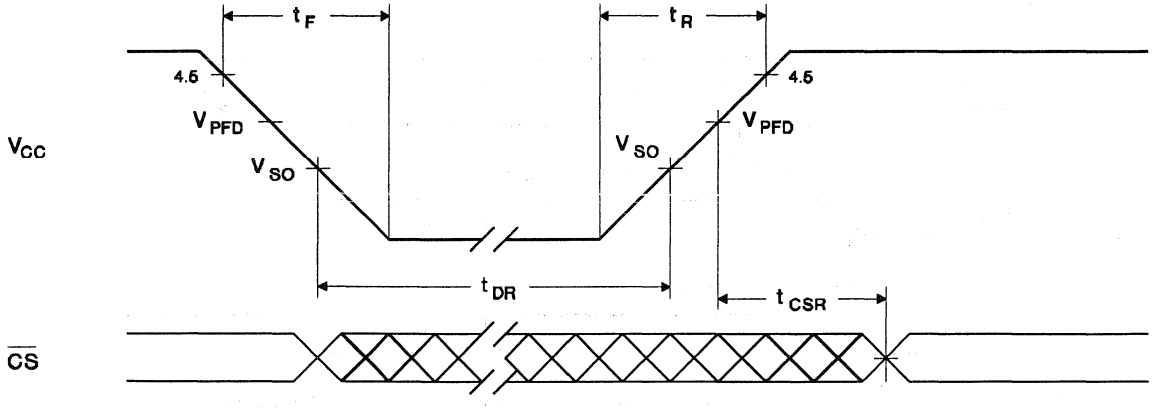
Power-Down/Power-Up Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10	-	-	years	T_A = 25°C.

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing

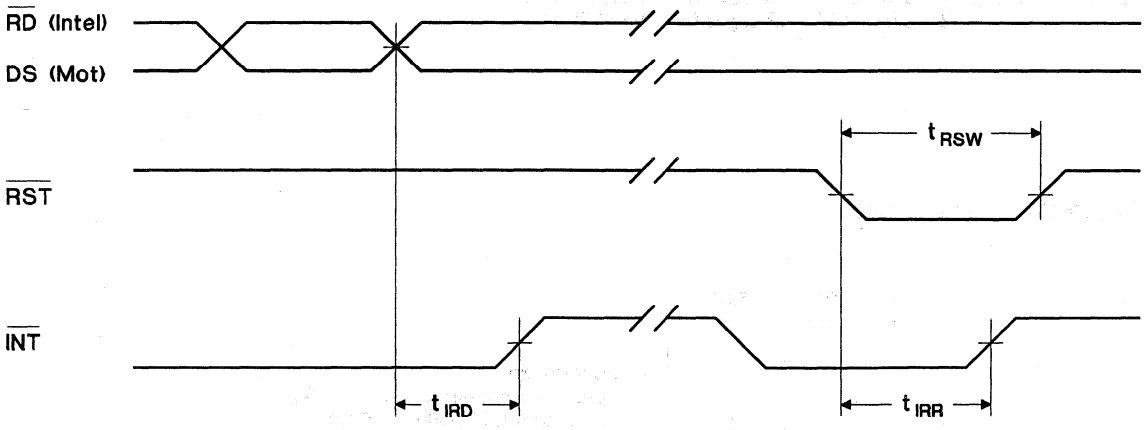


PD-4

Interrupt Delay Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)	-	-	2	µs

Interrupt Delay Timing



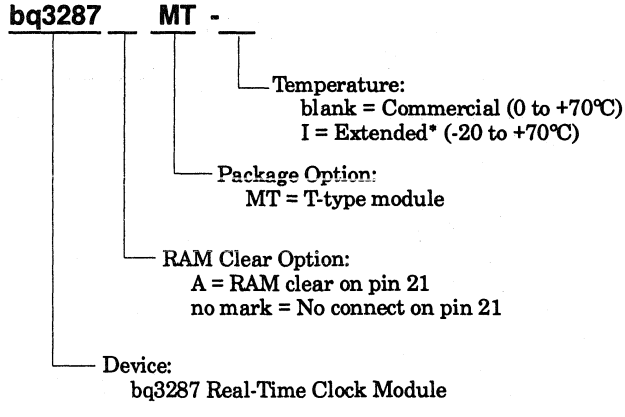
INT-1

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4-42	Address strobe input	Clarification
1	4-53	Power-fail detect voltage V_{PFD}	Was 4.1 min, 4.25 max; is 4.0 min, 4.35 max
2	4-41	Was : "As shipped from Benchmarq, the backup cell is electrically isolated from the memory." Is: "As shipped from Benchmarq, the backup cell is electrically isolated from the active circuitry."	Clarification
2	4-53, 4-60	Changed temperature from N (industrial, -40 to +85°C) to I (extended, -20 to +70°C)	Specification change

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.

Ordering Information



*Contact factory for availability.

bq3287E/bq3287EA

Real-Time Clock (RTC) Module

Features

- System wake-up capability—alarm interrupt active in battery-backup mode
- 242 bytes of general nonvolatile storage
- Provides a 32.768kHz output for power management
- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1287/DS1287A and MC146818A/MC146818B
- Integral lithium cell and crystal
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Calendar in day of the week, day of the month, months, and years with automatic leap-year adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

General Description

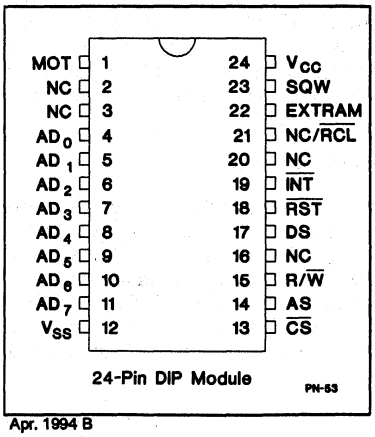
The CMOS bq3287E/bq3287EA is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square-wave output, and 242 bytes of general nonvolatile storage. A 32.768kHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode. The bq3287EA version is identical to the bq3287E, with the addition of the RAM clear input.

The bq3287E is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The bq3287E write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

As shipped from Benchmarq, the real time clock is turned off to maximize battery capacity for in-system operation.

4

Pin Connections



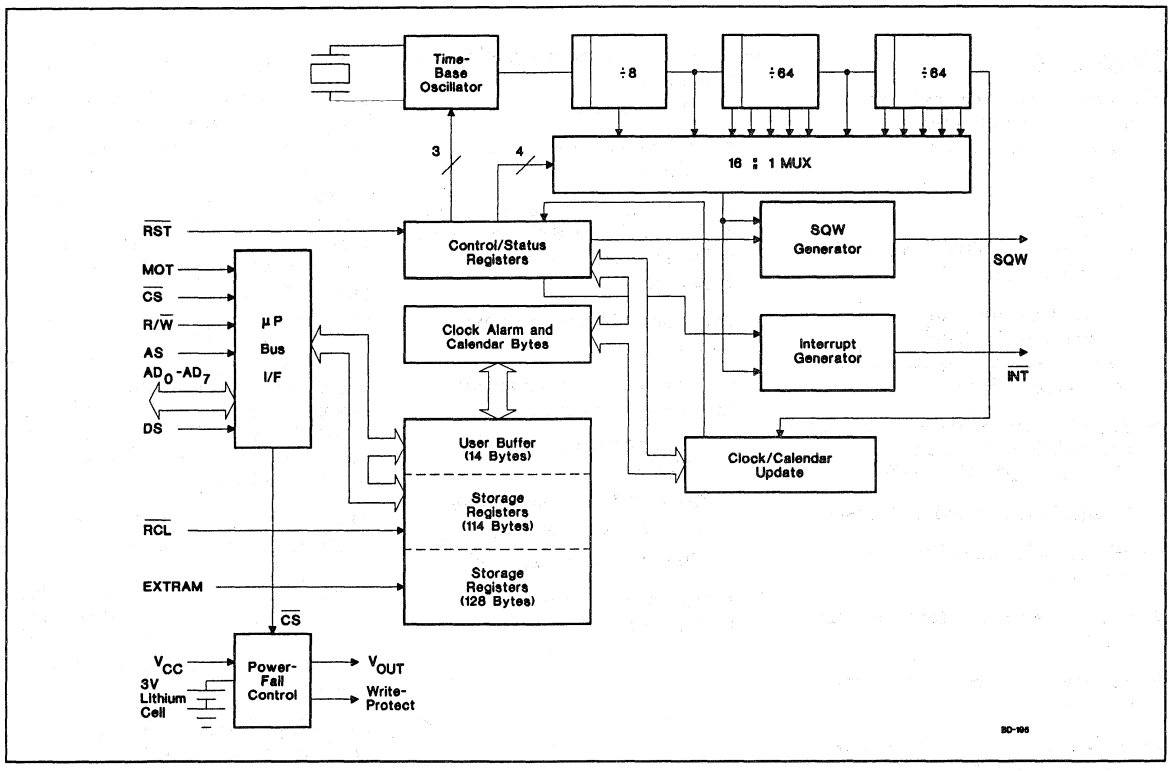
24-Pin DIP Module

PN-63

Pin Names

AD0–AD7	Multiplexed address/data input/output
MOT	Bus type select input
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
EXTRAM	Extended RAM enable
NC	No connect
$\overline{RCL}$	RAM clear input (bq3287EA only)
Vcc	+5V supply
Vss	Ground

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20KΩ resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/output**

The bq3287E bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 and EXTRAM is latched into the bq3287E on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins act as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7 and EXTRAM. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP, SOIC, and PLCC packages with MOT = V_{SS}, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3287E bus cycle. During a read cycle, the bq3287E drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3287E.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3287E.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. This allows alarm $\overline{INT}$ to be valid in battery-backup mode. To use this feature, $\overline{INT}$ must be connected to a power supply other than V_{CC}. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

EXTRAM **Extended RAM enable**

Enables 128 bytes of additional nonvolatile SRAM. It is connected internally to a 30KΩ pull-down resistor. To access the RTC registers, EXTRAM must be low.

SQW **Square-wave output**

SQW may output a programmable frequency square wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

A 32.768kHz output is enabled by setting the SQWE bit in register B to 1 and the 32KE bit in register C to 1 after setting OSC2–OSC0 to 011 (binary).

$\overline{RCL}$ **RAM clear input** (bq3287EA only)

A low level on the $\overline{RCL}$ pin causes the contents of each of the 242 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ is recognized when held low for at least 125 ms in the presence of V_{CC}. Using RAM clear does not affect the battery load. This pin is a no connect on the bq3287E.

$\overline{RST}$ **Reset input**

The bq3287E is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq3287E is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

4

Functional Description

The bq3287EA differs from the bq3287E only by the presence of $\overline{RCL}$ on pin 21. Otherwise, the two devices are identical.

Address Map

The bq3287E provides 14 bytes of clock and control/status registers and 242 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3287E.

Update Period

The update period for the bq3287E is one second. The bq3287E updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3287E copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes is frozen, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

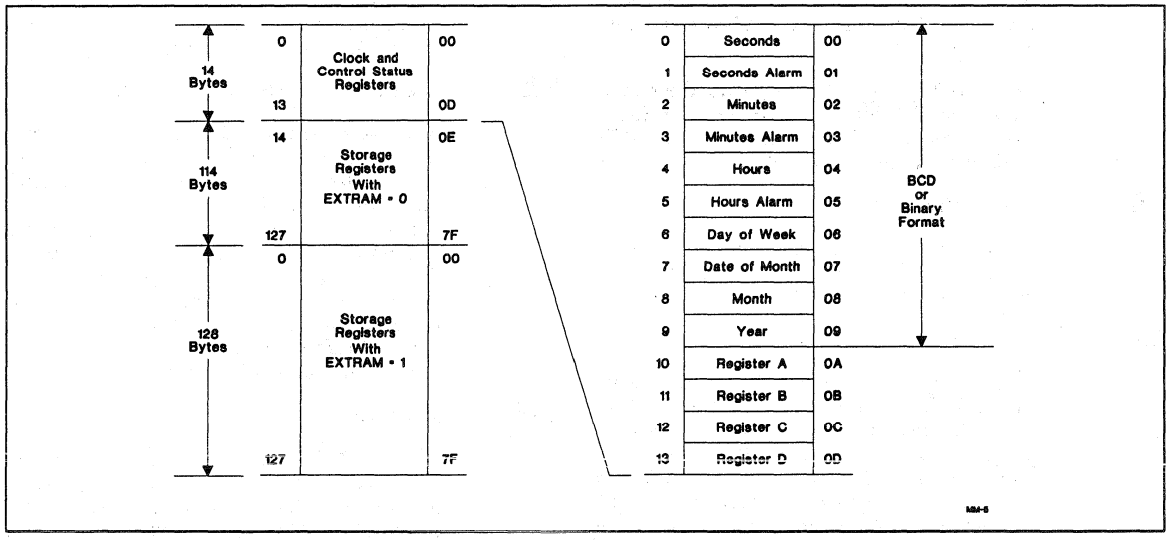


Figure 1. Address Map

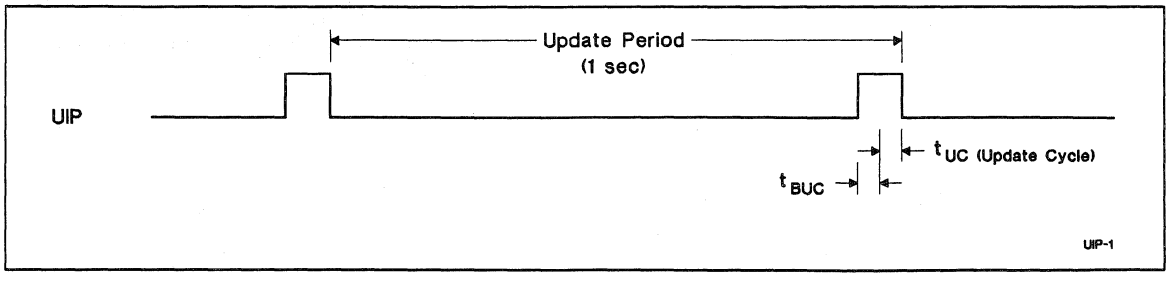


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format bit (DF) to select BCD or binary format for all clock and calendar bytes.
   c. Write the appropriate value to the hour format bit (HR).
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

4

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq3287E divides the 32.768 kHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B. A 32.768kHz output may be selected by setting OSC2–OSC0 in register A to 011 while SQWE = 1 and 32KE = 1.

Interrupts

The bq3287E allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a "wake-up" feature.
- The update-ended interrupt, which occurs at the end of an RTC update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq3287E interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits							Square Wave		Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	1	0	0	0	0	0	None		None	
0	1	0	0	0	0	1	256	Hz	3.90625	ms
0	1	0	0	0	1	0	128	Hz	7.8125	ms
0	1	0	0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	1	0	0	4.096	kHz	244.141	µs
0	1	0	0	1	0	1	2.048	kHz	488.281	µs
0	1	0	0	1	1	0	1.024	kHz	976.5625	µs
0	1	0	0	1	1	1	512	Hz	1.953125	ms
0	1	0	1	0	0	0	256	Hz	3.90625	ms
0	1	0	1	0	0	1	128	Hz	7.8125	ms
0	1	0	1	0	1	0	64	Hz	15.625	ms
0	1	0	1	0	1	1	32	Hz	31.25	ms
0	1	0	1	1	0	0	16	Hz	62.5	ms
0	1	0	1	1	0	1	8	Hz	125	ms
0	1	0	1	1	1	0	4	Hz	250	ms
0	1	0	1	1	1	1	2	Hz	500	ms
0	1	1	X	X	X	X	32.768	kHz	same as above defined by RS3–RS0	

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3). Setting OSC2–OSC0 in register A to 011 does not affect the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt is active in battery-backup mode, providing a "wake-up" capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

The EXTRAM pin must be low to access the RTC registers. Time and calendar readings during an update cycle may be in error. Three methods to access the RTC bytes without ambiguity are available:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler finishes accessing the clock bytes in $t_{PI}/2 + t_{BUC}$ time (see Figure 3).

Oscillator Control

The bq3287E is shipped from Benchmarq with its internal oscillator turned off. The internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz

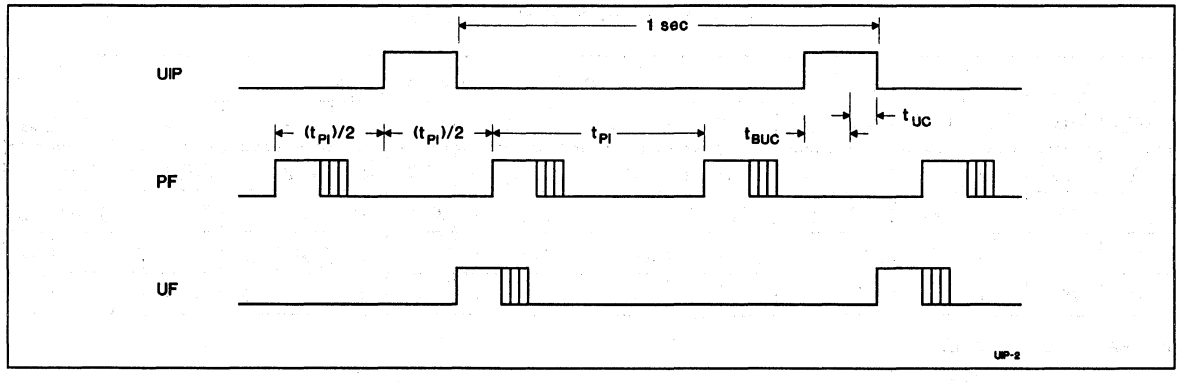


Figure 3. Update-Ended/Periodic Interrupt Relationship

wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

Power-Down/Power-Up Cycle

The bq3287E continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3287E write-protects the clock and storage registers. When V_{CC} is below V_{SO} (3V typical), the power source is switched to the internal lithium cell. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{SO}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3287E are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. The bq3287E is shipped from Benchmarq with its oscillator turned off. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset													
				7 (MSB)		6		5		4		3		2		1	0 (LSB)
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.
2. Read/write only when OSC2–OSC0 is 011 (binary).

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3287E increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0, 1, 3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	-	0	0

These bits are always set to 0.

32KE - 32kHz Enable Output

7	6	5	4	3	2	1	0
-	-	-	-	-	32KE	-	-

This bit may be set to a 1 only when the OSC2–OSC0 bits in register A are set to 011. Setting OSC2–OSC0 to anything other than 011 clears this bit. If SQWE in register B and 32KE are set, a 32.768kHz waveform is output on the square wave pin.

UF - Update-Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	$V_{CC} + 0.3$	V

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4	-	-	V	$I_{OH} = -1.0$ mA
V_{OL}	Output low voltage	-	-	0.4	V	$I_{OL} = 4.0$ mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	3.0	-	V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL} = V_{SS}$	-	-	275	µA	Internal 20K pull-up (bq3287EA only)
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-185	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = V_{CC}	-	-	-75	µA	Internal 30K pull-down

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

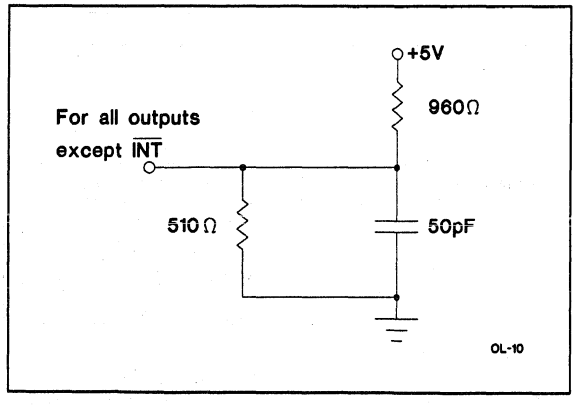


Figure 4. Output Load A

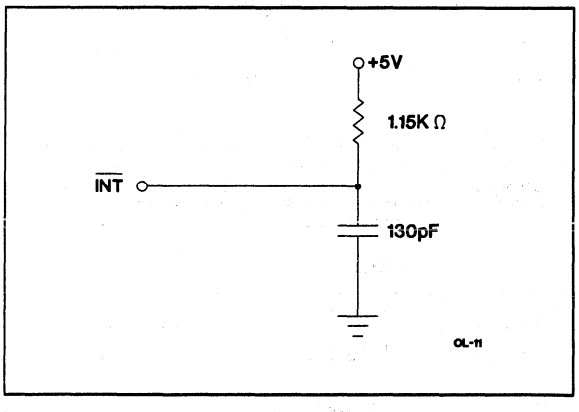


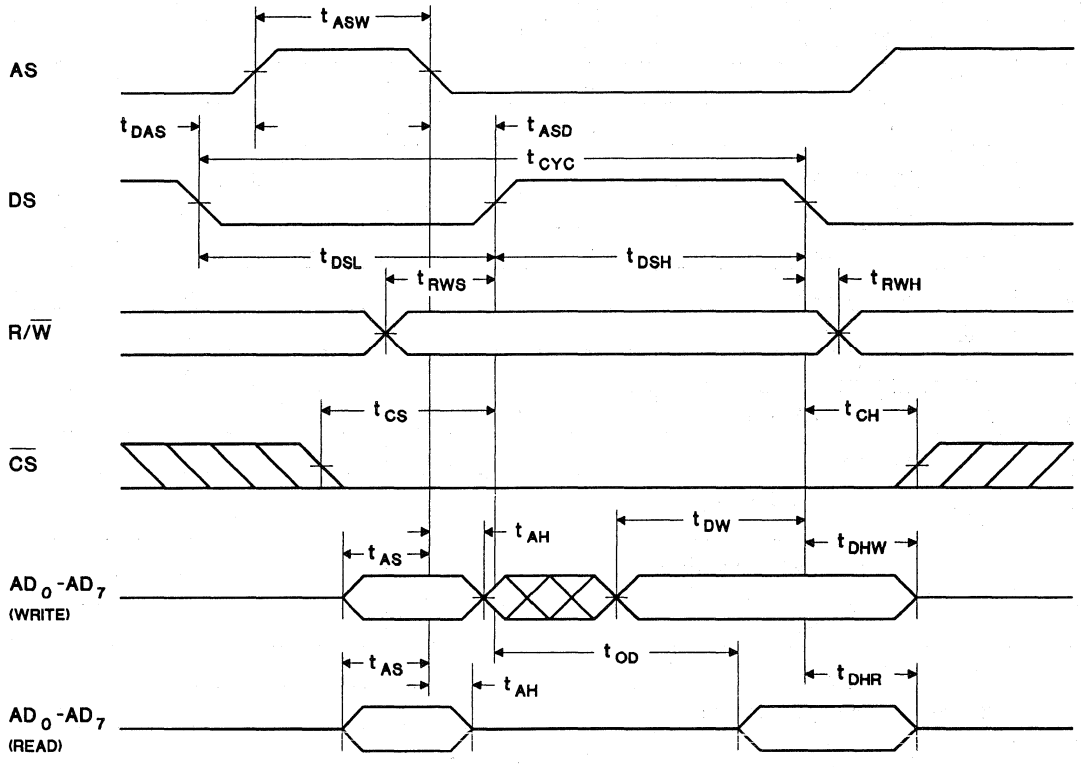
Figure 5. Output Load B

Read/Write Timing (TA = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns	
t_{ASW}	Pulse width, AS high	30	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

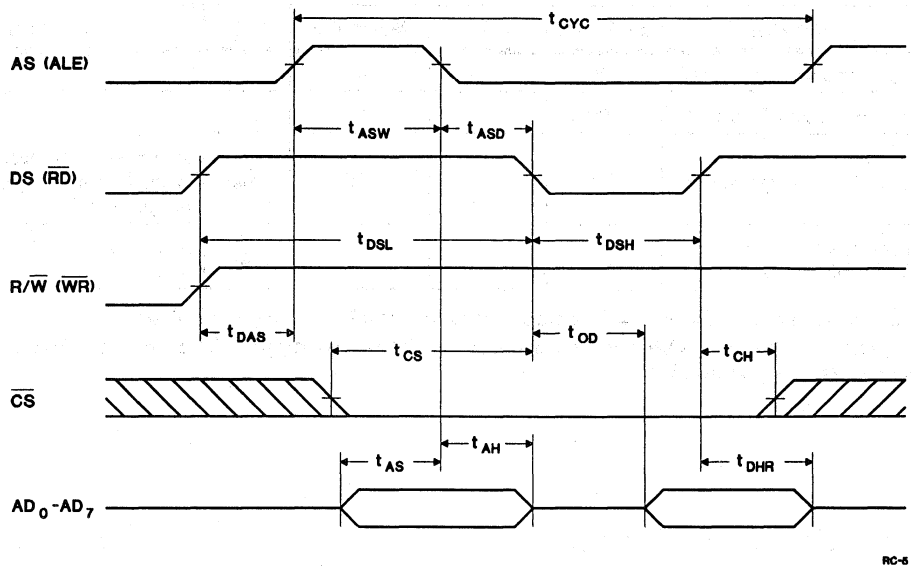
4

Motorola Bus Read/Write Timing



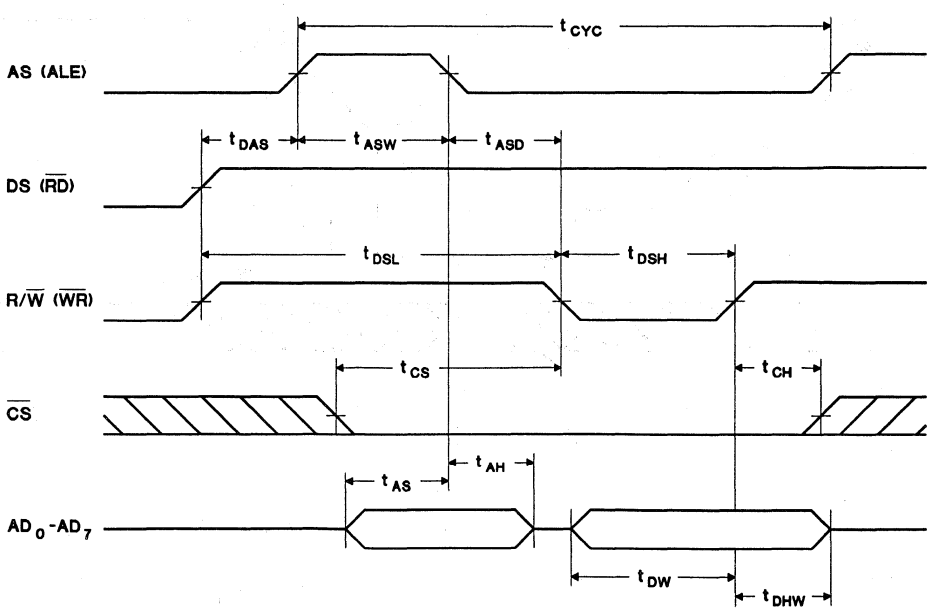
RC-4

Intel Bus Read Timing



RC-5

Intel Bus Write Timing



WC-5

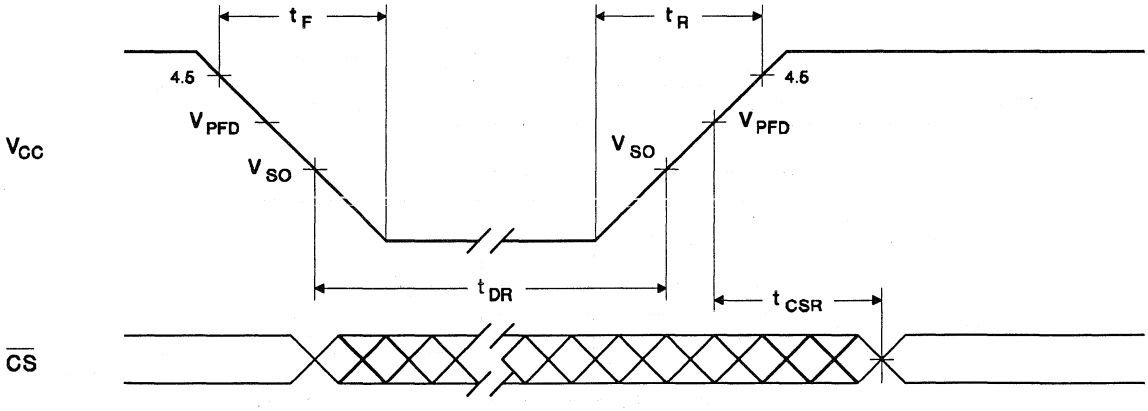
Power-Down/Power-Up Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10	-	-	years	T_A = 25°C.

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing

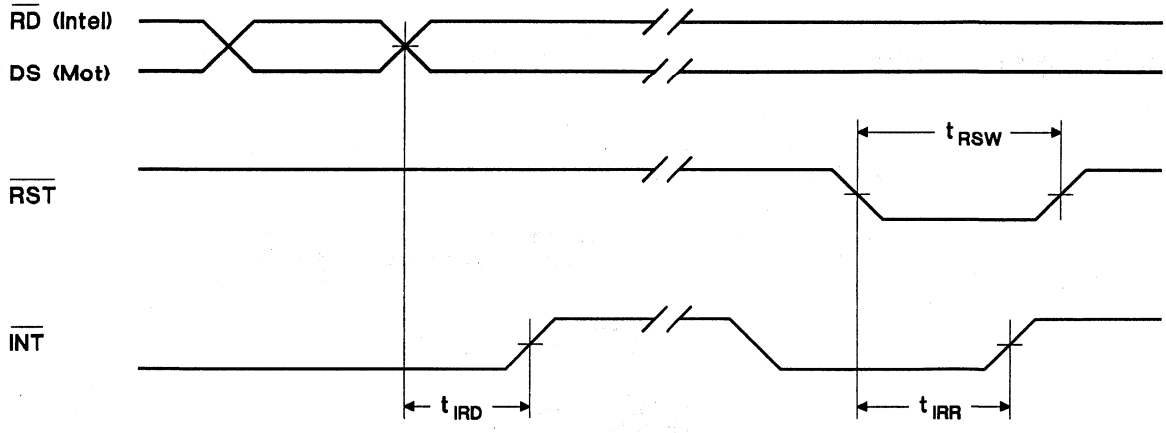


PD-4

Interrupt Delay Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)	-	-	2	µs

Interrupt Delay Timing



INT-1

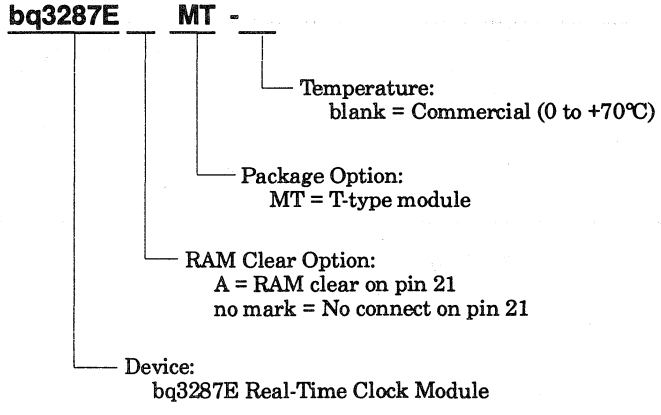
4

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4-68	Register C, bit 2	Was 0; is na (not affected)

Note: Change 1 = Apr. 1994 B "Final" changes from Dec. 1993 A "Preliminary."

Ordering Information



BENCHMARQ

bq4285

Real-Time Clock (RTC) With NVRAM Control

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 114 bytes of general nonvolatile storage
- Automatic backup and write-protect control to external SRAM
- 160 ns cycle time allows fast bus operation
- Selectable Intel or Motorola bus timing (PLCC), Intel bus timing (DIP and SOIC)
- Less than 0.5 µA load under battery operation
- 14 bytes for clock/calendar and control
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- BCD or binary format for clock and calendar data
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

The CMOS bq4285 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

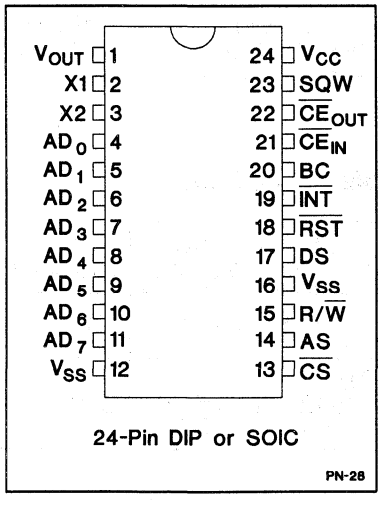
The bq4285 write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq4285 is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

The bq4285 integrates a battery-backup controller to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4285 automatically write-protects the external SRAM and provides a V_{CC} output sourced from the clock backup battery.

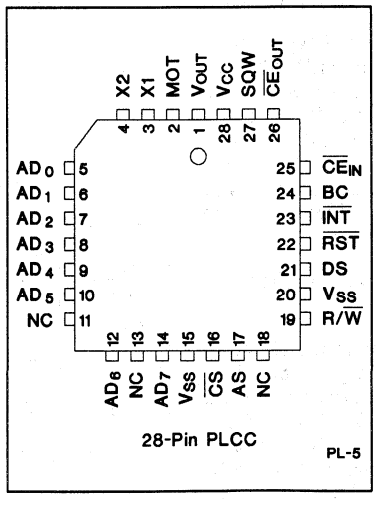
4

Pin Connections



24-Pin DIP or SOIC

PN-28

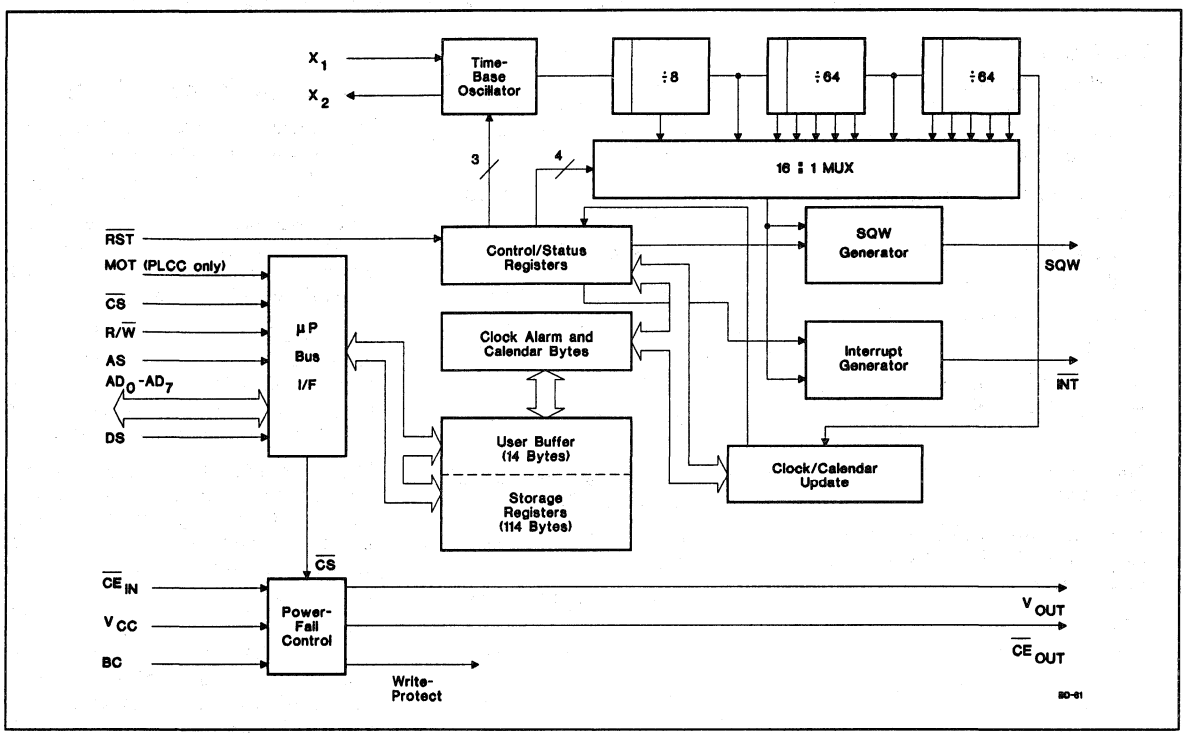


28-Pin PLCC

PL-5

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
MOT	Bus type select input (PLCC only)
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
BC	3V backup cell input
X1, X2	Crystal inputs
NC	No connect
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
V_{OUT}	Supply output
V_{CC}	+5V supply
V_{SS}	Ground



Block Diagram

Pin Descriptions

AD0–AD7 **Multiplexed address/data input/output**

The bq4285 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD0–AD7 is latched into the bq4285 on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD0–AD7 pins serve as a bidirectional data bus.

MOT **Bus type select input (PLCC package only)**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to VCC for Motorola timing or to VSS for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20KΩ resistor. For the DIP and SOIC packages, this pin is internally connected to VSS, enabling the bus timing for the Intel architecture.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq4285.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	VCC	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	VSS	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD0–AD7. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP, SOIC, and PLCC packages with MOT = VCC, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

For DIP, SOIC, and PLCC packages with MOT = VSS, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

For the PLCC package, when MOT = VCC, DS controls data transfer during a bq4285 bus cycle. During a read cycle, the bq4285 drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

R/$\overline{W}$ **Read/write input**

For DIP, SOIC, and PLCC packages with MOT = VSS, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq4285.

For the PLCC package, when MOT = VCC, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

$\overline{RST}$ **Reset input**

The bq4285 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq4285 is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to VCC. This allows the control bits to retain their states through power-down/power-up cycles.

SQW **Square-wave output**

SQW may output a programmable frequency square-wave signal during normal (VCC valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of power. When VCC slows down past VBC (3V typical), the integral control circuitry switches the power source to BC. When VCC returns above VBC, the power source is switched to VCC.

X1, X2 **Crystal input**

The X1, X2 inputs are provided for an external 32.768Khz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

$\overline{CE}_{IN}$ **External RAM chip enable input, active low**

$\overline{CE}_{IN}$ should be driven low to enable the controlled external RAM. $\overline{CE}_{IN}$ is internally pulled up with a 50KΩ resistor.

$\overline{CE}_{OUT}$ **External RAM chip enable output, active low**

When power is valid, $\overline{CE}_{OUT}$ reflects $\overline{CE}_{IN}$.

VOUT **Supply output**

VOUT provides the higher of VCC or VBC, switched internally, to supply external RAM.

VCC **+5V supply**

VSS **Ground**

Functional Description

Address Map

The bq4285 provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq4285.

Update Period

The update period for the bq4285 is one second. The bq4285 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq4285 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

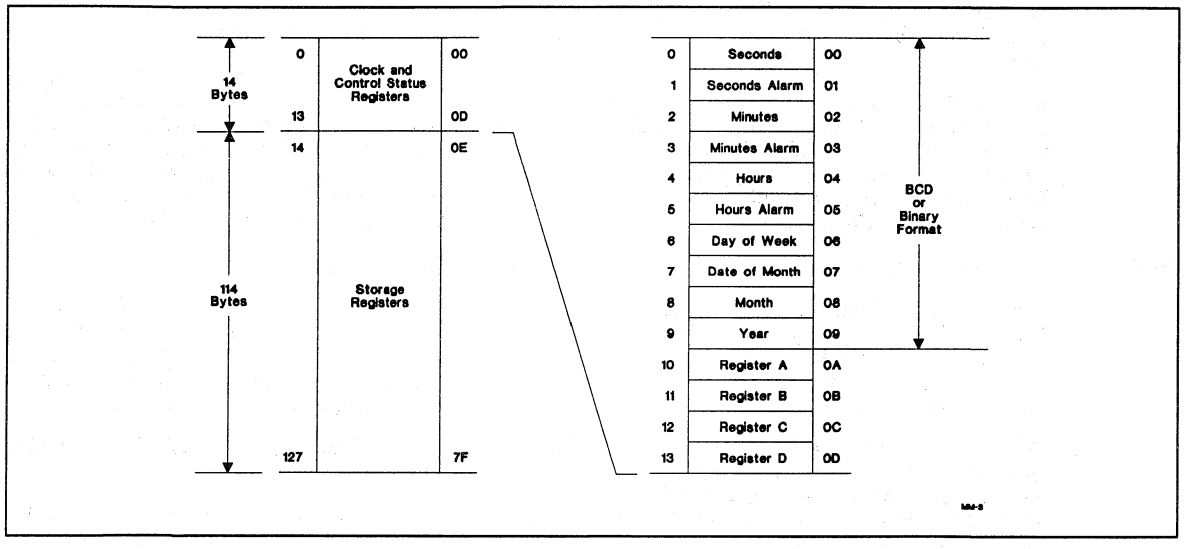


Figure 1. Address Map

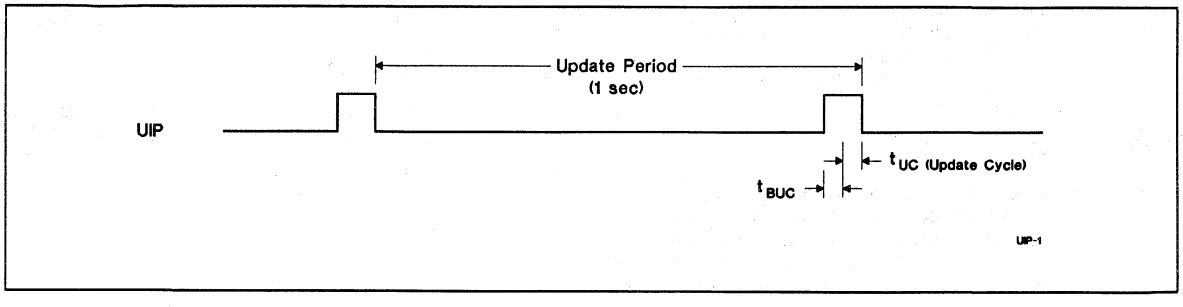


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

4

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square Wave Output

The bq4285 divides the 32.768kHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B.

Interrupts

The bq4285 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of each update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq4285 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	4.096	kHz	244.141	µs
0	1	0	1	2.048	kHz	488.281	µs
0	1	1	0	1.024	kHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122μs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3).

Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler will have a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq4285 and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

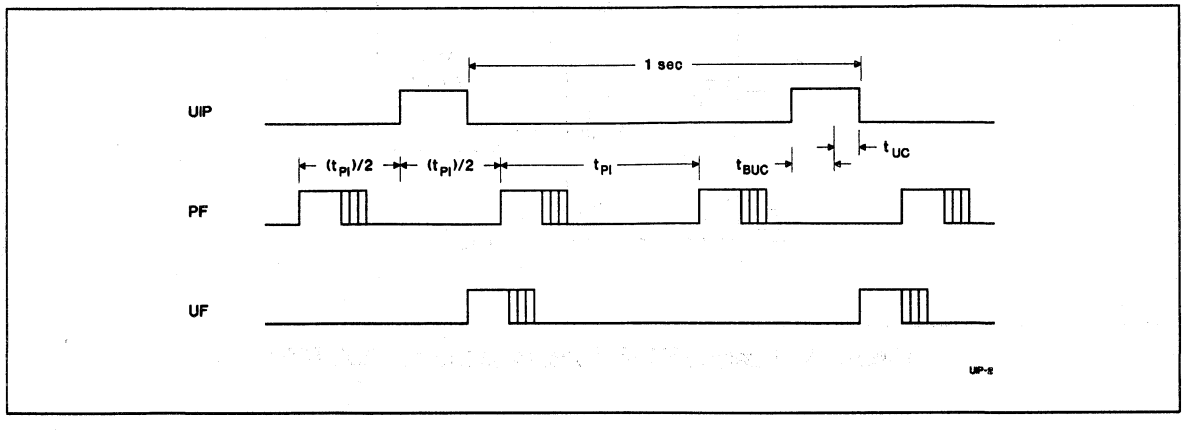


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq4285 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq4285 write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4285. As the voltage input V_{CC} slows down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in process to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (30µs maximum), the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. $\overline{CE}_{OUT}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 10ns.

Figure 4 shows the hardware hookup for the external RAM.

A primary backup energy source input is provided on the bq4285. The BC input accepts a 3V primary battery, typically some type of lithium chemistry. To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{OUT}$ are internally isolated from BC by the initial connection of a battery. Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM.

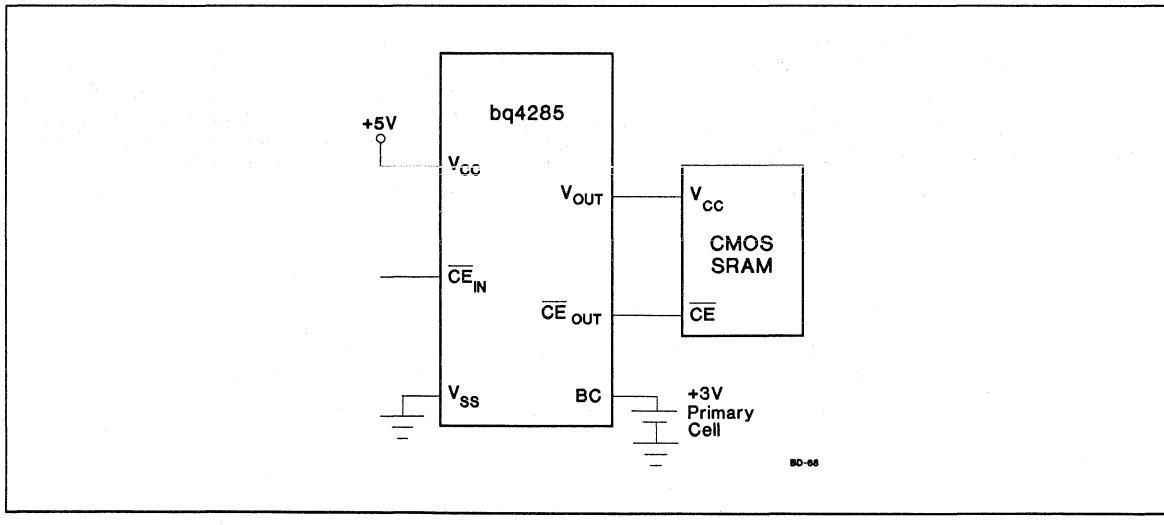


Figure 4. External RAM Hookup to the bq4285 RTC

Control/Status Registers

The four control/status registers of the bq4285 are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.
1. Except bit 7.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq4285 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.5	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = Vss to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, V_{OUT} = Vss to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 100mA, V_{CC} > V_{BC}
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V				I_{OUT} = 100µA, V_{CC} < V_{BC}
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-275	µA	Internal 20K pull-down
$I_{\overline{CE}}$	Chip enable input current	-	-	100	µA	Internal 50K pull-up

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 5 and 6

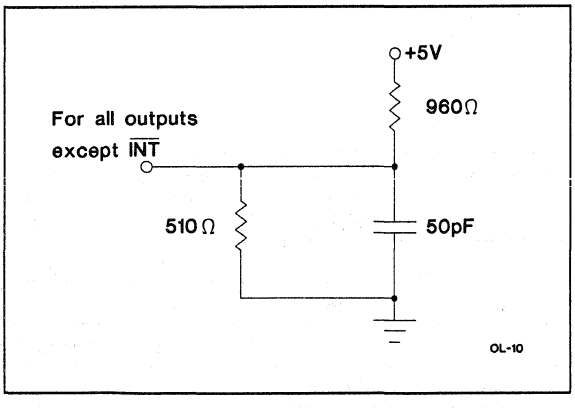


Figure 5. Output Load A

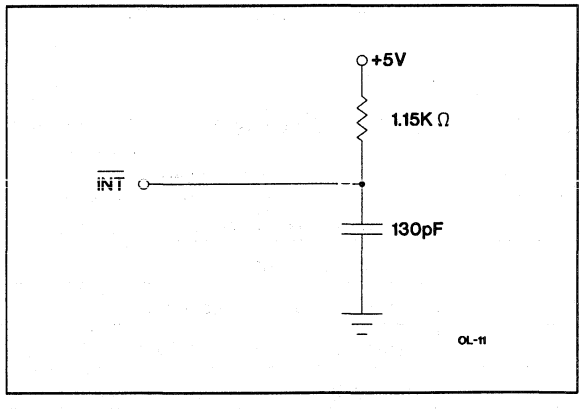


Figure 6. Output Load B

Read/Write Timing ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns	
t_{ASW}	Pulse width, AS high	30	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

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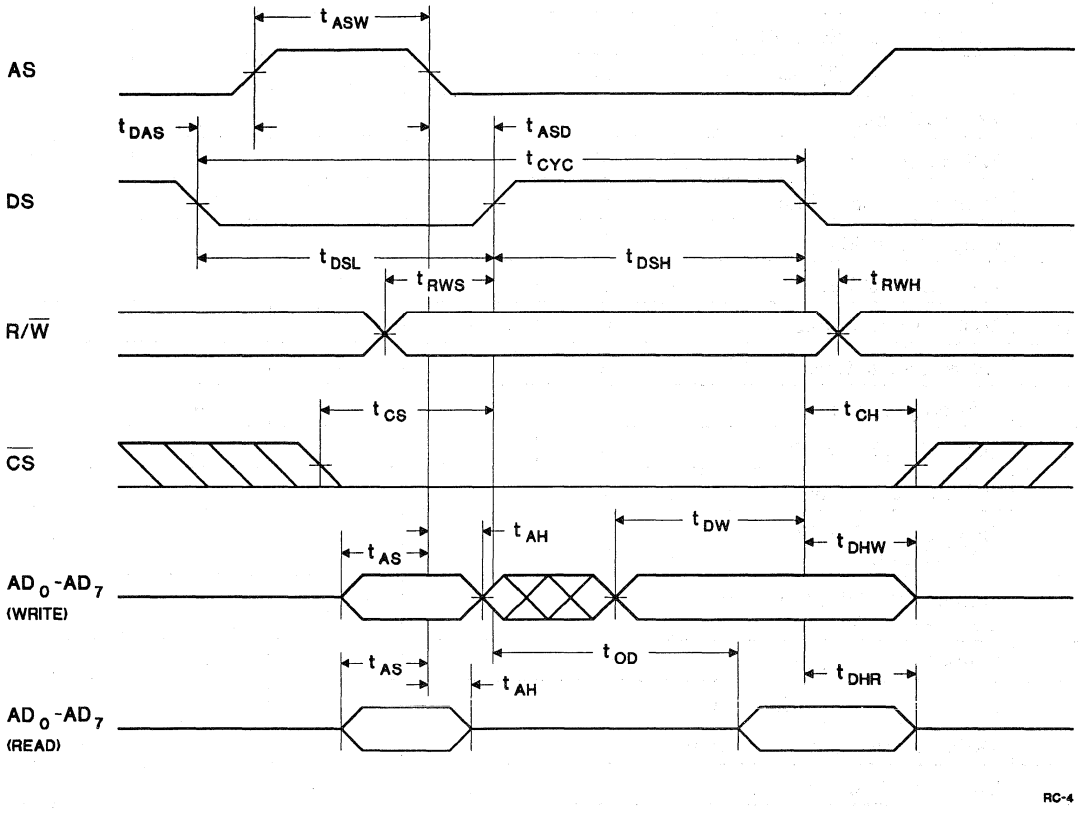
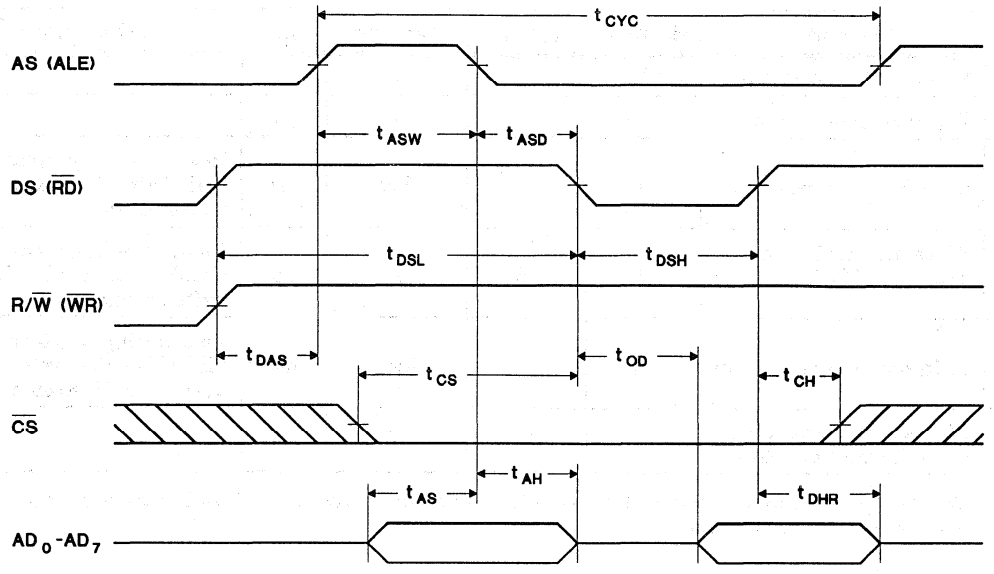
Motorola Bus Read/Write Timing (PLCC Package Only)

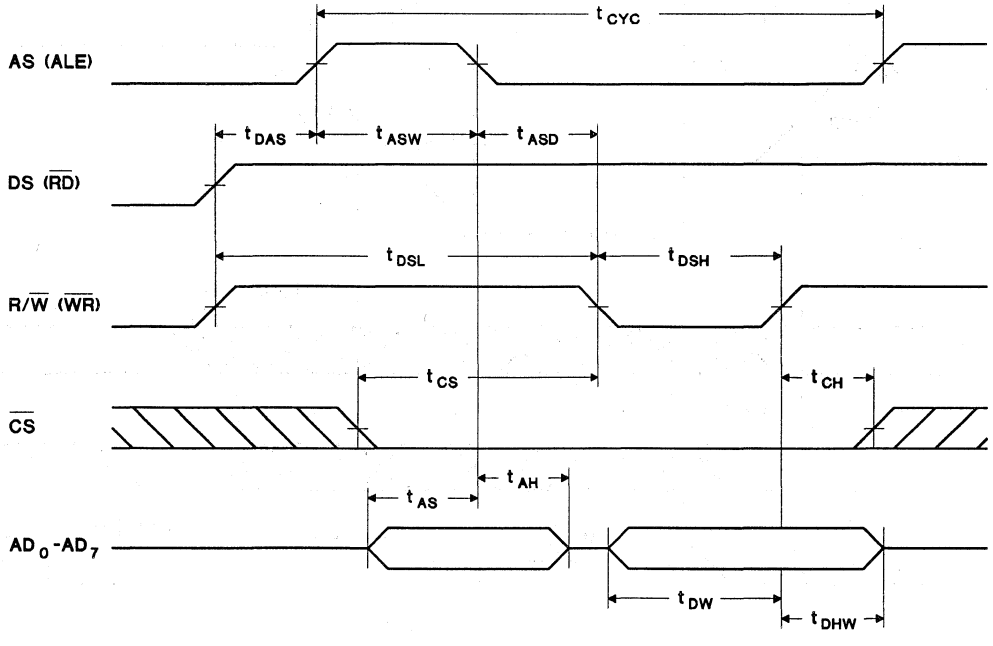


Intel Bus Read Timing



RC-5

Intel Bus Write Timing



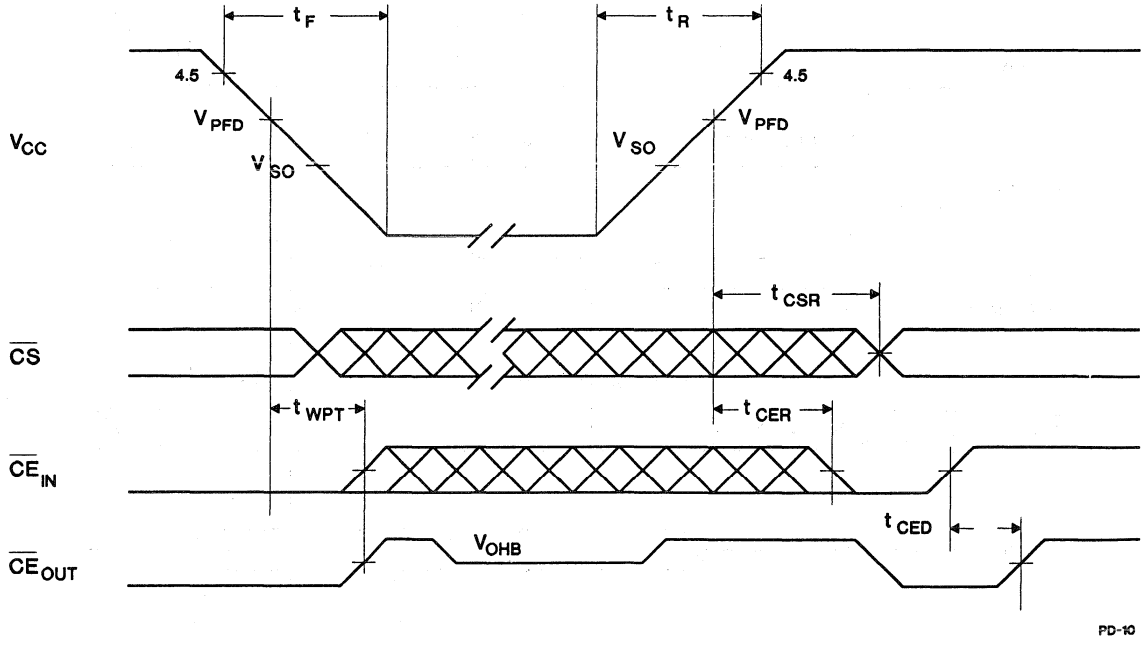
WC-5

Power-Down/Power-Up Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	7	10	ns	

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

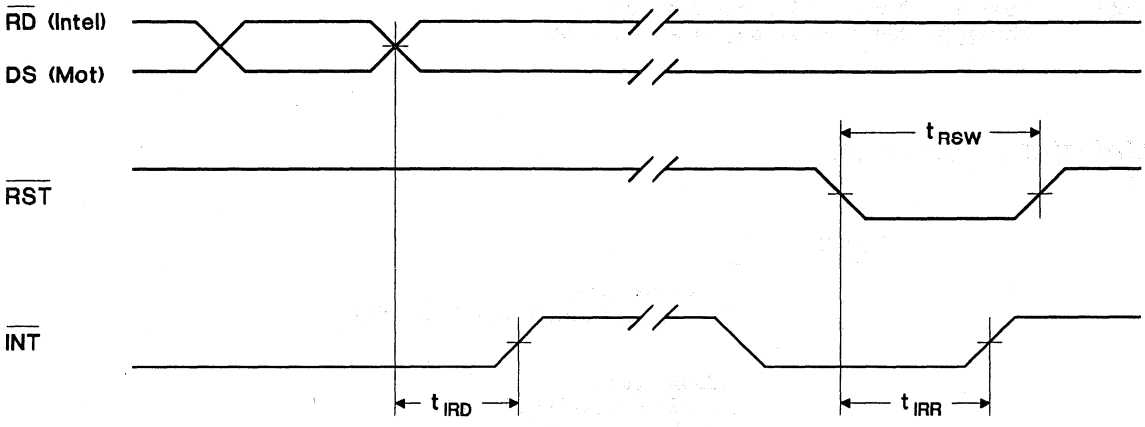
Power-Down/Power-Up Timing



Interrupt Delay Timing ($T_A = T_{OPR}$)

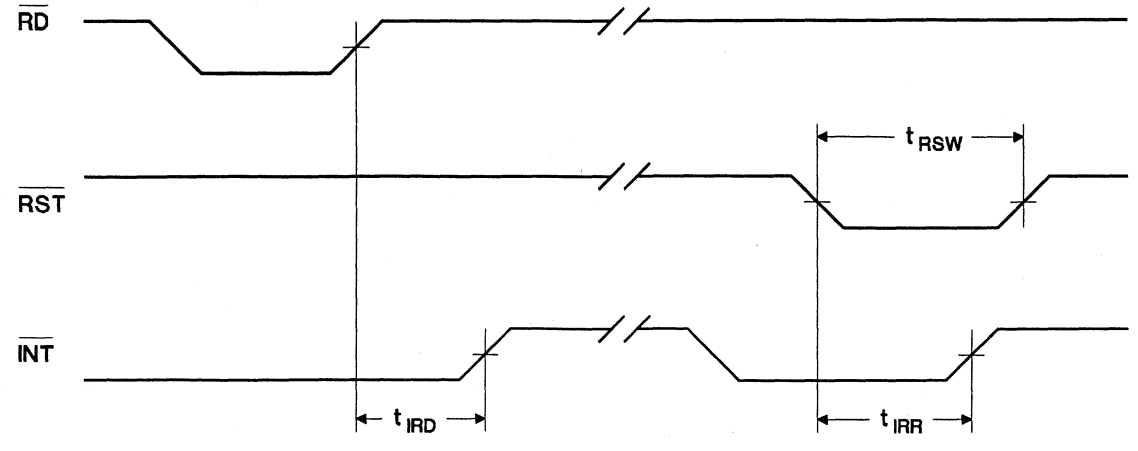
Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)	-	-	2	µs

Interrupt Delay Timing (PLCC Package Only)



INT-1

Interrupt Delay Timing (SOIC, DIP Packages)



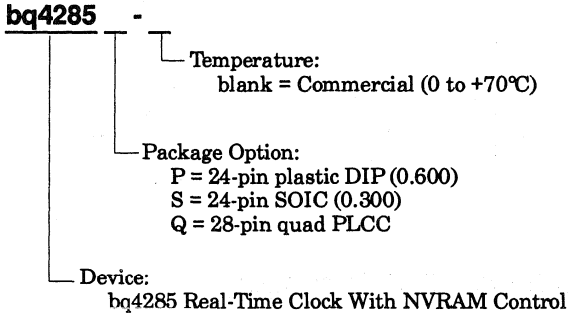
INT-4

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4-81	Address strobe input	Clarification
1	4-90	Backup cell voltage V_{BC}	Was 2.0 min; is 2.5 min
1	4-91	Power-fail detect voltage V_{PFD}	Was 4.1 min, 4.25 max; is 4.0 min, 4.35 max
1	4-91	Chip enable input current	Additional specification
2	4-81, 4-91	Crystal type Daiwa DT-26 (not DT-26S)	Clarification

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.

Ordering Information



bq4285E/bq4285L

Enhanced RTC With NVRAM Control

Features

- Enhanced features include:
  - System wake-up capability—alarm interrupt output active in battery-backup mode
  - 2.7–3.6V operation (bq4285L); 4.5–5.5V operation (bq4285E)
  - 32KHz output for power management
- 114 bytes of general nonvolatile storage
- Automatic backup and write-protect control to external SRAM
- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
- Less than 0.5 µA load under battery operation
- Selectable Intel or Motorola bus timing (PLCC), Intel bus timing (DIP and SOIC)
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP or SOIC and 28-pin PLCC

General Description

The CMOS bq4285E/bq4285L is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

A 32.768kHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode.

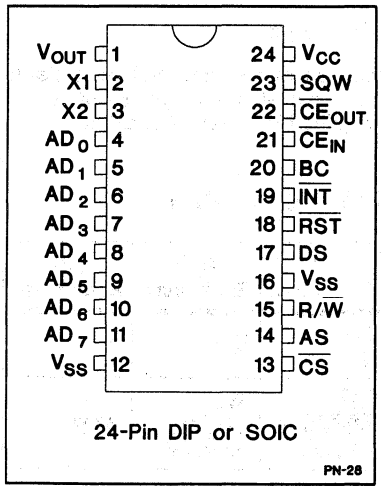
The bq4285E/bq4285L write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq4285E/bq4285L is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

The bq4285E/bq4285L integrates a battery-backup controller to make a

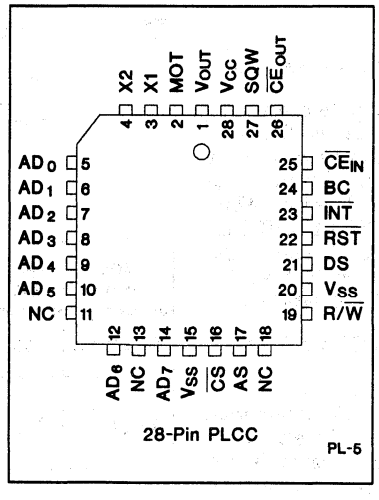
4

Pin Connections



24-Pin DIP or SOIC

PN-28



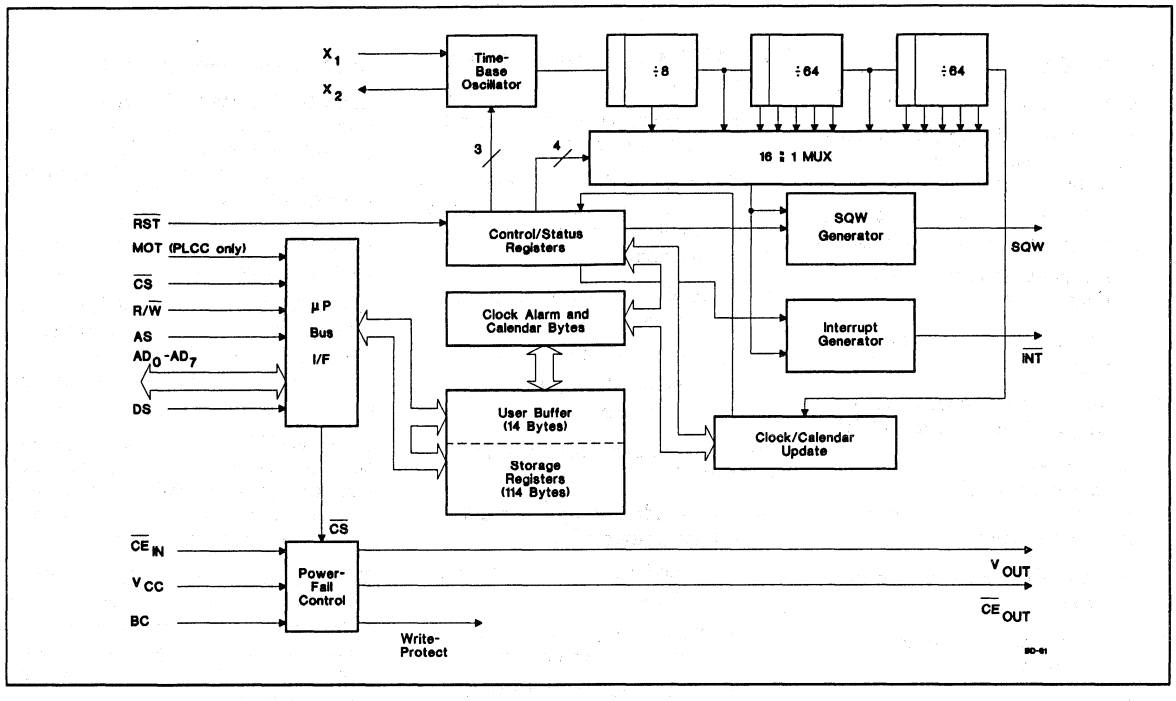
28-Pin PLCC

PL-5

Pin Names

AD0-AD7	Multiplexed address/data input/output
MOT	Bus type select input (PLCC only)
$\overline{CS}$	Chip select input
AS	Address strobe input
DS	Data strobe input
R/$\overline{W}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
BC	3V backup cell input
X1, X2	Crystal inputs
NC	No connect
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
VOUT	Supply output
VCC	+5V supply
VSS	Ground

Block Diagram



standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4285E/bq4285L automatically write-protects the external SRAM and provides a V_{CC} output sourced from the clock backup battery.

Pin Descriptions

AD_0–AD_7 Multiplexed address/data input/output

The bq4285E/bq4285L bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq4285E/bq4285L on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

MOT Bus type select input (PLCC package only)

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 20KΩ resistor. For the DIP and SOIC packages, this pin is internally connected to V_{SS}, enabling the bus timing for the Intel architecture.

$\overline{CS}$ Chip select input

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq4285E/bq4285L.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP, SOIC, and PLCC packages with MOT = V_{CC}, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

For DIP, SOIC, and PLCC packages with MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

For the PLCC package, when MOT = V_{CC}, DS controls data transfer during a bq4285E/bq4285L bus cycle. During a read cycle, the bq4285E/bq4285L drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

R/$\overline{W}$ **Read/write input**

For DIP, SOIC, and PLCC packages with MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq4285E/bq4285L.

For the PLCC package, when MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. This allows $\overline{INT}$ to be valid in battery-backup mode for the alarm interrupt. To use this feature, $\overline{INT}$ must be connected to a power supply other than V_{CC}. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

$\overline{RST}$ **Reset input**

The bq4285E/bq4285L is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq4285E/bq4285L is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

SQW **Square-wave output**

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

A 32.768kHz output is enabled by setting the SQWE bit in register B to 1 and the 32KE bit in register C to 1 after setting OSC2–OSC0 in register A to 011 (binary).

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of power. When V_{CC} slows down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

X1, X2 **Crystal input**

The X1, X2 inputs are provided for an external 32.768Khz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

$\overline{CE}_{IN}$ **External RAM chip enable input, active low**

$\overline{CE}_{IN}$ should be driven low to enable the controlled external RAM. $\overline{CE}_{IN}$ is internally pulled up with a 50KΩ resistor.

$\overline{CE}_{OUT}$ **External RAM chip enable output, active low**

When power is valid, $\overline{CE}_{OUT}$ reflects $\overline{CE}_{IN}$.

V_{OUT} **Supply output**

V_{OUT} provides the higher of V_{CC} or V_{BC}, switched internally, to supply external RAM.

V_{CC} **Positive power supply**

V_{SS} **Ground**

4

Functional Description

Address Map

The bq4285E/bq4285L provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq4285L.

Update Period

The update period for the bq4285E/bq4285L is one second. The bq4285E/bq4285L updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq4285E/bq4285L copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

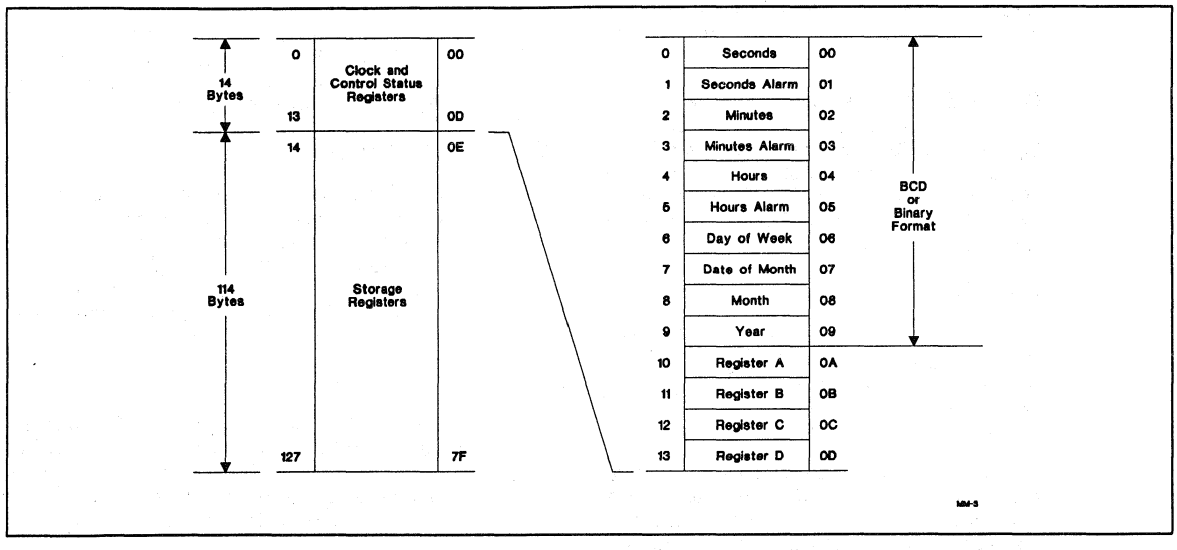


Figure 1. Address Map

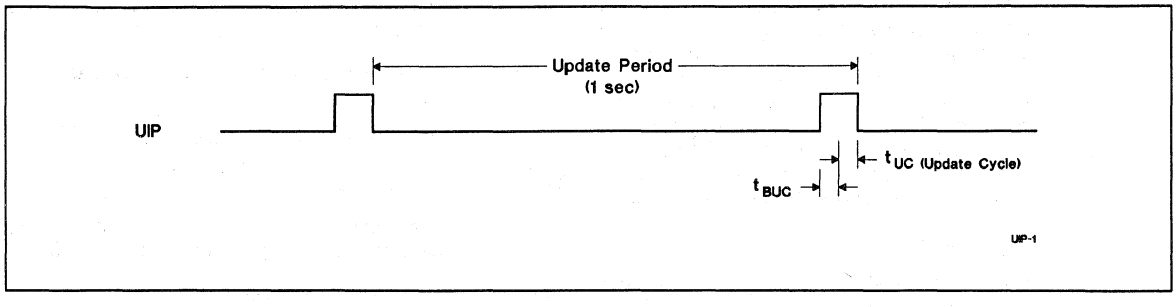


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square Wave Output

The bq4285E/bq4285L divides the 32.768kHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B. A 32.768kHz output may be selected by setting OSC2–OSC0 in register A to 011 while SQWE = 1 and 32KE = 1.

Interrupts

The bq4285E/bq4285L allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a "wake-up" feature.
- The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq4285E/bq4285L interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits							Square Wave		Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	1	0	0	0	0	0	None		None	
0	1	0	0	0	0	1	256	Hz	3.90625	ms
0	1	0	0	0	1	0	128	Hz	7.8125	ms
0	1	0	0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	1	0	0	4.096	kHz	244.141	µs
0	1	0	0	1	0	1	2.048	kHz	488.281	µs
0	1	0	0	1	1	0	1.024	kHz	976.5625	µs
0	1	0	0	1	1	1	512	Hz	1.953125	ms
0	1	0	1	0	0	0	256	Hz	3.90625	ms
0	1	0	1	0	0	1	128	Hz	7.8125	ms
0	1	0	1	0	1	0	64	Hz	15.625	ms
0	1	0	1	0	1	1	32	Hz	31.25	ms
0	1	0	1	1	0	0	16	Hz	62.5	ms
0	1	0	1	1	0	1	8	Hz	125	ms
0	1	0	1	1	1	0	4	Hz	250	ms
0	1	0	1	1	1	1	2	Hz	500	ms
0	1	1	X	X	X	X	32.768	kHz	same as above defined by RS3–RS0	

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122μs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3). Setting OSC2–OSC0 in register A to 011 does not affect the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt request is valid in battery-backup mode, providing a "wake-up" capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler will have a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq4285E/bq4285L and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns

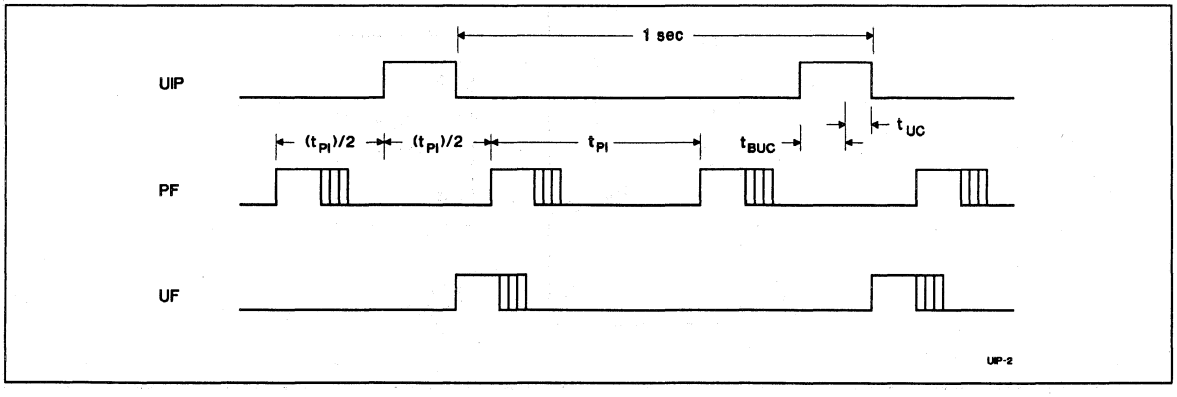


Figure 3. Update-Ended/Periodic Interrupt Relationship

the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

Power-Down/Power-Up Cycle

The bq4285E/bq4285L power-up/power-down cycles are different. The bq4285L continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (2.53V typical), the bq4285L write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

The bq4285E continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq4285E write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4285E/bq4285L. As the voltage input V_{CC} slows down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in process to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (30µs maximum), the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. CE_{OUT} is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the main supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. If $V_{PFD} < V_{BC}$ on the bq4285L, the switch to the main supply occurs at V_{PFD}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 10ns.

Figure 4 shows the hardware hookup for the external RAM.

A primary backup energy source input is provided on the bq4285E/bq4285L. The BC input accepts a 3V primary battery, typically some type of lithium chemistry. To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{OUT}$ are internally isolated from BC by the initial connection of a battery. Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM.

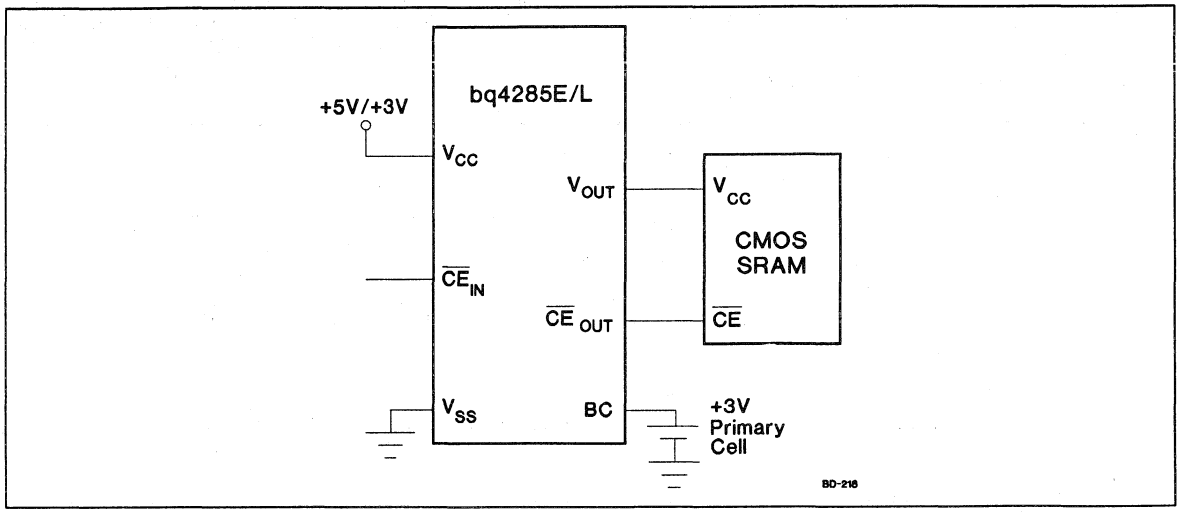


Figure 4. External RAM Hookup to the bq4285E/bq4285L RTC

Control/Status Registers

The four control/status registers of the bq4285E/bq4285L are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

4

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.
2. Read/write only when OSC2–OSC0 in register A is 011 (binary).

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq4285E/bq4285L increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	-	0	0

These bits are always set to 0.

32KE –32KHz Enable Output

7	6	5	4	3	2	1	0
-	-	-	-	-	32KE	-	-

This bit may be set to a 1 only when the OSC2–OSC0 bits in register A are set to 011. Setting OSC2–OSC0 to anything other than 011 clears this bit. If SQWE in register B and 32KE are set, a 32.768KHz waveform is output on the square wave pin.

UF - Update Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings—bq4285E

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Absolute Maximum Ratings—bq4285L

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 6.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 6.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions—bq4285E ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.5	-	4.0	V

Notes: Typical values indicate operation at T_A = 25°C.
Potentials are relative to V_{SS}.

Recommended DC Operating Conditions—bq4285L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	2.7	3.15	3.6	V
V_{IL}	Input low voltage	-0.3	-	0.6	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.4	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.
Potentials are relative to V_{SS}.

Crystal Specifications—bq4285E/bq4285L (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

DC Electrical Characteristics—bq4285E ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
I_{CCSB}	Standby supply current	-	300	-	µA	$V_{IN} = V_{CC}$ or V_{SS}, $\overline{CS} \geq V_{CC}$ - 0.2, no load on V_{OUT}
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V				I_{OUT} = 100µA, $V_{CC} < V_{BC}$
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-275	µA	Internal 20K pull-down
$I_{\overline{CE}}$	Chip enable input current	-	-	100	µA	Internal 50K pull-up

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

DC Electrical Characteristics—bq4285L ($T_A = T_{OPR}$, V_{CC} = 3.13V ± 0.45%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.2	-	-	V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	5	9	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
V_{SO}	Supply switch-over voltage	-	V_{PFD}	-	V	$V_{BC} > V_{PFD}$
		-	V_{BC}	-	V	$V_{BC} < V_{PFD}$
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
I_{CCSB}	Standby supply current	-	100	-	µA	$V_{IN} = V_{CC}$ or V_{SS}, $\overline{CS} \geq V_{CC}$ - 0.2, no load on V_{OUT}
V_{PFD}	Power-fail-detect voltage	2.4	2.53	2.65	V	
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 80mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V				I_{OUT} = 100µA, $V_{CC} < V_{BC}$
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-185	µA	Internal 30K pull-down
$I_{\overline{CE}}$	Chip enable input current	-	-	120	µA	Internal 30K pull-up

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 3V.

4

Capacitance—bq4285E/bq4285L (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested. It does not include the X1 or X2 pin.

AC Test Conditions—bq4285E

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 5 and 6

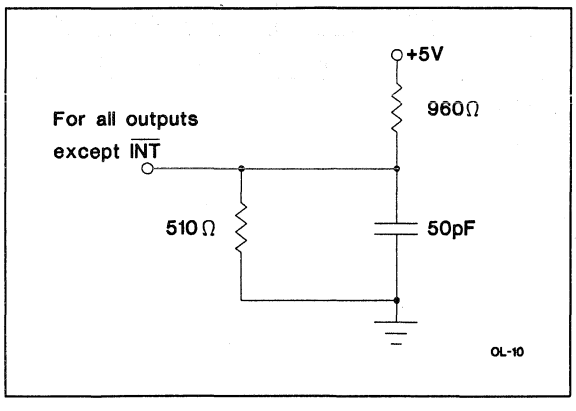


Figure 5. Output Load A—bq4285E

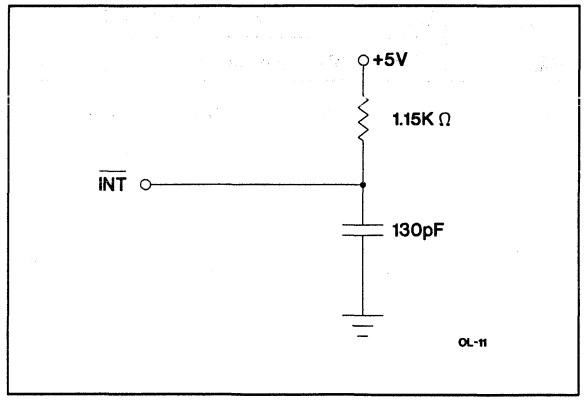


Figure 6. Output Load B—bq4285E

AC Test Conditions—bq4285L

Parameter	Test Conditions
Input pulse levels	0 to 2.3 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.2 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 7 and 8

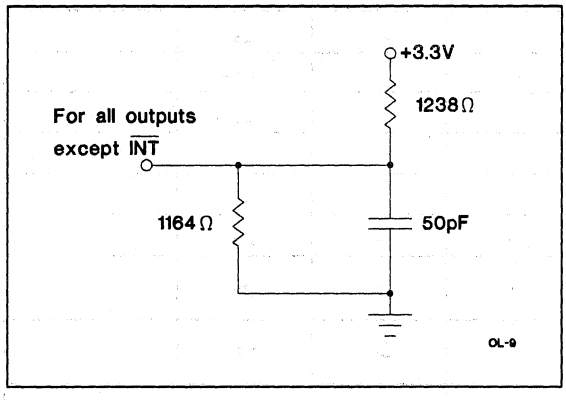


Figure 7. Output Load A—bq4285L

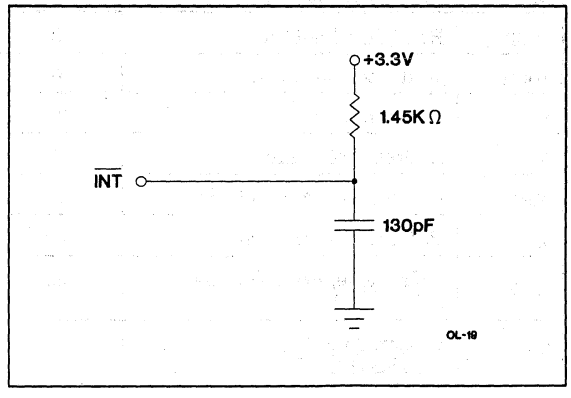


Figure 8. Output Load B—bq4285L

Read/Write Timing—bq4285E ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

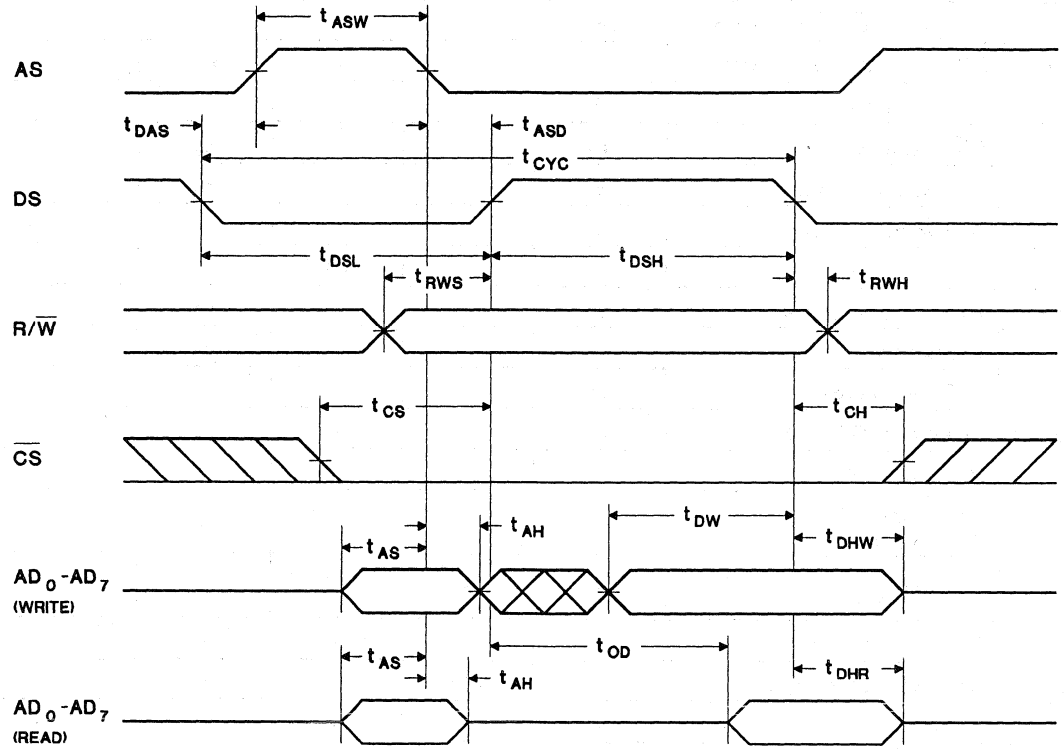
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns	
t_{ASW}	Pulse width, AS high	30	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

Read/Write Timing—bq4285L ($T_A = T_{OPR}$, V_{CC} = 3.15V ± 0.45%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	270	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	135	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	90	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	15	-	-	ns	
t_{CS}	Chip select setup time	8	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	40	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	30	-	-	ns	
t_{AH}	Address hold time	15	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	15	-	-	ns	
t_{ASW}	Pulse width, AS high	50	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	55	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	100	ns	
t_{DW}	Write data setup time	50	-	-	ns	
t_{BUC}	Delay time before update	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

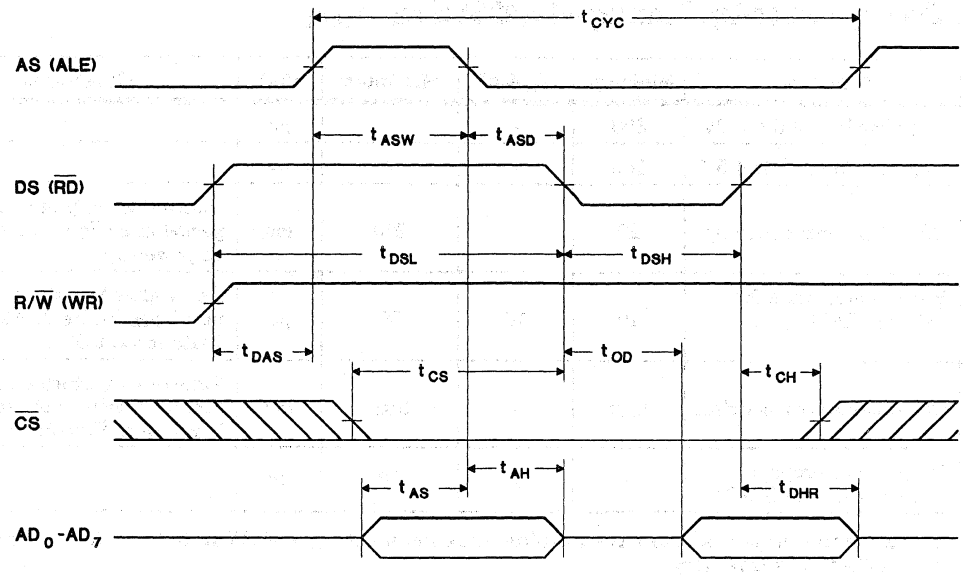
4

Motorola Bus Read/Write Timing—bq4285E/bq4285L (PLCC Package Only)



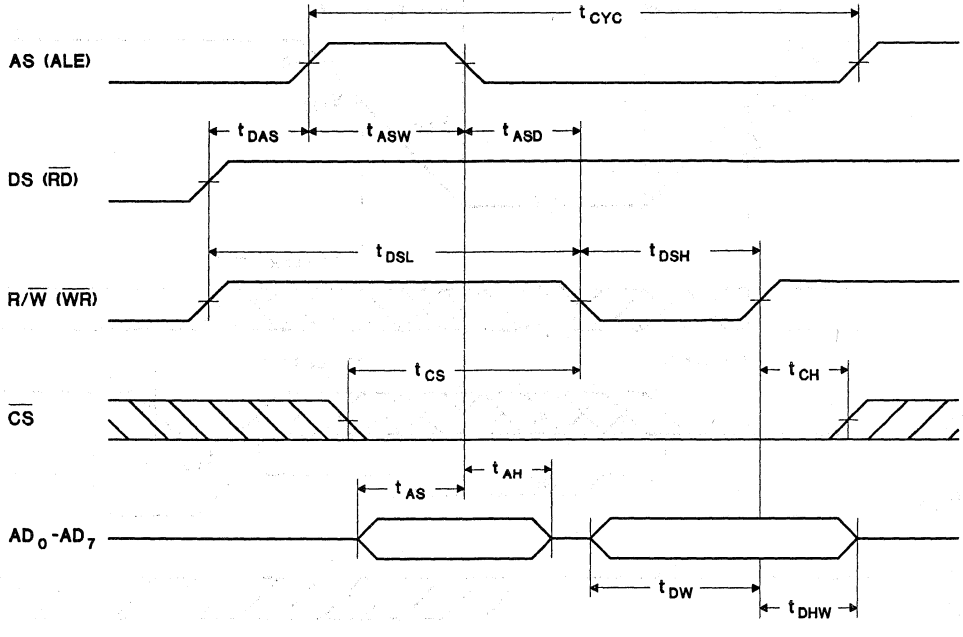
RC-4

Intel Bus Read Timing—bq4285E/bq4285L



RC-5

Intel Bus Write Timing—bq4285E/bq4285L



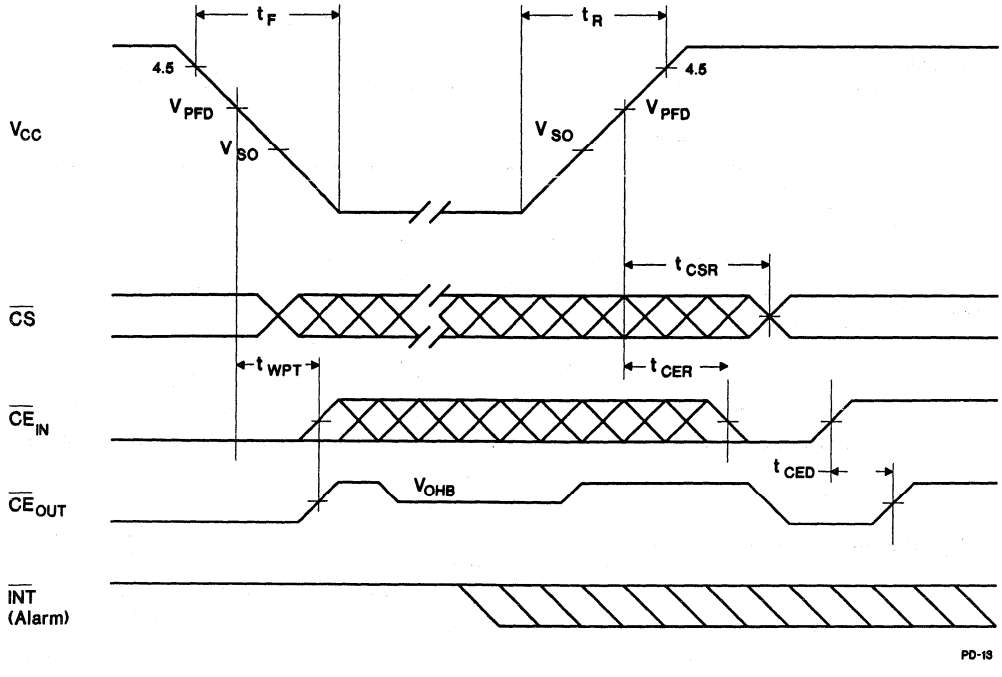
WC-5

Power-Down/Power-Up Timing—bq4285E ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slows down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	7	10	ns	

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing—bq4285E

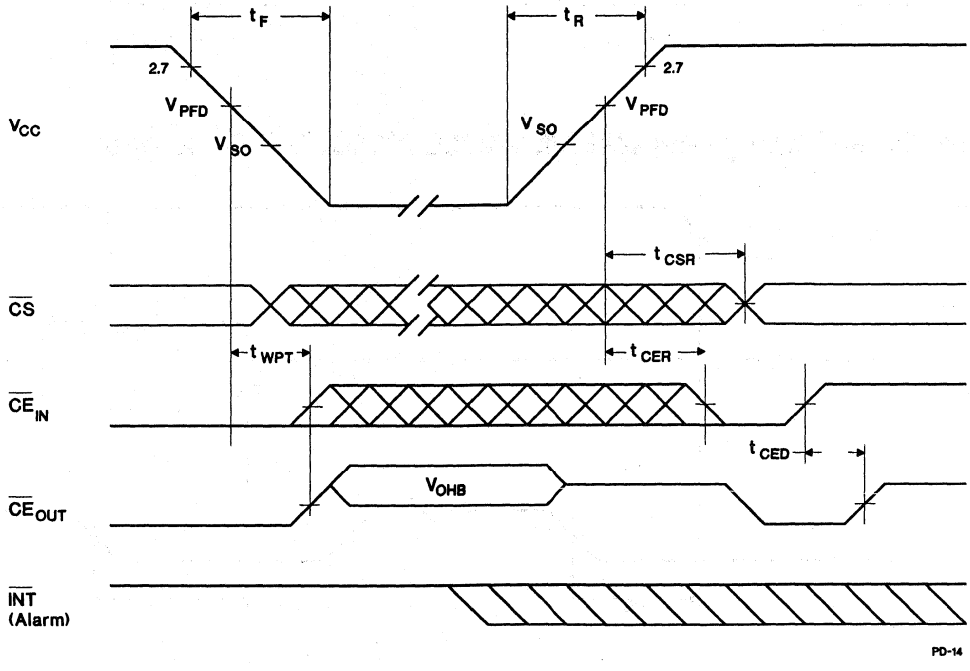


Power-Down/Power-Up Timing—bq4285L (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 2.7V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 2.7V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{WPT}	Write-protect time for external RAM	-	0	-		$V_{BC} > V_{PFD}$
		10	16	30	µs	$V_{BC} < V_{PFD}$
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	9	15	ns	

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

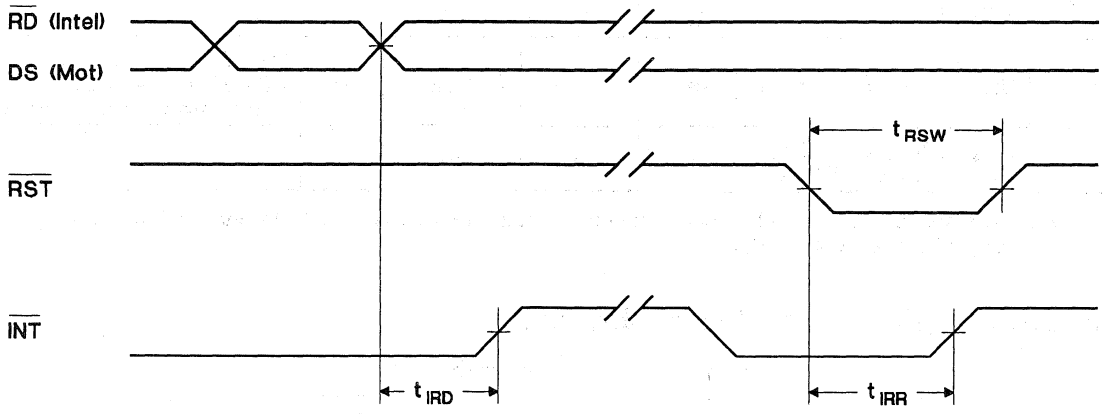
Power-Down/Power-Up Timing—bq4285L



Interrupt Delay Timing—bq4285E/bq4285L ($T_A = T_{OPR}$)

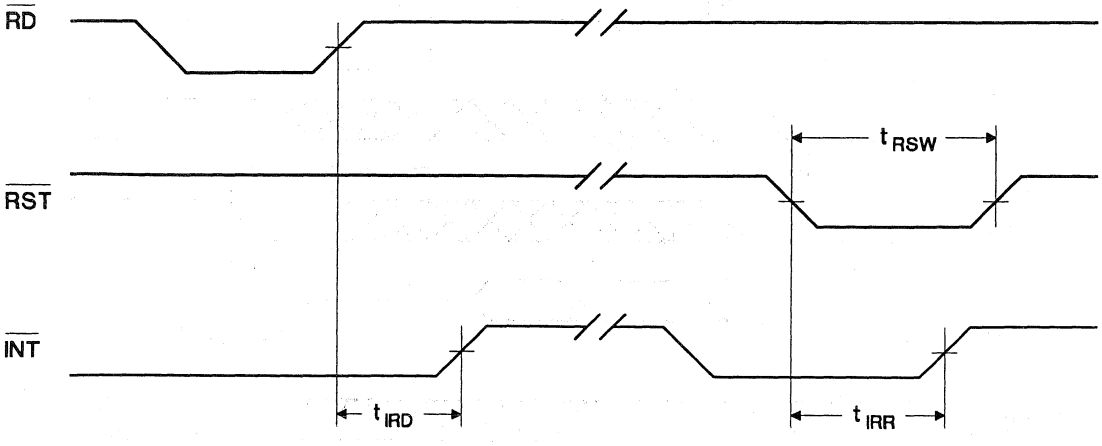
Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS ($\overline{RD}$)	-	-	2	µs

Interrupt Delay Timing—bq4285E/bq4285L (PLCC Package Only)



INT-1

Interrupt Delay Timing—bq4285E/bq4285L (SOIC, DIP Packages)



INT-4

Ordering Information

bq4285E/bq4285L _ -

- Temperature:
  - blank = Commercial (0 to +70°C)
  - N = Industrial* (-40 to +85°C)
- Package Option:
  - P = 24-pin plastic DIP (0.600)
  - S = 24-pin SOIC (0.300)
  - Q = 28-pin quad PLCC
  - SS = 24-pin SSOP (0.150)
- Device:
  - bq4285E/bq4285L Real-Time Clock With NVRAM Control

*bq4285E Q package only.

4

BENCHMARQ

bq4287

Real-Time Clock Module With NVRAM Control

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1287/DS1287A and MC146818A
- 114 bytes of general nonvolatile storage
- Automatic backup supply and write-protection to make external SRAM nonvolatile
- Integral lithium cell and crystal
- 160 ns cycle time allows fast bus operation
- Intel bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- Better than one minute per month clock accuracy

General Description

The CMOS bq4287 is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

The bq4287 write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

The bq4287 uses its integral battery-backup controller and battery to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4287 automatically write-protects the external SRAM and provides a V_{CC} output sourced from its internal battery.

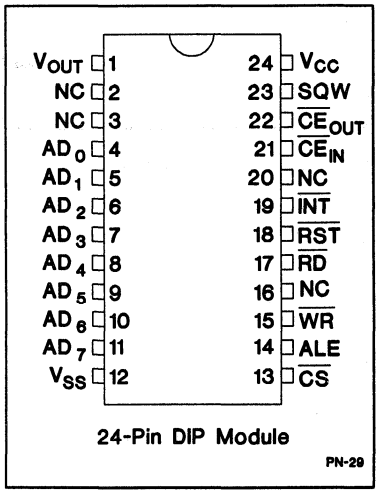
The bq4287 is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of V_{CC}, this isolation is broken, and the backup cell provides data retention to the clock, internal RAM, V_{OUT}, and $\overline{CE}_{OUT}$ on subsequent power-downs.

Caution:

Care should be taken to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

Pin Connections



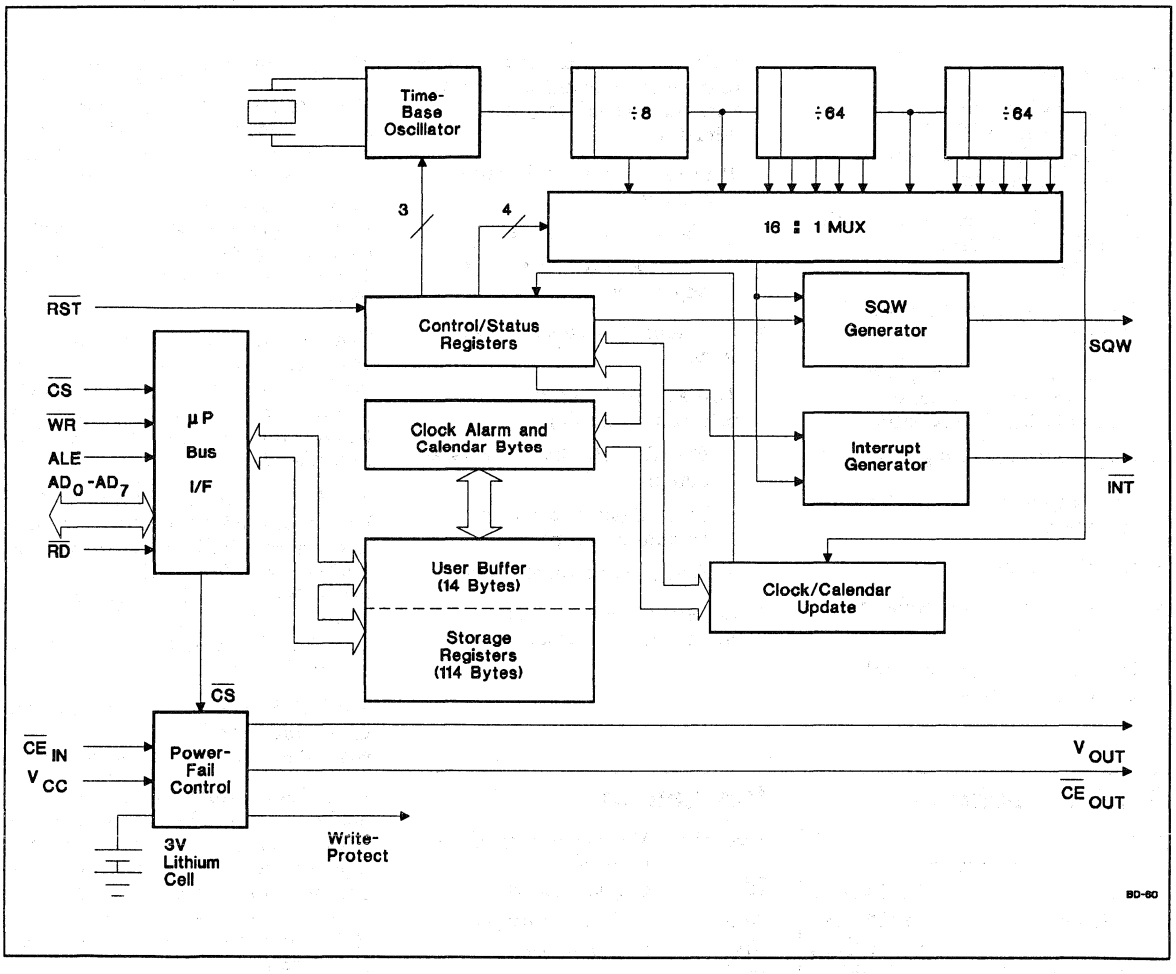
24-Pin DIP Module

PN-29

Pin Names

AD_0–AD_7	Multiplexed address/data input/output
$\overline{CS}$	Chip select input
ALE	Address strobe input
$\overline{RD}$	Data strobe input
$\overline{WR}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
NC	No connect
V_{OUT}	Supply output
V_{CC}	+5V supply
V_{SS}	Ground

Block Diagram



Pin Descriptions

AD_0–AD_7 Multiplexed address/data input/output

The bq4287 bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq4287 on the falling edge of the ALE signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins act as a bidirectional data bus.

$\overline{CS}$ Chip select input

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq4287.

ALE Address latch enable

ALE serves to demultiplex the address/data bus. The falling edge of ALE latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal.

$\overline{RD}$ Read input

The falling edge on $\overline{RD}$ is used to enable the outputs during a read cycle.

$\overline{WR}$ Write input

The rising edge on $\overline{WR}$ latches data into the bq4287.

$\overline{INT}$ Interrupt request output

$\overline{INT}$ is an open-drain output. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

$\overline{RST}$ Reset input

The bq4287 is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq4287 is not accessible. Table 3 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

SQW Square-wave output

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

$\overline{CE}_{IN}$ External RAM chip enable input, active low

$\overline{CE}_{IN}$ should be driven low to enable the controlled external RAM. $\overline{CE}_{IN}$ is internally pulled up with a 50KΩ resistor.

$\overline{CE}_{OUT}$ External RAM chip enable output, active low

When power is valid, $\overline{CE}_{OUT}$ reflects $\overline{CE}_{IN}$.

V_{OUT} Supply output

V_{OUT} provides the higher of V_{CC} or V_{BC}, switched internally to supply external RAM.

V_{CC} +5V supply

V_{SS} Ground

4

Functional Description

Address Map

The bq4287 provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq4287.

Update Period

The update period for the bq4287 is one second. The bq4287 updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq4287 copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes is frozen, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

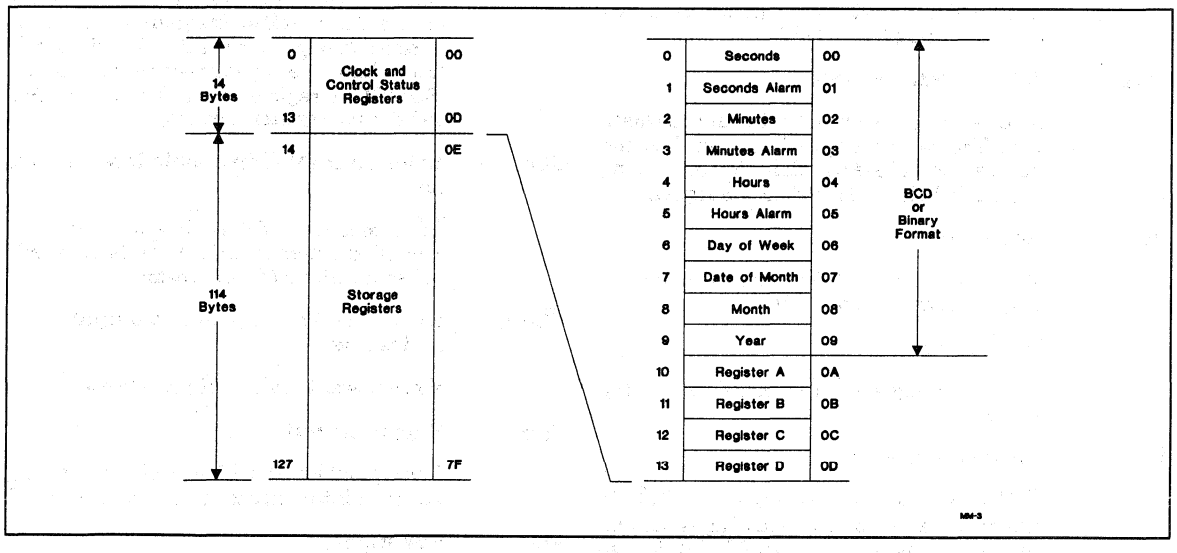


Figure 1. Address Map

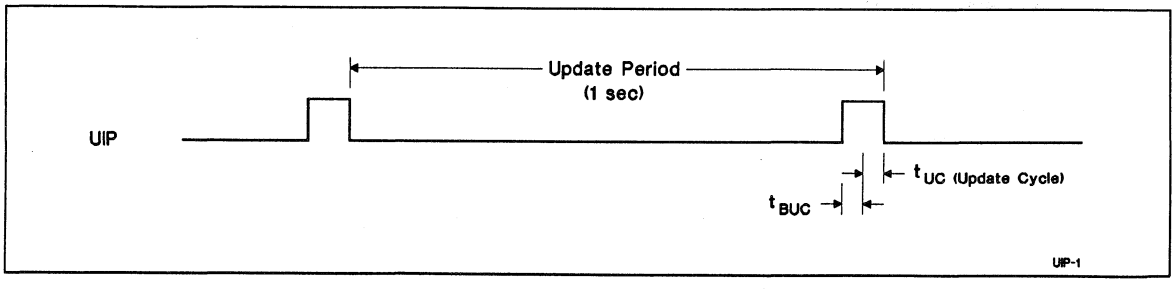


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 1).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format bit (DF) to select BCD or binary format for all clock and calendar bytes.
   c. Write the appropriate value to the hour format bit (HR).
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 1. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq4287 divides the 32.768kHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 2). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B.

Interrupts

The bq4287 allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of an RTC update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq4287 interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 2. Square Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	4.096	kHz	244.141	µs
0	1	0	1	2.048	kHz	488.281	µs
0	1	1	0	1.024	kHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 2).

Alarm Interrupt

During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar readings during an update cycle may be in error. Three methods to access the RTC bytes without ambiguity are available:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler finishes accessing the clock bytes in $t_{PI}/2 + t_{BUC}$ time (see Figure 3).

Oscillator Control

The bq4287 is shipped from Benchmarq with its internal oscillator turned off. The internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

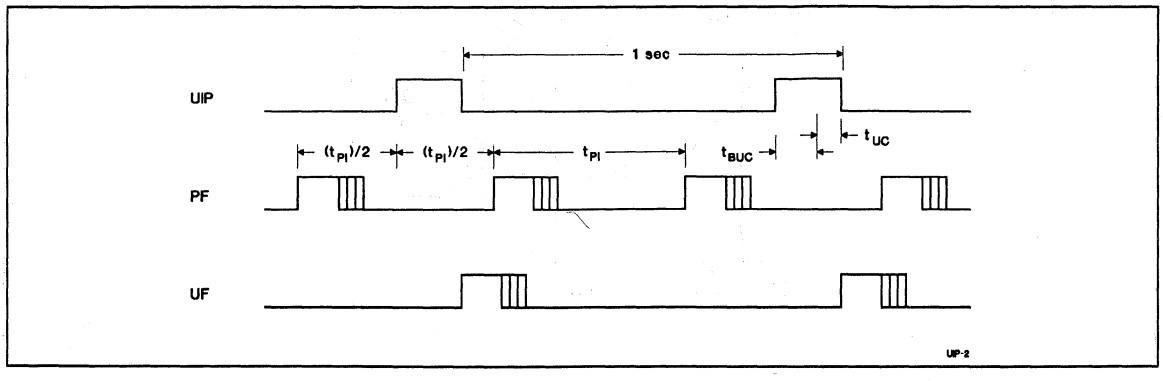


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq4287 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq4287 write-protects the clock and storage registers. When V_{CC} is below V_{SO} (3V typical), the power source is switched to the internal lithium cell. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{SO}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM can be battery-backed using the V_{OUT} and RAM chip enable output pins from the bq4287. As the voltage input V_{CC} slows down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input, $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in process to the external SRAM during power-fail detection, the memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (30µs maximum), the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{OUT}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 10 ns.

The internal lithium cell is capable of supplying 3V on V_{OUT} for an extended period of time. The length of time that the external SRAM retains data is a function of the data-retention current of the SRAMs used. The initial capacity of the internal lithium cell is 130mAh. Typically, if the data-retention current for external SRAM is 1µA at room temperature and the clock data-retention current (I_{CCB}) is 0.5µA, cumulative data-retention time is calculated to be more than nine years.

The bq4287 battery life is a function of the time spent in battery-backed mode and the data-retention current of the external SRAM. For example, office equipment is generally powered on for 8 hours and powered off for 16 hours. Under these conditions, a single bq4287 provides an SRAM drawing 1µA total data-retention current with more than 14 years of nonvolatility.

The hardware hookup is shown in Figure 4.

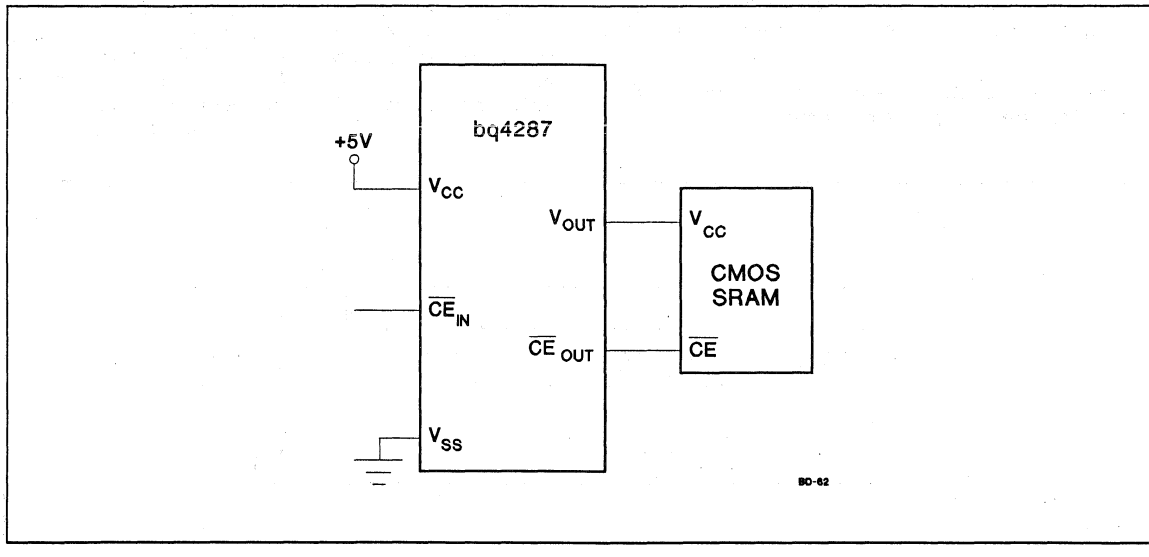


Figure 4. External RAM Hookup to the bq4287 RTC

As shipped from Benchmarq, the internal lithium cell is electrically isolated from active circuitry including V_{OUT} and $\overline{CE}_{OUT}$. Self-discharge in this condition is less than 0.5% per year at 20°C.

Note: Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM.

Caution:

Care should be taken to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

Control/Status Registers

The four control/status registers of the bq4287 are accessible regardless of the status of the update cycle (see Table 3).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 2.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. The bq4287 is shipped from Benchmarq with its oscillator turned off. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

4

Table 3. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No	INTF	0	PF	0	AF	0	UF	0	-	0	-	0	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.
1. Except bit 7.

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq4287 increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	0	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

UF - Update-Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	$V_{CC} + 0.3$	V

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity	-	130	-	mAh	Refer to graphs in Typical Battery Characteristics section
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4	-	-	V	$I_{OH} = -1.0$ mA
V_{OL}	Output low voltage	-	-	0.4	V	$I_{OL} = 4.0$ mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCB}	Battery operation current	-	0.3	0.5	µA	$V_{BC} = 3V$, $T_A = 25°C$, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{SO}	Supply switch-over voltage	-	3.0	-	V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{BC}	Backup cell voltage	-	3.0	-	V	Internal backup cell voltage; refer to graphs in Typical Battery Characteristics section
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	$I_{OUT} = 100$mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V	-	-	V	$I_{OUT} = 100$µA, $V_{CC} < V_{BC}$
$I_{\overline{CE}}$	Chip enable input current	-	-	100	µA	Internal 50K pull-up

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 5 and 6

4

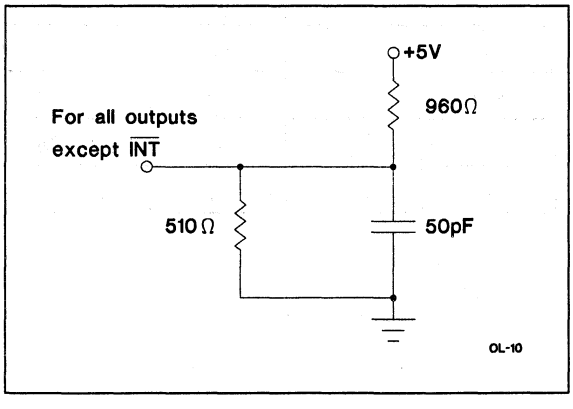


Figure 5. Output Load A

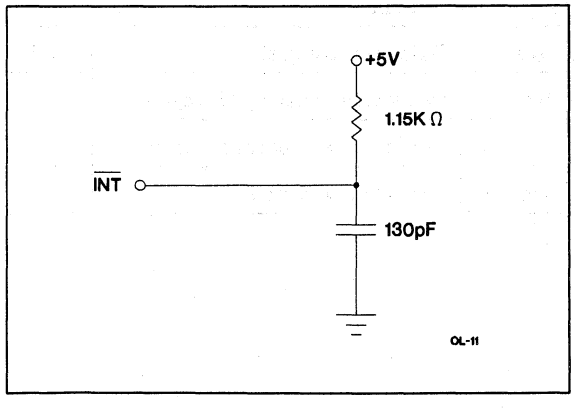
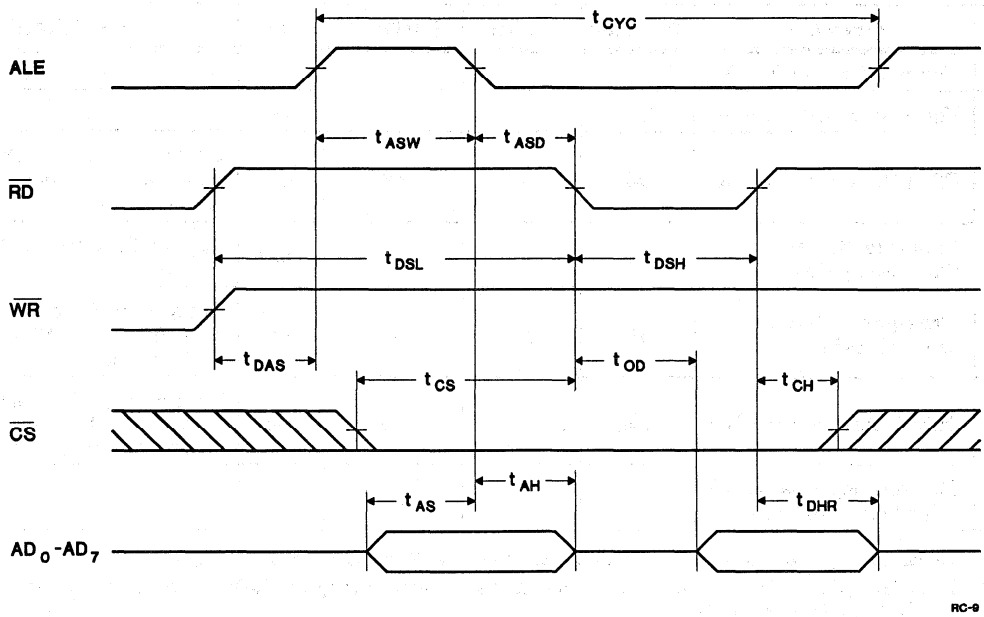


Figure 6. Output Load B

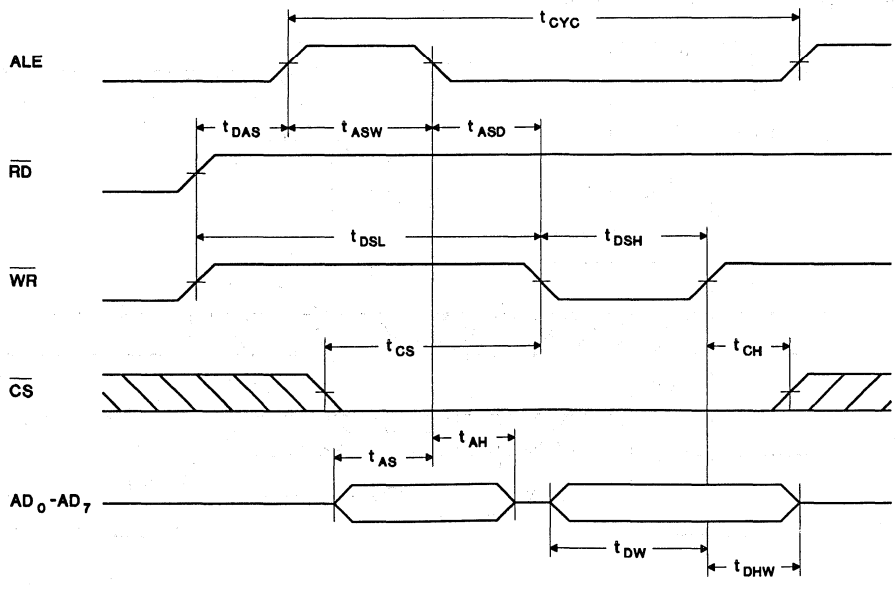
Read/Write Timing (TA = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	$\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	$\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, $\overline{RD}$ to ALE rise	10	-	-	ns	
t_{ASW}	Pulse width, ALE high	30	-	-	ns	
t_{ASD}	Delay time, ALE to $\overline{RD}/\overline{WR}$ fall	35	-	-	ns	
t_{OD}	Output data delay time from $\overline{RD}$ fall	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 2
t_{UC}	Time of update cycle	-	1	-	µs	

Read Timing



Write Timing



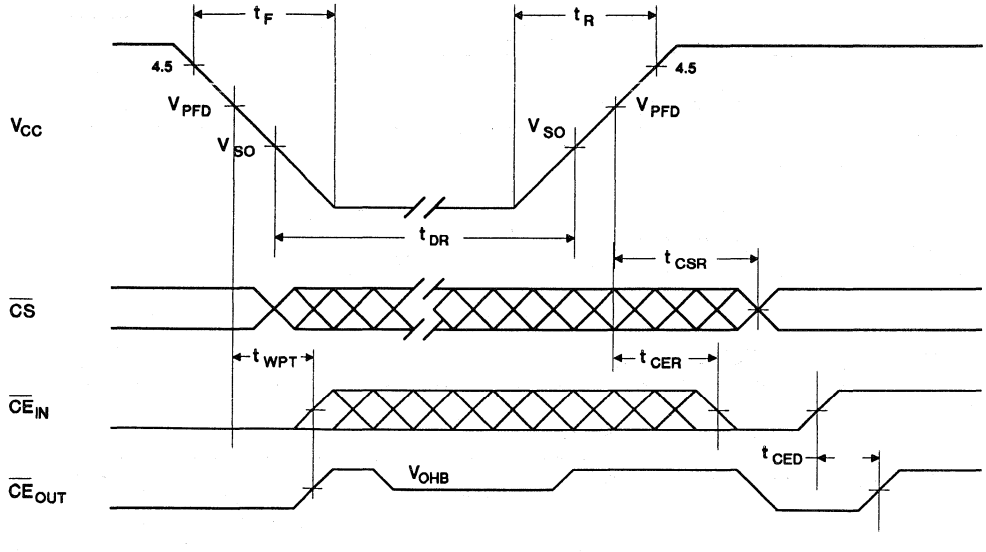
Power-Down/Power-Up Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10	-	-	years	T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slows down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	7	10	ns	

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

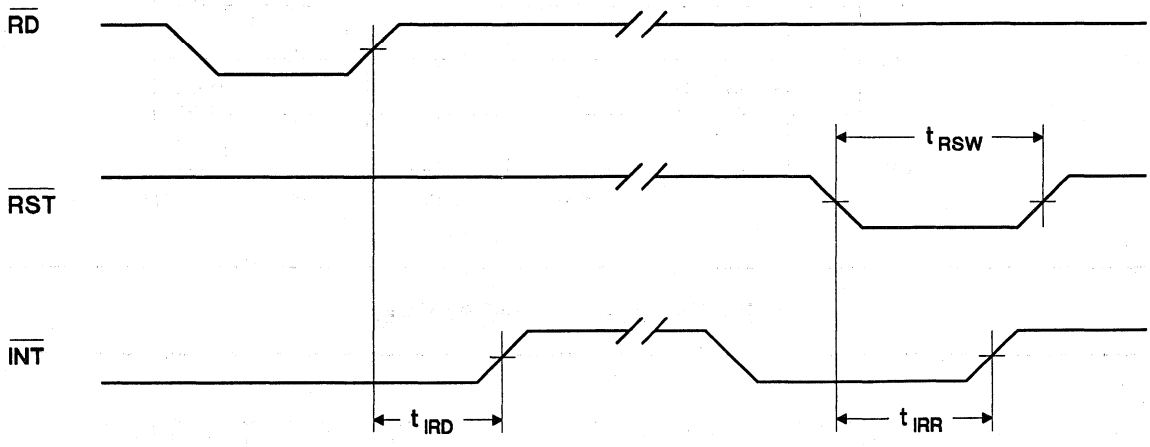
Power-Down/Power-Up Timing



Interrupt Delay Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from $\overline{RD}$	-	-	2	µs

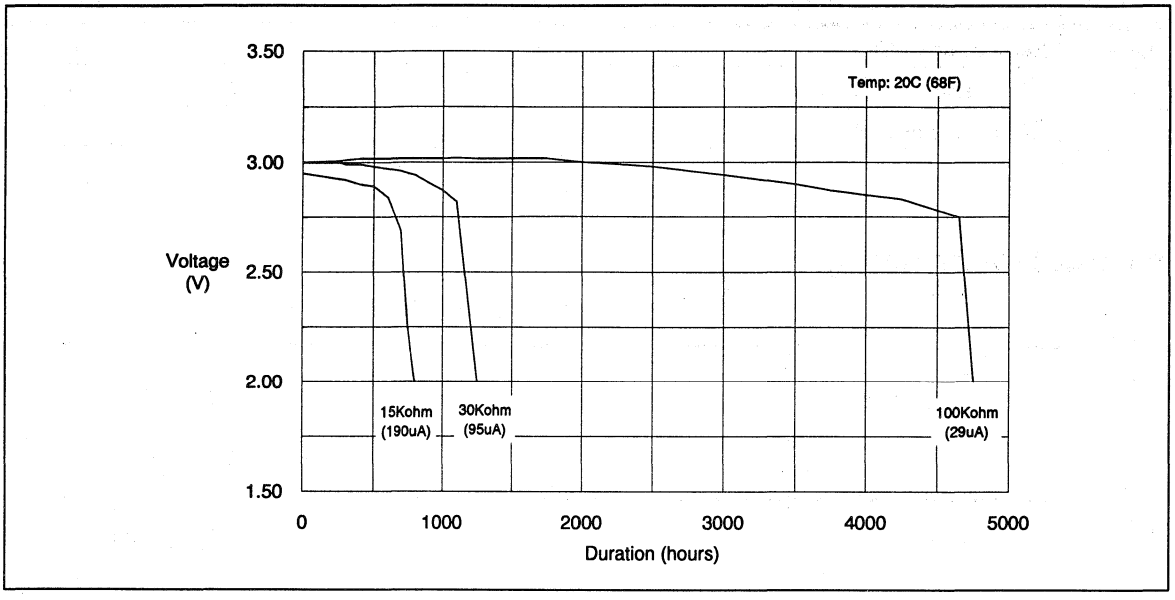
Interrupt Delay Timing



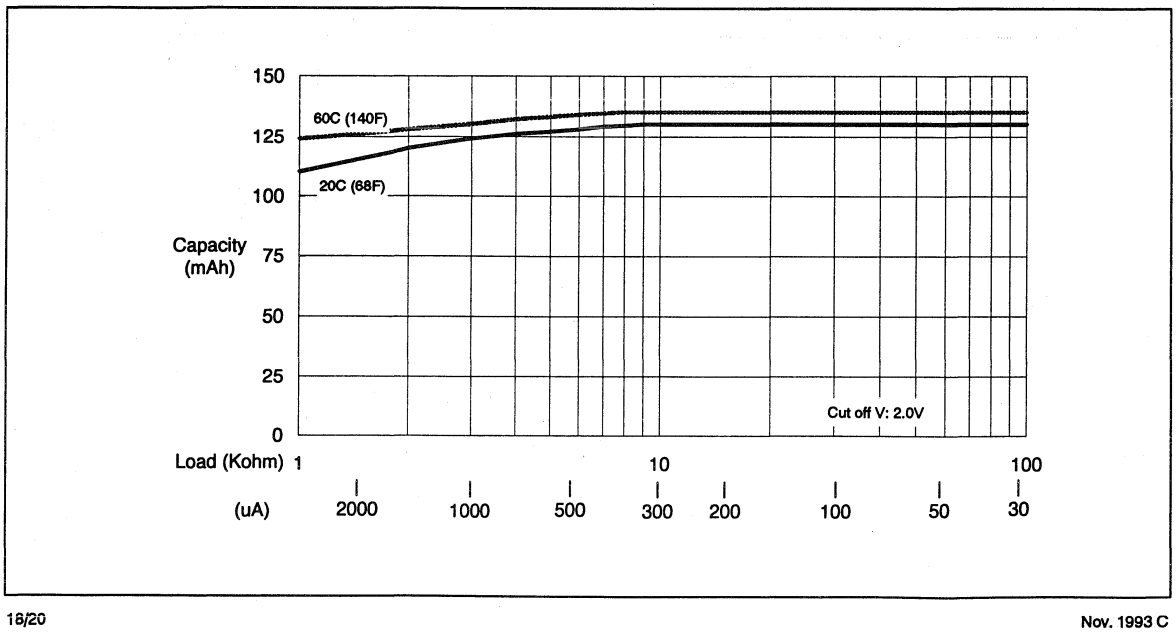
INT-3

Typical Battery Characteristics (source = Panasonic)

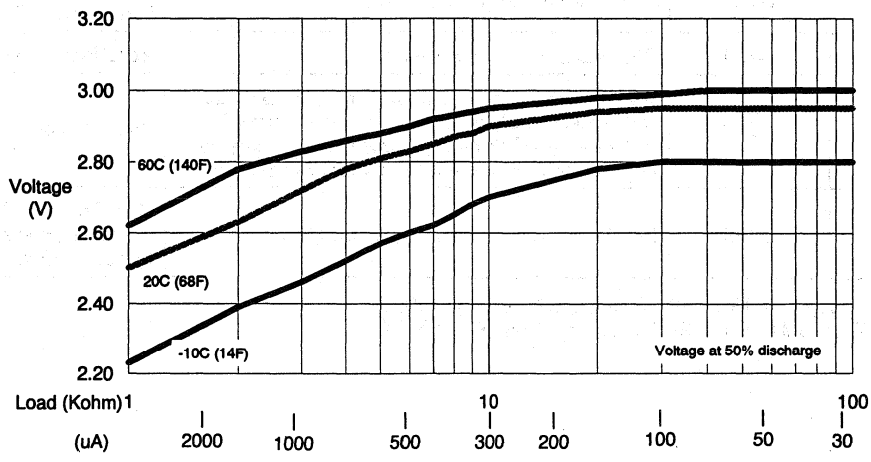
CR1632 Load Characteristics



CR1632 Capacity vs. Load Resistance



CR1632 Operating Voltage vs. Load Resistance



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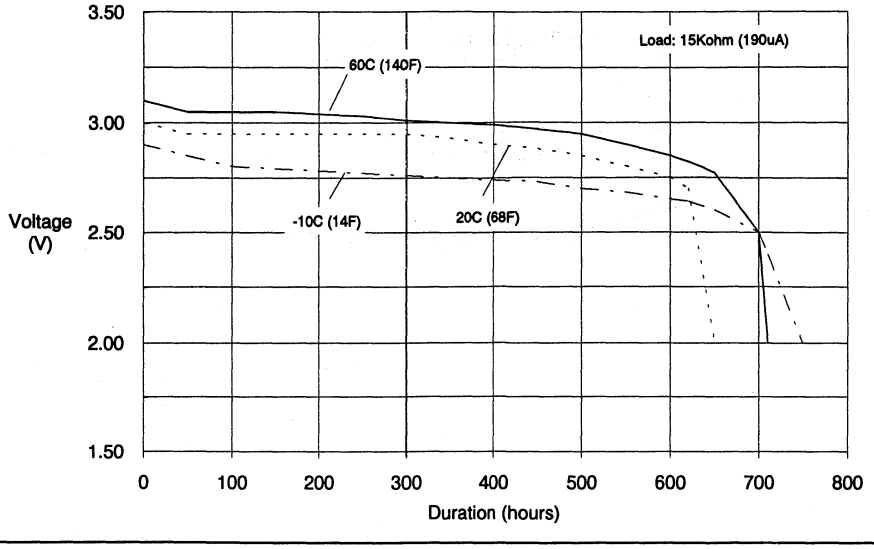
CR1632 Temperature Characteristics



Data Sheet Revision History

Change #	Page No.	Description	Nature of Change
1	4-136	Power-fail detect voltage V_{PFD}	Was 4.1 min, 4.25 max; is 4.0 min, 4.35 max
1	4-136	Chip enable input current	Additional specification
2	4-133	Was: "As shipped from Benchmarq, the backup cell is electrically isolated from the memory." Is: "As shipped from Benchmarq, the backup cell is electrically isolated from the active circuitry."	Clarification
2	4-138	Deleted specifications for t_{RWH} and t_{RWS}	Clarification; these parameters are not supported by the bq4287

Note: Change 1 = Nov. 1992 B changes from June 1991 A.
Change 2 = Nov. 1993 C changes from Nov. 1992 B.

Ordering Information

bq4287 MT -

- Temperature:
  blank = Commercial (0 to +70°C)
- Package Option:
  MT = T-type module
- Device:
  bq4287 Real-Time Clock Module With NVRAM Control

BENCHMARQ

Preliminary **bq4830Y**

RTC Module With 32Kx8 NVSRAM

Features

- Integrated low-power SRAM, real-time clock, crystal, power-fail control circuit, and battery
- Real-Time Clock counts hundredths of seconds through years in BCD format
- RAM-like clock access
- Pin-compatible with industry-standard 32K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Software clock calibration for greater accuracy

General Description

The bq4830Y RTC Module is a non-volatile 262,144-bit SRAM organized as 32,768 words by 8 bits with an integral accessible real-time clock.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 28-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

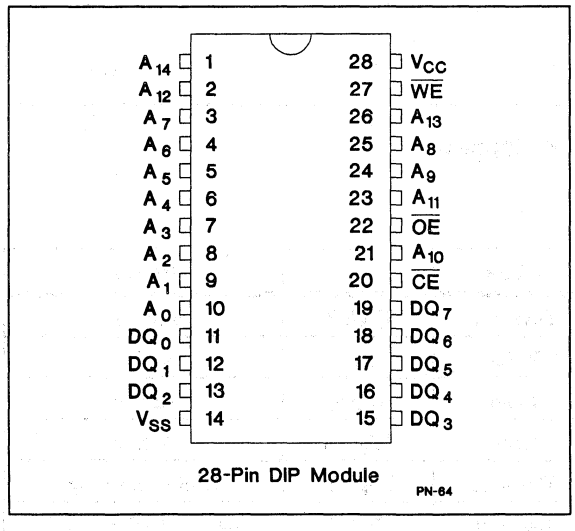
Registers for the real-time clock, alarm and other special functions are located in registers 7FF0h–7FF8h of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4830Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

4

Pin Connections



Pin Names

A_0–A_{14}	Address input
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_0–DQ_7	Data in/data out
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4830Y. The following sections describe the bq4830Y functional operation, including memory and clock interface, and data-retention modes.

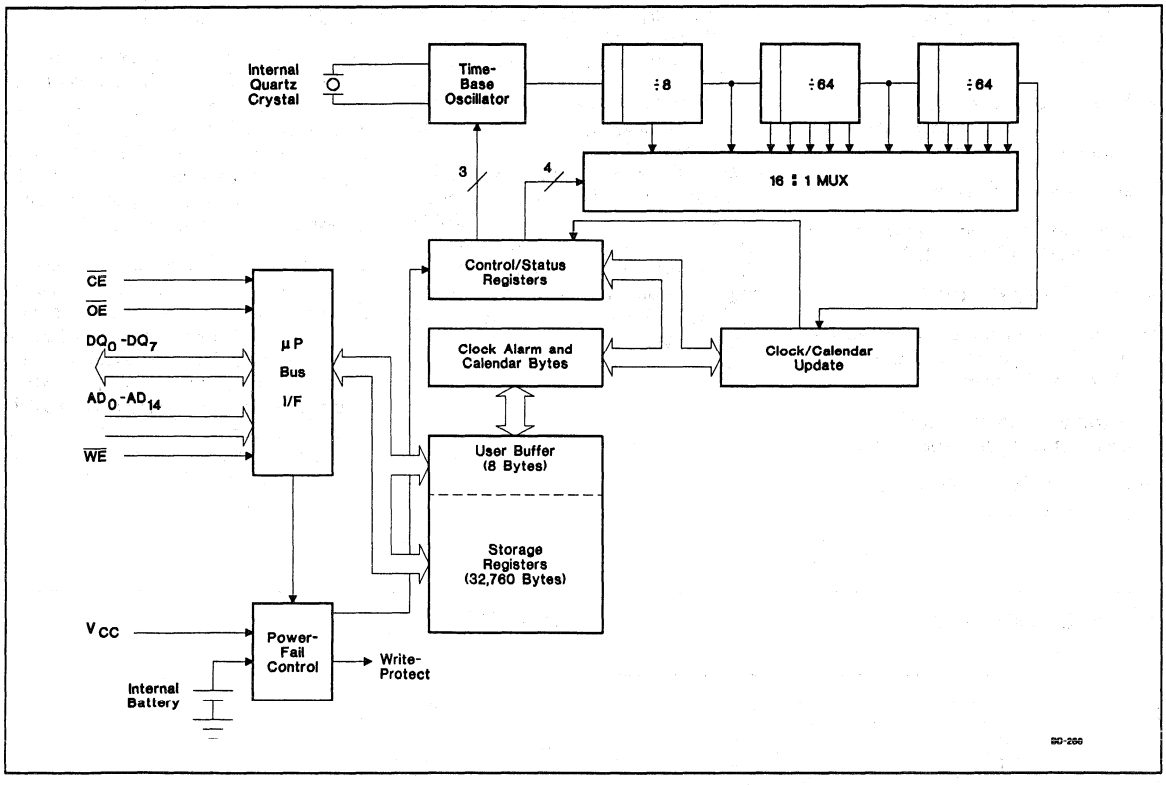


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	Deselect	High Z	Standby
> V_{CC} (min.)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backup mode

Address Map

The bq4830Y provides 8 bytes of clock and control status registers and 32,760 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4830Y. Table 1 is a map of the bq4830Y registers.

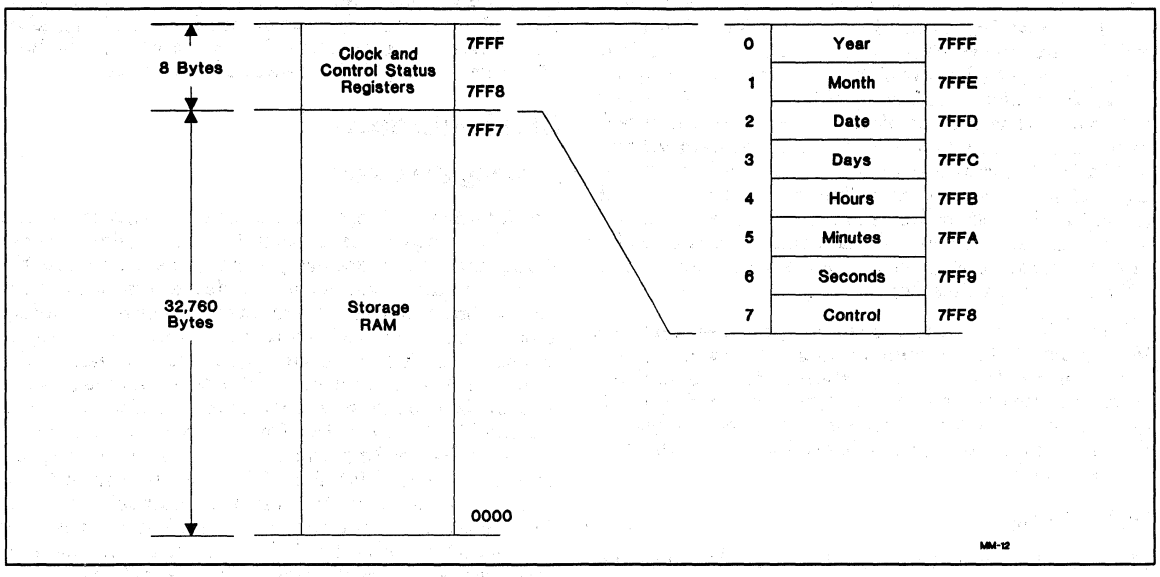


Figure 2. Address Map

Table 1. bq4830Y Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FFF	10 Years				Year				00–99	Year
7FFE	X	X	X	10 Month	Month				01–12	Month
7FFD	X	X	10 Date		Date				01–31	Date
7FFC	X	FTE	X	X	X	Day			01–07	Days
7FFB	X	X	10 Hours		Hours				00–23	Hours
7FFA	X	10 Minutes			Minutes				00–59	Minutes
7FF9	OSC	10 Seconds			Seconds				00–59	Seconds
7FF8	W	R	S	Calibration					00–31	Control

Note: X = Unused bits; unwritable and read as 0.

Memory Interface

Read Mode

The bq4830Y is in read mode whenever $\overline{WE}$ (write enable) is high and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4830Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Data-Retention Mode

With valid V_{CC} applied, the bq4830Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4830Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-protection continues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4830Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4830Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second.

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4830Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4830Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4830Y package along with the battery. The clock accuracy of the bq4830Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4830Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4830Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

The second approach uses a bq4830Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6*0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10*-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4830Y must be selected and held in an extended read of the seconds register, location 7FF9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

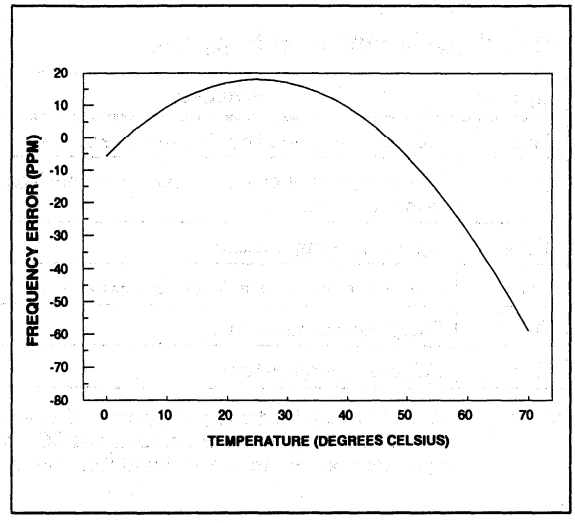


Figure 3. Frequency Error

4

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	$V_{CC} + 0.3$	V	

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2V
I_{CC}	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage	-	3	-	V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

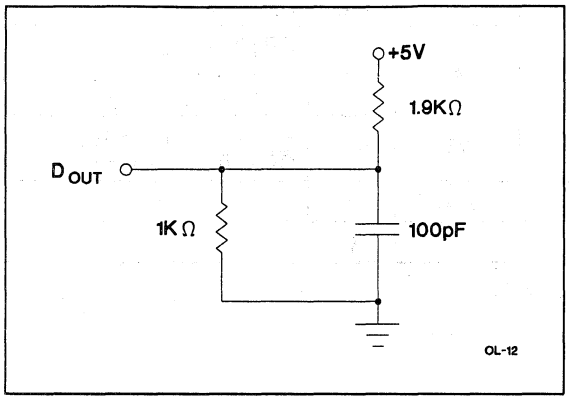


Figure 4. Output Load A

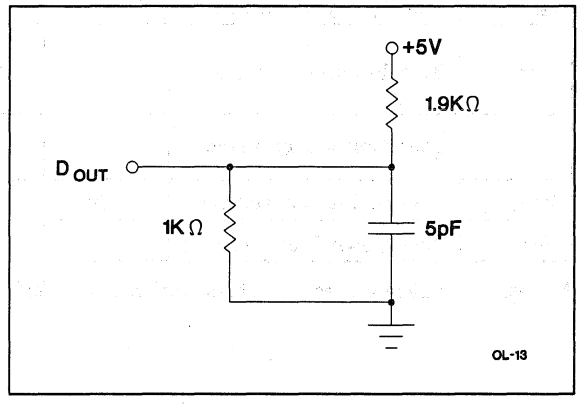
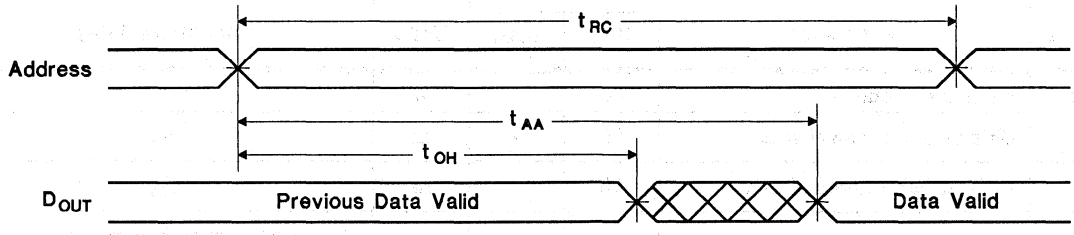


Figure 5. Output Load B

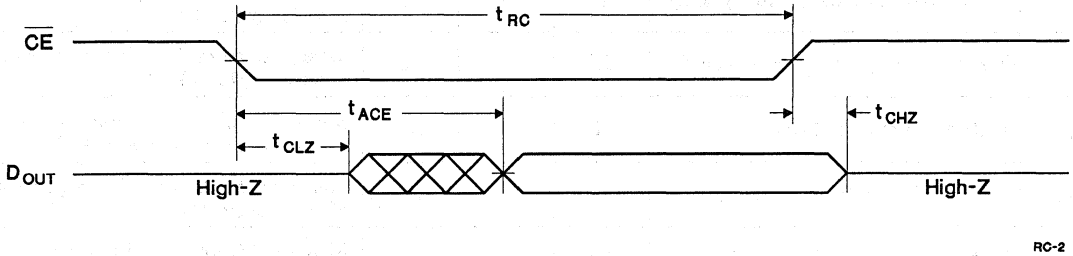
Read Cycle (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	85	-	ns	
t_{AA}	Address access time	-	85	ns	Output load A
t_{ACE}	Chip enable access time	-	85	ns	Output load A
t_{OE}	Output enable to output valid	-	45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

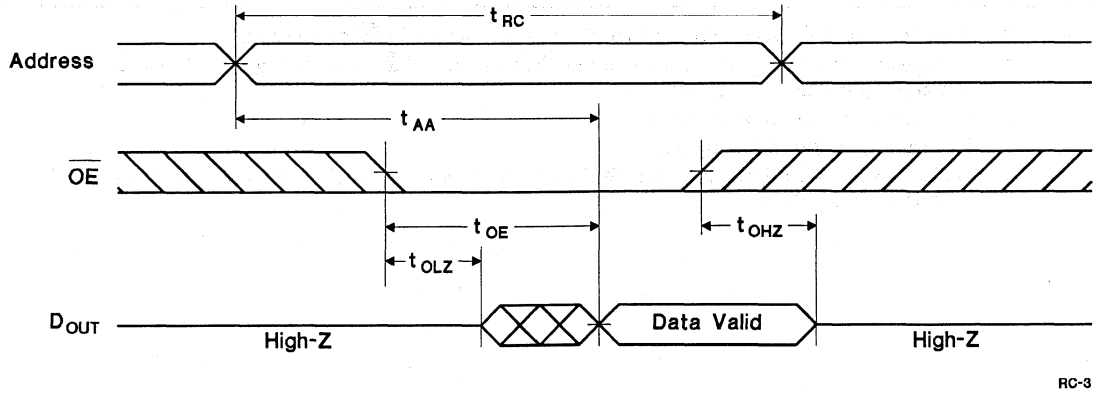
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

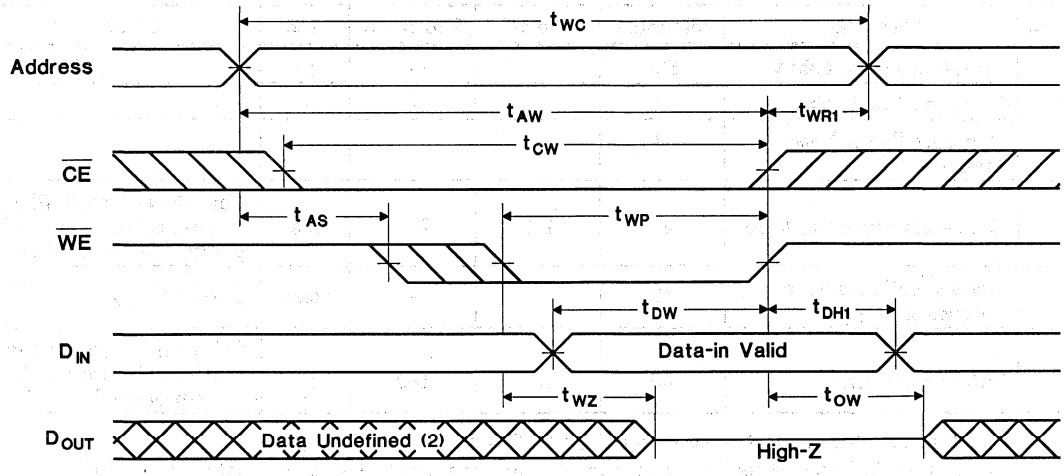
Write Cycle (TA =TOPR , VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	85	-	ns	
t_{CW}	Chip enable to end of write	75	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

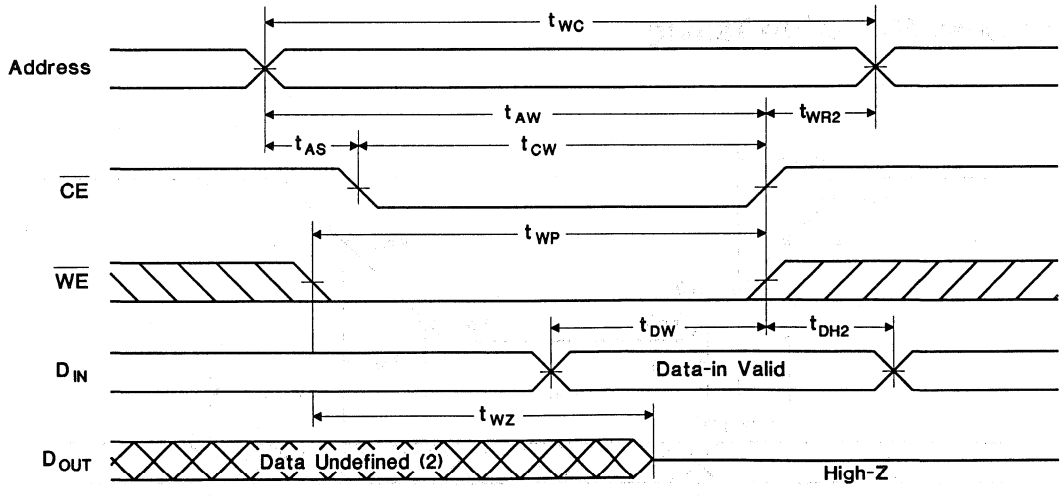
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

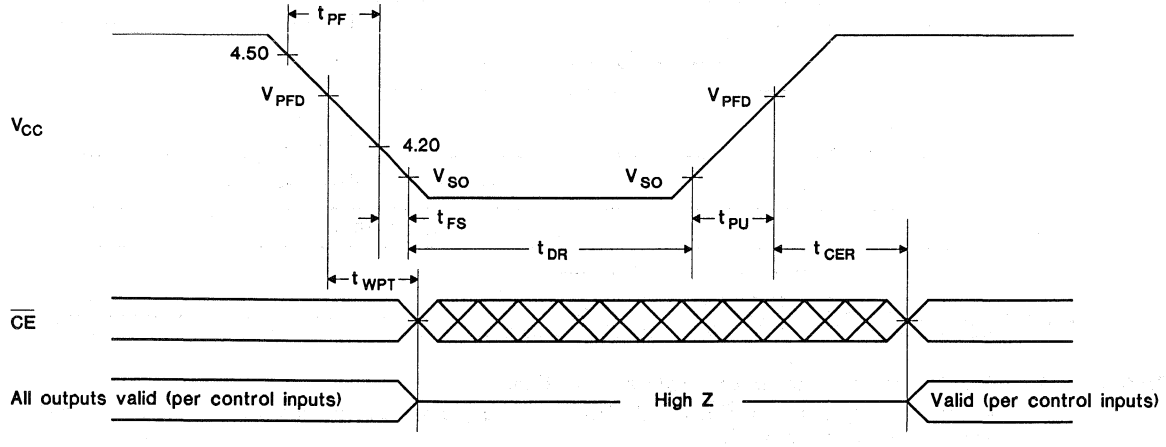
Power-Down/Power-Up Cycle ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	160	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

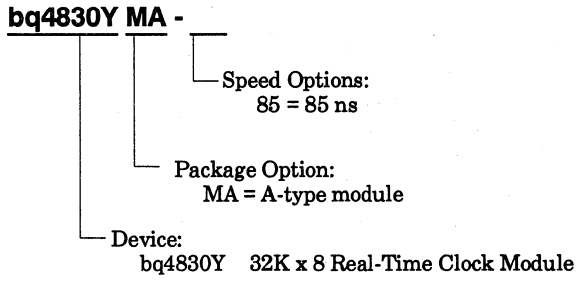
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-16

Ordering Information



4

Notes

BENCHMARQ

Preliminary **bq4832Y**

RTC Module With 32Kx8 NVSRAM

Features

- Integrated low-power SRAM, real-time clock, CPU supervisor, crystal, power-fail control circuit, and battery
- Real-Time Clock counts hundredths of seconds through years in BCD format
- RAM-like clock access
- Compatible with industry-standard 32K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Watchdog timer, power-on reset, alarm/periodic interrupt, power-fail and battery-low warning
- Software clock calibration for greater accuracy

General Description

The bq4832Y RTC Module is a non-volatile 262,144-bit SRAM organized as 32,768 words by 8 bits with an integral real-time clock and CPU supervisor. The CPU supervisor provides a programmable watchdog timer and a microprocessor reset. Other features include an alarm, power-fail and periodic interrupt, and a battery low warning.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 32-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

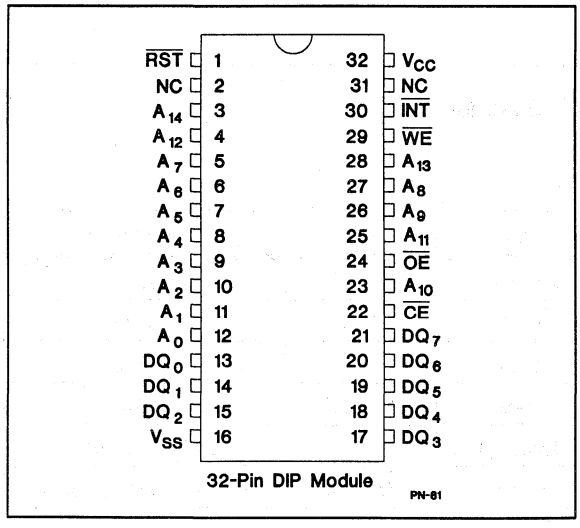
Registers for the real-time clock, alarm and other special functions are located in registers 7FE0h–7FEFh of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4832Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

4

Pin Connections



Pin Names

A_0–A_{14}	Address input
$\overline{CE}$	Chip enable
$\overline{RST}$	Power-on reset
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_0–DQ_7	Data in/data out
$\overline{INT}$	Programmable interrupt
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4832Y. The following sections describe the bq4832Y functional operation, including memory and clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

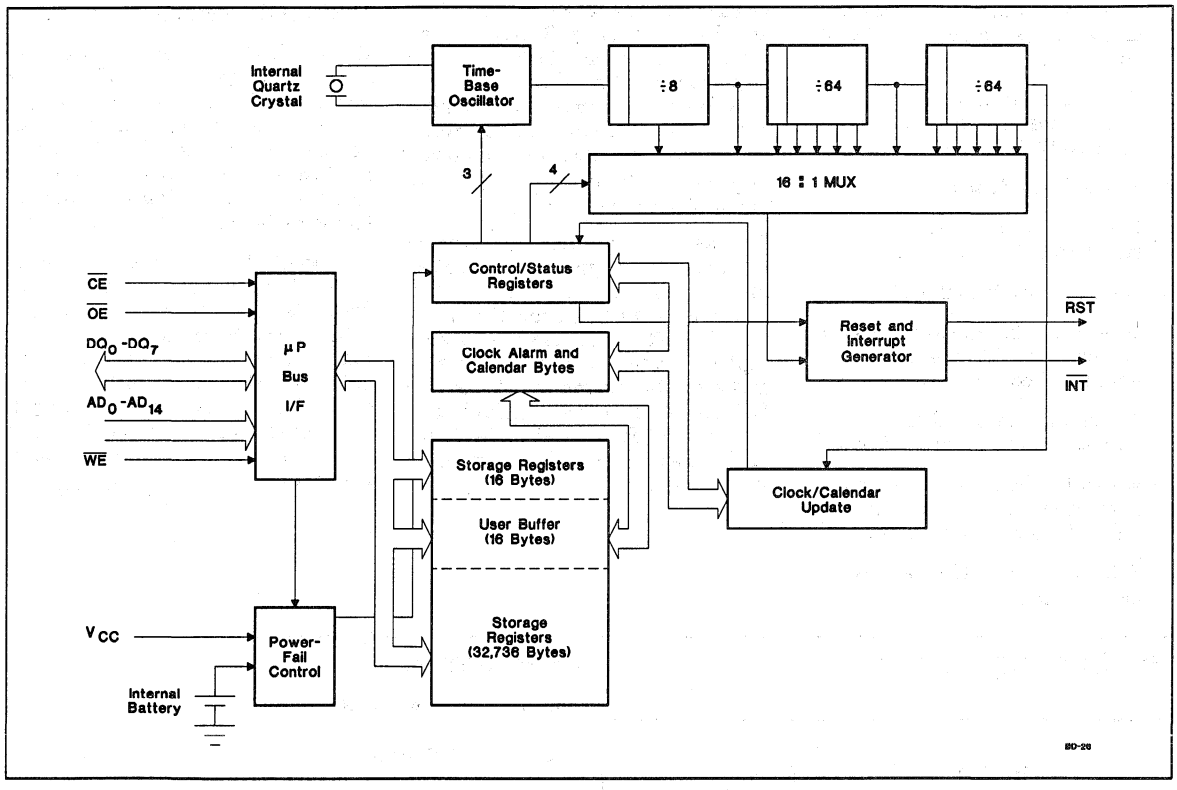


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
> V_{CC} (min.)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backup mode

Address Map

The bq4832Y provides 16 bytes of clock and control status registers and 32,752 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4832Y. Table 1 is a map of the bq4832Y registers, and Table 2 describes the register bits.

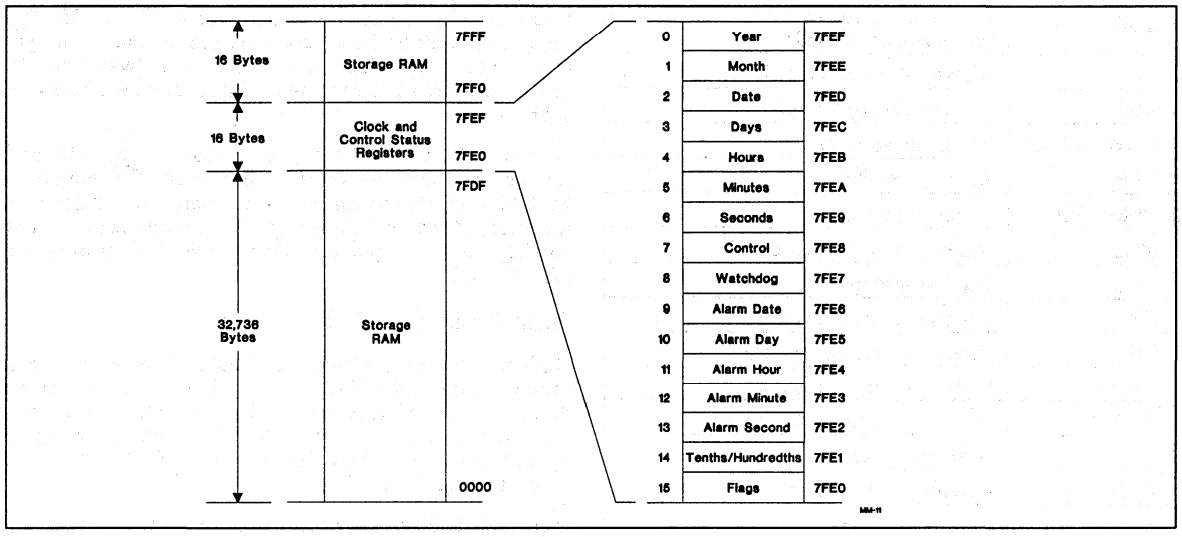


Figure 2. Address Map

Table 1. bq4832Y Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FEF	10 Years				Year				00–99	Year
7FEE	X	X	X	10 Month	Month				01–12	Month
7FED	X	X	10 Date		Date				01–31	Date
7FEC	X	FTE	X	X	X	Day			01–07	Days
7FEB	X	X	10 Hours		Hours				00–23	Hours
7FEA	X	10 Minutes			Minutes				00–59	Minutes
7FE9	OSC	10 Seconds			Seconds				00–59	Seconds
7FE8	W	R	S	Calibration					00–31	Control
7FE7	WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0		Watchdog
7FE6	AIE	PIE	ABE	PWRIE	RS3	RS2	RS1	RS0		Interrupts
7FE5	ALM3	X	X	X	X	Alarm days			01–07/81–87	Alarm date
7FE4	ALM2	X	10-hour alarm		Alarm hours				00–23/80–A3	Alarm hours
7FE3	ALM1	Alarm 10 minutes			Alarm minutes				00–59/80–D9	Alarm minutes
7FE2	ALM0	Alarm 10 seconds			Alarm seconds				00–59/80–D9	Alarm seconds
7FE1	0.1 seconds				0.01 seconds				00–99	0.1/0.01 seconds
7FE0	WDF	AF	PF	BLF	PWRF	X	X	X		Flags

Note: X = Unused bits; unwriteable and read as 0.

Table 2. Clock and Control Register Bits

Bits	Description
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM3	Alarm repeat rate
BLF	Battery-low flag
BM0–BM4	Watchdog multiplier
FTE	Frequency test mode enable
OSC	Oscillator stop
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
R	Read clock enable
RS0–RS3	Periodic interrupt rate
S	Calibration sign
W	Write clock enable
WD0–WD1	Watchdog resolution
WDF	Watchdog flag
WDS	Watchdog steering

Memory Interface

Read Mode

The bq4832Y is in read mode whenever $\overline{WE}$ (write enable) is high and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4832Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Data-Retention Mode

With valid V_{CC} applied, the bq4832Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4832Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-protection continues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4832Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4832Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters.

Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second.

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4832Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4832Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4832Y package along with the battery. The clock accuracy of the bq4832Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4832Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4832Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

The second approach uses a bq4832Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6*0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10*-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4832Y must be selected and held in an extended read of the seconds register, location 7FE9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

Power-On Reset

The bq4832Y provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for T_{CER} after V_{CC} passes V_{PFD}.

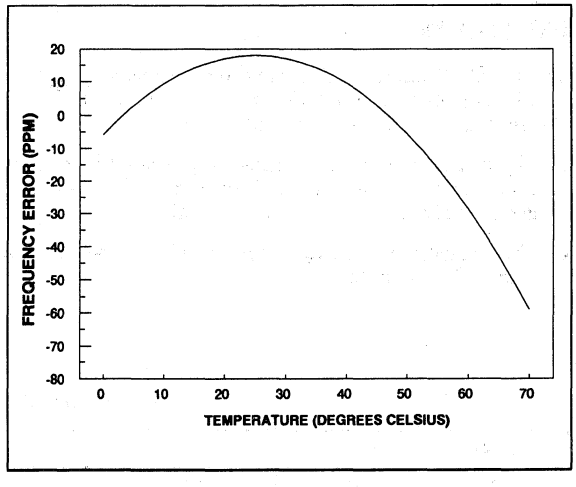


Figure 3. Frequency Error

Watchdog Timer

The watchdog circuit monitors the microprocessor's activity. If the processor does not reset the watchdog timer within the programmed time-out period, the circuit asserts the $\overline{INT}$ or $\overline{RST}$ pin. The watchdog timer is activated by writing the desired time-out period into the eight-bit watchdog register described in Table 3 (device address 7FE7). The five bits (BM4–BM0) store a binary multiplier, and the two lower-order bits (WD1–WD0) select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds.

The time-out period is the multiplication of the five-bit multiplier with the two-bit resolution. For example, writing 00011 in BM4–BM0 and 10 in WD1–WD0 results in a total time-out setting of 3 x 1 or 3 seconds. A multiplier of zero disables the watchdog circuit. Bit 7 of the watchdog register (WDS) is the watchdog steering bit. When WDS is set to a 1 and a time-out occurs, the watchdog asserts a reset pulse for t_{CER} on the $\overline{RST}$ pin. During the reset pulse, the watchdog register is cleared to all zeros disabling the watchdog. When WDS is set to a 0, the watchdog asserts the $\overline{INT}$ pin on a time-out. The $\overline{INT}$ pin remains low until the watchdog is reset by the microprocessor or a power failure occurs. Additionally, when the watchdog times out, the watchdog flag bit (WDF) in the flags register, location 7FE0, is set.

To reset the watchdog timer, the microprocessor must write to the watchdog register. After being reset by a write, the watchdog time-out period starts over. As a precaution, the watchdog circuit is disabled on a power failure. The user must, therefore, set the watchdog at boot-up for activation.

Interrupts

The bq4832Y allows four individually selected interrupt events to generate an interrupt request on the $\overline{INT}$ pin. These four interrupt events are:

- The watchdog timer interrupt, programmable to occur according to the time-out period and conditions described in the watchdog timer section
- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per year
- The power-fail interrupt, which can be enabled to be asserted when the bq4832Y detects a power failure

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register 7FE6, the interrupts register. When an event occurs, its event flag bit in the flags register, location 7FE0, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4832Y addresses must be held stable at location 7FE0 for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4832Y sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Alarm Interrupt

Registers 7FE5–7FE2 program the real-time clock alarm. During each update cycle, the bq4832Y compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags register. ALM3–ALM0 puts the alarm into a periodic mode of operation. Table 5 describes the selectable rates.

The alarm interrupt can be made active while the bq4832Y is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin tri-states during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit is set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can read the flags register during boot-up to determine if an alarm was generated during power-on reset.

Table 3. Watchdog Register Bits

MSB			Bits				LSB
7	6	5	4	3	2	1	0
WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0

Power-Fail Interrupt

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4832Y generates a reset and deselects. The PWRIE bit is cleared on power-up.

Battery-Low Warning

The bq4832Y checks the internal battery on power-up. If the battery voltage is below 2.4V, the battery-low flag BLF in the flags register is set to a 1 indicating that clock and RAM data may be invalid.

Table 5. Alarm Frequency (Alarm Bits DQ7

ALM3	ALM2	ALM1	ALM0	Alarm Frequency
1	1	1	1	Once per second
1	1	1	0	Once per minute when seconds match
1	1	0	0	Once per hour when minutes, and seconds match
1	0	0	0	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

Table 4. Periodic Rates

RS3	RS2	RS1	RS0	Interrupt Rate
0	0	0	0	None
0	0	0	1	10ms
0	0	1	0	100ms
0	0	1	1	122.07µs
0	1	0	0	244.14µs
0	1	0	1	488.281µs
0	1	1	0	976.5625
0	1	1	1	1.953125ms
1	0	0	0	3.90625ms
1	0	0	1	7.8125ms
1	0	1	0	15.625ms
1	0	1	1	21.25ms
1	1	0	0	62.5ms
1	1	0	1	125ms
1	1	1	0	250ms
1	1	1	1	500ms

4

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{OD}	$\overline{RST}$, $\overline{INT}$ sink current	10	-	-	mA	V_{OL} = 0.4V
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2V
I_{CC}	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage	-	3	-	V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

Capacitance (TA = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

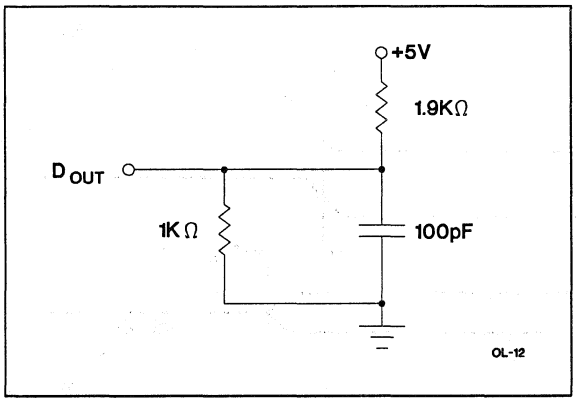


Figure 4. Output Load A

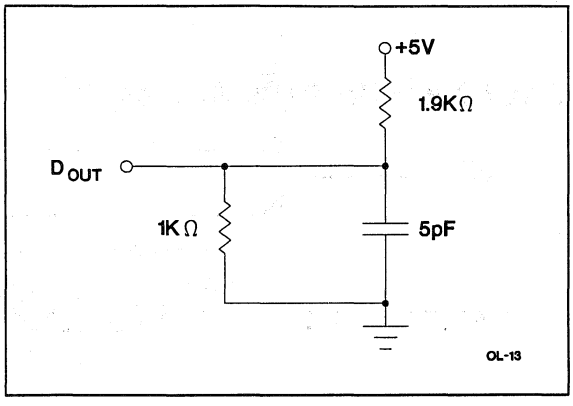


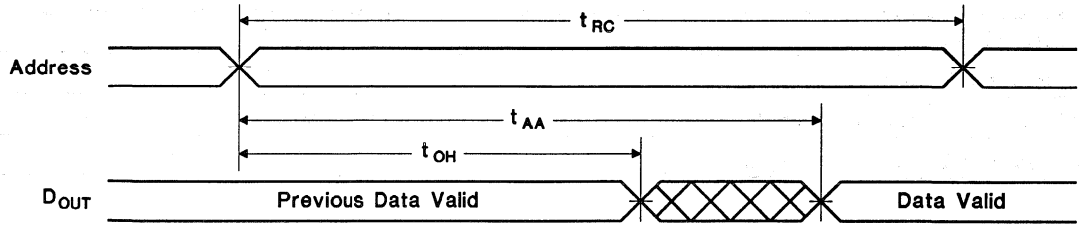
Figure 5. Output Load B

4

Read Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

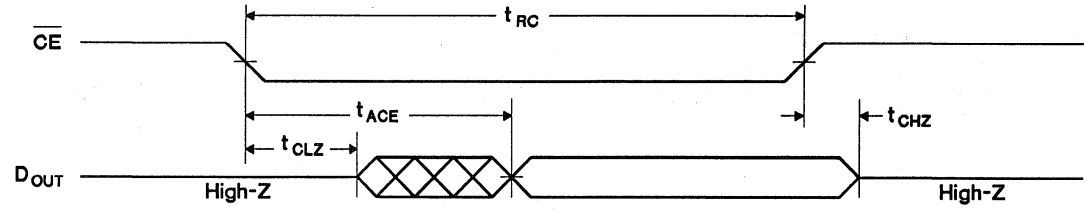
Symbol	Parameter	-85		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	85	-	ns	
t_{AA}	Address access time	-	85	ns	Output load A
t_{ACE}	Chip enable access time	-	85	ns	Output load A
t_{OE}	Output enable to output valid	-	45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



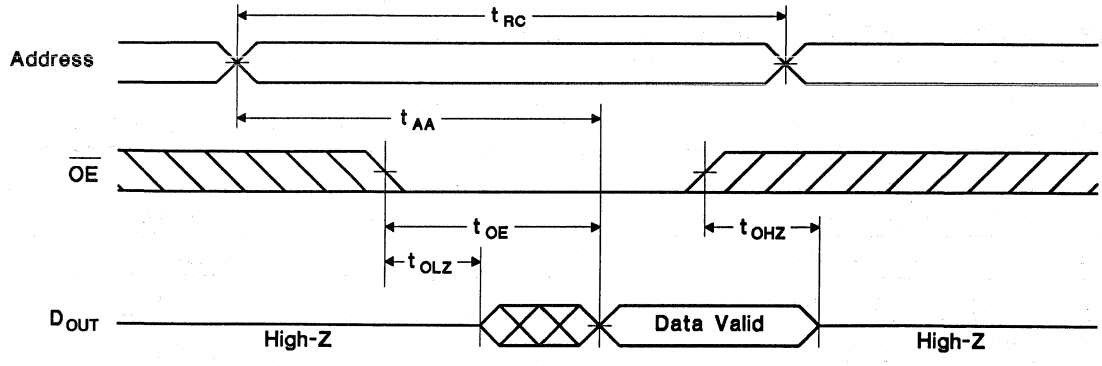
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

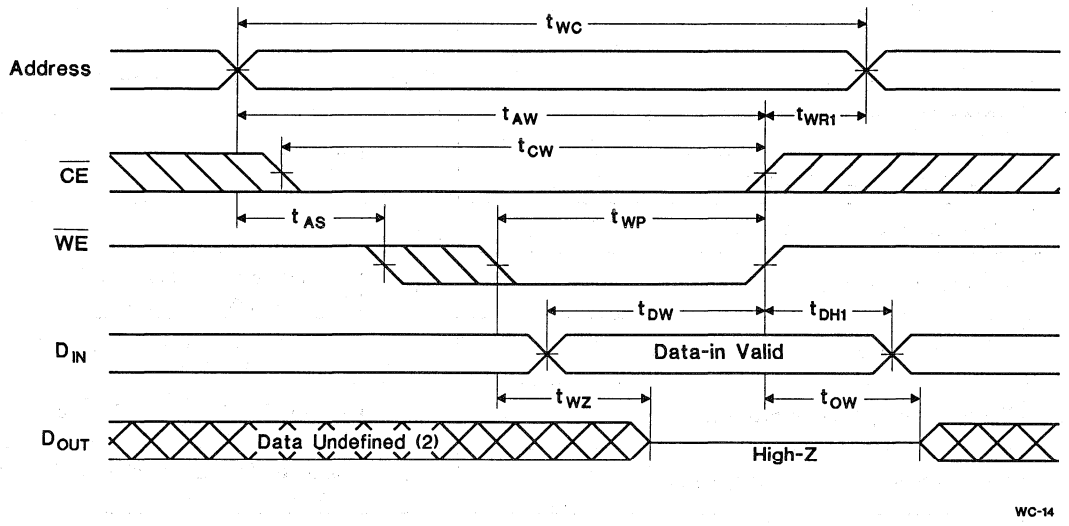
Symbol	Parameter	-85		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	85	-	ns	
t_{CW}	Chip enable to end of write	75	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

Notes:

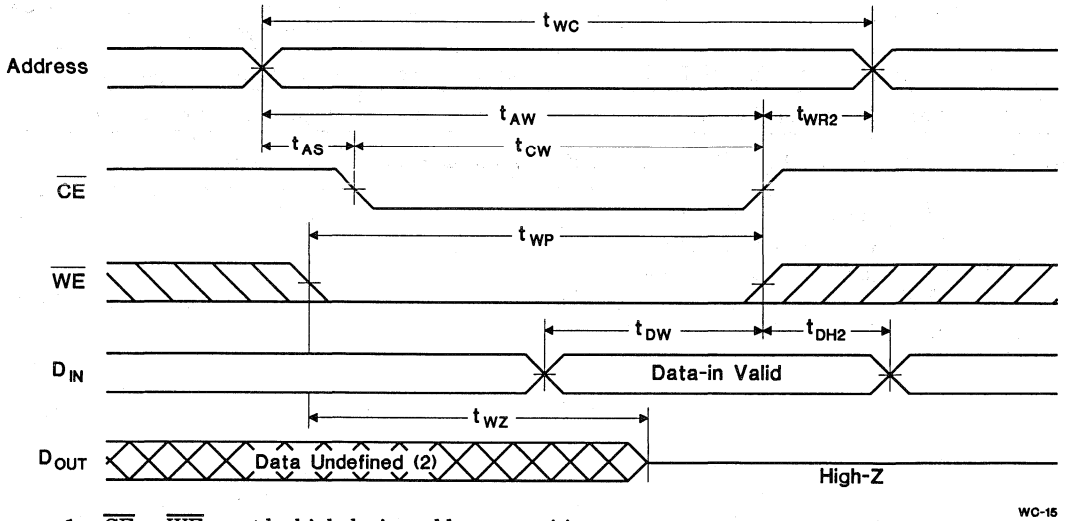
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

4

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

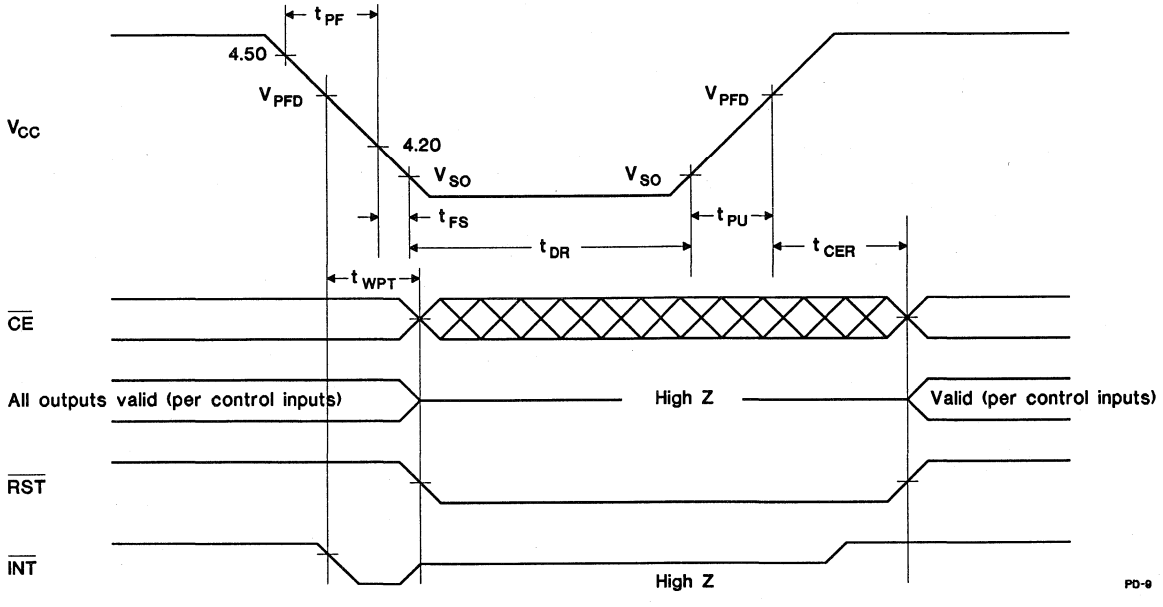
Power-Down/Power-Up Cycle (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	160	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

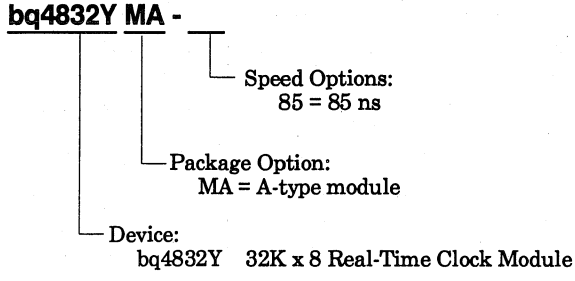
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



Notes:
1. PWRIE is set to "1" to enable power fail interrupt.
2. $\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

Ordering Information



BENCHMARQ

Preliminary **bq4842Y**

RTC Module With 128Kx8 NVSRAM

Features

- Integrated low-power SRAM, real-time clock, CPU supervisor, crystal, power-fail control circuit, and battery
- Real-Time Clock counts hundredths of seconds through years in BCD format
- RAM-like clock access
- Compatible with industry-standard 128K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Watchdog timer, power-on reset, alarm/periodic interrupt, power-fail and battery-low warning
- Software clock calibration for greater accuracy

General Description

The bq4842Y RTC Module is a non-volatile 1,048,576-bit SRAM organized as 131,072 words by 8 bits with an integral accessible real-time clock and CPU supervisor. The CPU supervisor provides a programmable watchdog timer and a microprocessor reset. Other features include an alarm, power-fail, and periodic interrupt and a battery low warning.

The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 32-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

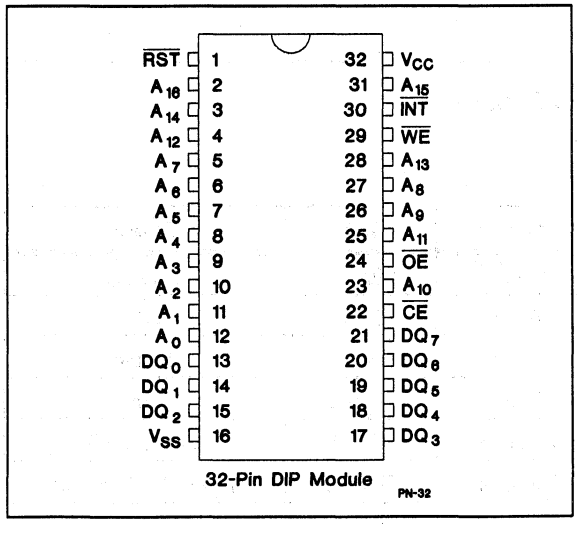
Registers for the real-time clock, alarm and other special functions are located in registers 1FFE0h–1FFEFh of the memory array.

The clock and alarm registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4842Y also contains a power-fail-detect circuit. The circuit deselects the device whenever V_{CC} falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of V_{CC}.

4

Pin Connections



32-Pin DIP Module PN-32

Pin Names

A_0–A_{16}	Address input
$\overline{CE}$	Chip enable
$\overline{RST}$	Power-on reset
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_0–DQ_7	Data in/data out
$\overline{INT}$	Programmable interrupt
V_{CC}	+5 volts
V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4842Y. The following sections describe the bq4842Y functional operation, including memory and clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

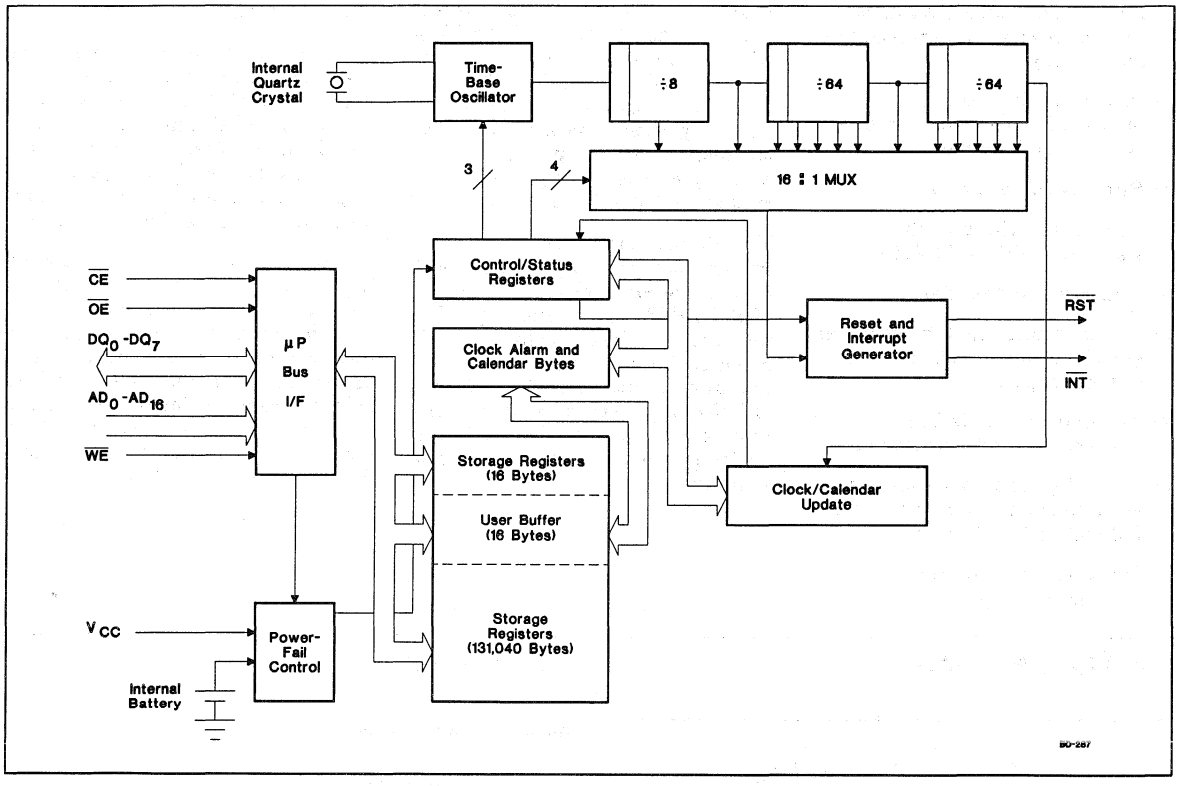


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	Deselect	High Z	Standby
> V_{CC} (min.)	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery-backup mode

Address Map

The bq4842Y provides 16 bytes of clock and control status registers and 131,056 bytes of storage RAM.

Figure 2 illustrates the address map for the bq4842Y. Table 1 is a map of the bq4842Y registers, and Table 2 describes the register bits.

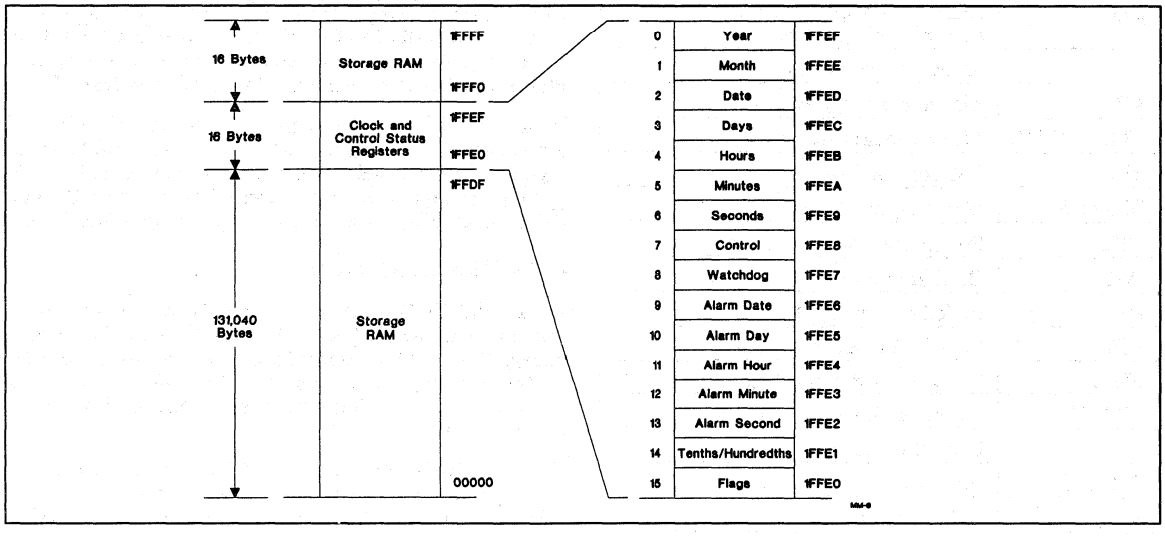


Figure 2. Address Map

Table 1. bq4842 Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
1FFEF	10 Years				Year				00–99	Year
1FFEE	X	X	X	10 Month	Month				01–12	Month
1FFED	X	X	10 Date		Date				01–31	Date
1FFEC	X	FTE	X	X	X	Day			01–07	Days
1FFEB	X	X	10 Hours		Hours				00–23	Hours
1FFEA	X	10 Minutes			Minutes				00–59	Minutes
1FFE9	OSC	10 Seconds			Seconds				00–59	Seconds
1FFE8	W	R	S	Calibration					00–31	Control
1FFE7	WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0		Watchdog
1FFE6	AIE	PIE	ABE	PWRIE	RS3	RS2	RS1	RS0		Interrupts
1FFE5	ALM3	X	X	X	X	Alarm days			01–07/81–87	Alarm date
1FFE4	ALM2	X	10-hour alarm		Alarm hours				00–23/80–A3	Alarm hours
1FFE3	ALM1	Alarm 10 minutes			Alarm minutes				00–59/80–D9	Alarm minutes
1FFE2	ALM0	Alarm 10 seconds			Alarm seconds				00–59/80–D9	Alarm seconds
1FFE1	0.1 seconds				0.01 seconds				00–99	0.1/0.01 seconds
1FFE0	WDF	AF	PF	BLF	PWRF	X	X	X		Flags

Note: X = Unused bits; unwritable and read as 0.

Table 2. Clock and Control Register Bits

Bits	Description
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM3	Alarm repeat rate
BLF	Battery-low flag
BM0–BM4	Watchdog multiplier
FTE	Frequency test mode enable
OSC	Oscillator stop
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
R	Read clock enable
RS0–RS3	Periodic interrupt rate
S	Calibration sign
W	Write clock enable
WD0–WD1	Watchdog resolution
WDF	Watchdog flag
WDS	Watchdog steering

Memory Interface

Read Mode

The bq4842Y is in read mode whenever $\overline{WE}$ (write enable) is high and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 address inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data is available at the data I/O pins within t_{AA} (address access time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If the $\overline{CE}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip enable access time (t_{ACE}) or output enable access time (t_{OE}).

$\overline{CE}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4842Y is in write mode whenever $\overline{WE}$ and $\overline{CE}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CE}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CE}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CE}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Data-Retention Mode

With valid VCC applied, the bq4842Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself t_{WPT} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4842Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write-protection continues for t_{CER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{CER}, normal RAM operation can resume.

Clock Interface

Reading the Clock

The interface to the clock and control registers of the bq4842Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4842Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on

accuracy. Once the read bit is reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second.

Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4842Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmarq factory.

Calibrating the Clock

The bq4842Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4842Y package along with the battery. The clock accuracy of the bq4842Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4842Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4842Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

The second approach uses a bq4842Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a (1E6*0.01024)/512 or +20 ppm oscillator frequency error, requiring ten steps of negative calibration (10*-2.034 or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4842Y must be selected and held in an extended read of the seconds register, location 1FFE9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

Power-On Reset

The bq4842Y provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for t_{CER} after V_{CC} passes V_{PFD}.

Watchdog Timer

The watchdog circuit monitors the microprocessor's activity. If the processor does not reset the watchdog timer within the programmed time-out period, the circuit asserts the $\overline{INT}$ or $\overline{RST}$ pin. The watchdog timer is activated by writing the desired time-out period into the eight-bit watchdog register described in Table 3 (device

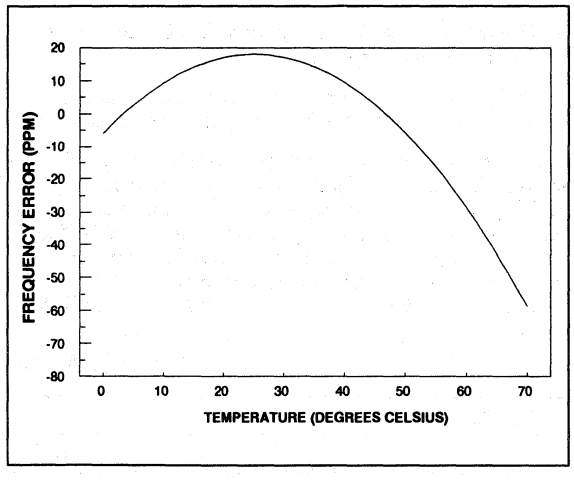


Figure 3. Frequency Error

address 1FFE7). The five bits (BM4–BM0) store a binary multiplier, and the two lower-order bits (WD1–WD0) select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds.

The time-out period is the multiplication of the five-bit multiplier with the two-bit resolution. For example, writing 00011 in BM4–BM0 and 10 in WD1–WD0 results in a total time-out setting of 3 x 1 or 3 seconds. A multiplier of zero disables the watchdog circuit. Bit 7 of the watchdog register (WDS) is the watchdog steering bit. When WDS is set to a 1 and a time-out occurs, the watchdog asserts a reset pulse for t_{CER} on the $\overline{RST}$ pin. During the reset pulse, the watchdog register is cleared to all zeros disabling the watchdog. When WDS is set to a 0, the watchdog asserts the $\overline{INT}$ pin on a time-out. The $\overline{INT}$ pin remains low until the watchdog is reset by the microprocessor or a power failure occurs. Additionally, when the watchdog times out, the watchdog flag bit (WDF) in the flags register, location 1FFE0, is set.

To reset the watchdog timer, the microprocessor must write to the watchdog register. After being reset by a write, the watchdog time-out period starts over. As a precaution, the watchdog circuit is disabled on a power failure. The user must, therefore, set the watchdog at boot-up for activation.

Interrupts

The bq4842Y allows four individually selected interrupt events to generate an interrupt request on the $\overline{INT}$ pin. These four interrupt events are:

- The watchdog timer interrupt, programmable to occur according to the time-out period and conditions described in the watchdog timer section
- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per year
- The power-fail interrupt, which can be enabled to be asserted when the bq4842Y detects a power failure

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register 1FFE6, the interrupts register. When an event occurs, its event flag bit in the flags register, location 1FFE0, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4842Y addresses must be held stable at location 1FFE0 for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4842Y sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Alarm Interrupt

Registers 1FFE5–1FFE2 program the real-time clock alarm. During each update cycle, the bq4842Y compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags register. ALM3–ALM0 puts the alarm into a periodic mode of operation. Table 5 describes the selectable rates.

The alarm interrupt can be made active while the bq4842Y is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin tri-states during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit is set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can read the flags register during boot-up to determine if an alarm was generated during power-on reset.

Power-Fail Interrupt

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4842Y generates a reset and deselects. The PWIE bit is cleared on power-up.

Battery-Low Warning

The bq4842Y checks the internal battery on power-up. If the battery voltage is below 2.4V, the battery-low flag BLF in the flags register is set to a 1 indicating that clock and RAM data may be invalid.

Table 3. Watchdog Register Bits

MSB			Bits				LSB
7	6	5	4	3	2	1	0
WDS	BM4	BM3	BM2	BM1	BM0	WD1	WD0

Table 4. Periodic Rates

RS3	RS2	RS1	RS0	Interrupt Rate
0	0	0	0	None
0	0	0	1	10ms
0	0	1	0	100ms
0	0	1	1	122.07µs
0	1	0	0	244.14µs
0	1	0	1	488.281
0	1	1	0	976.5625
0	1	1	1	1.953125ms
1	0	0	0	3.90625ms
1	0	0	1	7.8125ms
1	0	1	0	15.625ms
1	0	1	1	21.25ms
1	1	0	0	62.5ms
1	1	0	1	125ms
1	1	1	0	250ms
1	1	1	1	500ms

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Table 5. Alarm Frequency (Alarm Bits DQ7 of Alarm Registers)

ALM3	ALM2	ALM1	ALM0	Alarm Frequency
1	1	1	1	Once per second
1	1	1	0	Once per minute when seconds match
1	1	0	0	Once per hour when minutes, and seconds match
1	0	0	0	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature (V_{CC} off; oscillator off)	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{OD}	$\overline{RST}$, $\overline{INT}$ sink current	10	-	-	mA	V_{OL} = 0.4V
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	75	105	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	
V_{SO}	Supply switch-over voltage	-	3	-	V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

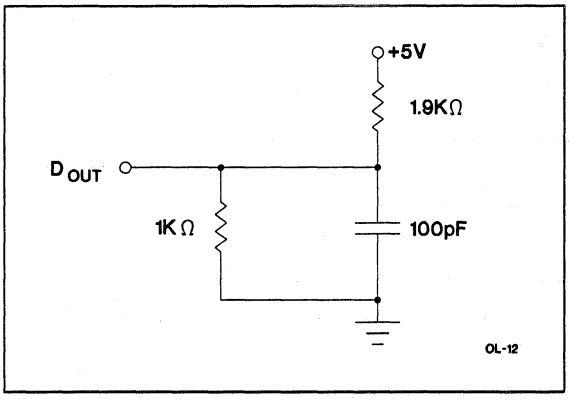

Figure 4. Output Load A

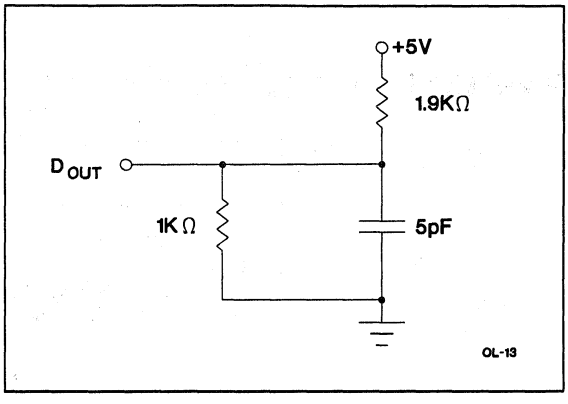

Figure 5. Output Load B

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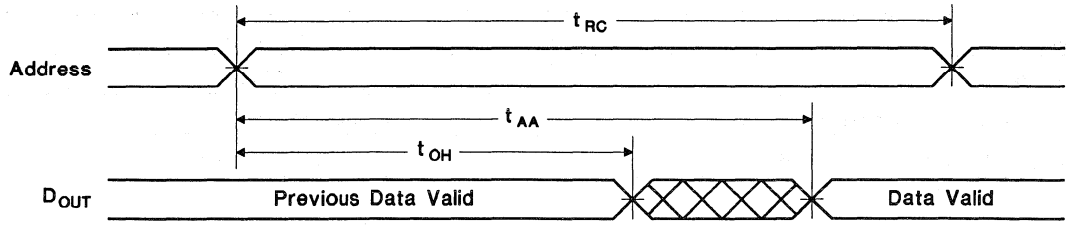
Read Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

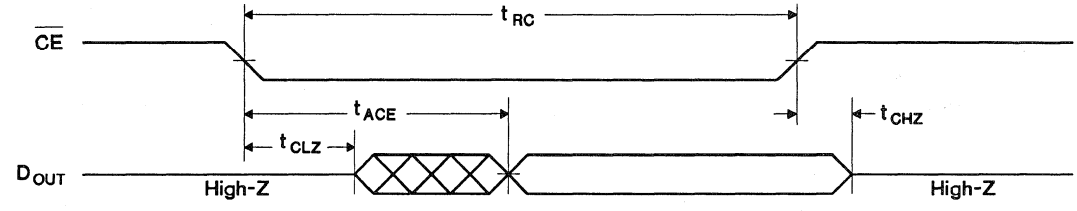
Symbol	Parameter	-85		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	85	-	ns	
t_{AA}	Address access time	-	85	ns	Output load A
t_{ACE}	Chip enable access time	-	85	ns	Output load A
t_{OE}	Output enable to output valid	-	45	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



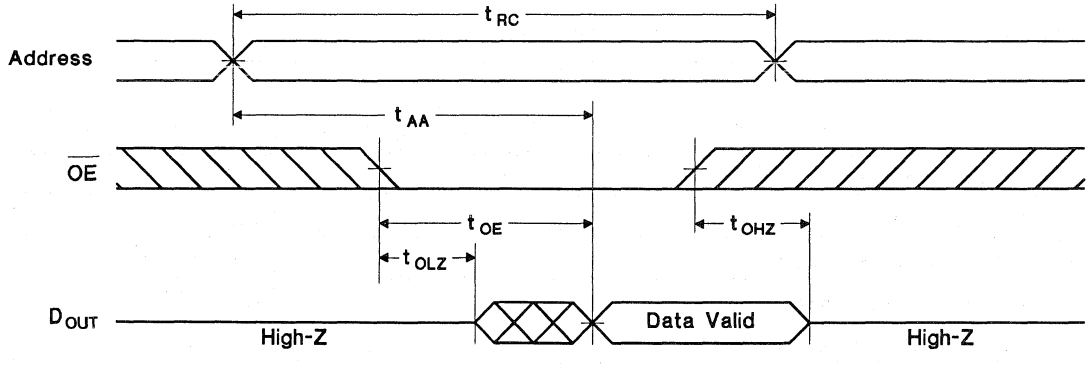
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	-85		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	85	-	ns	
t_{CW}	Chip enable to end of write	75	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

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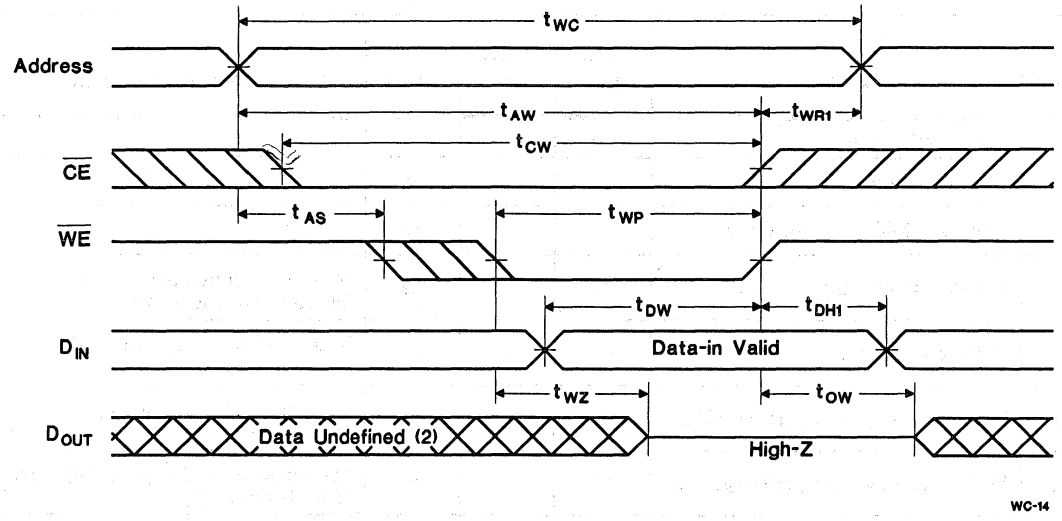
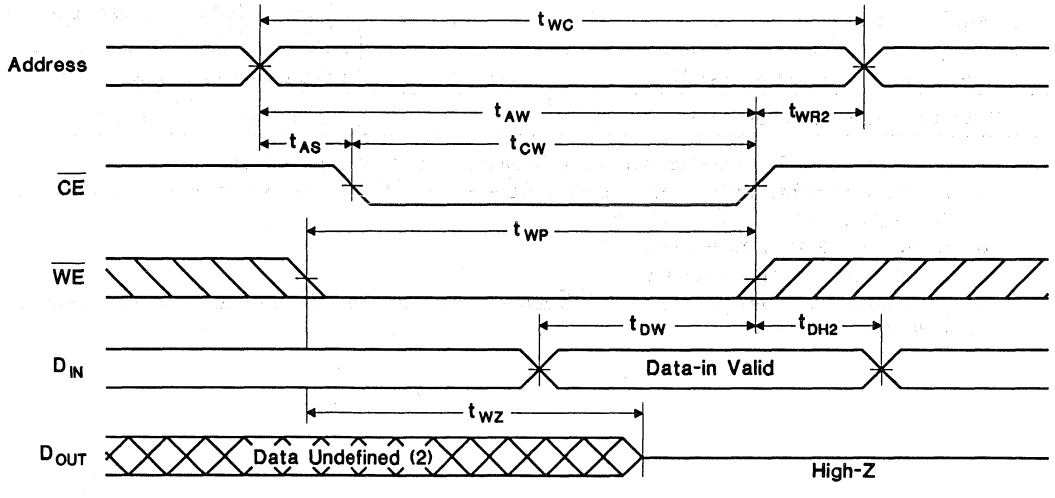
Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

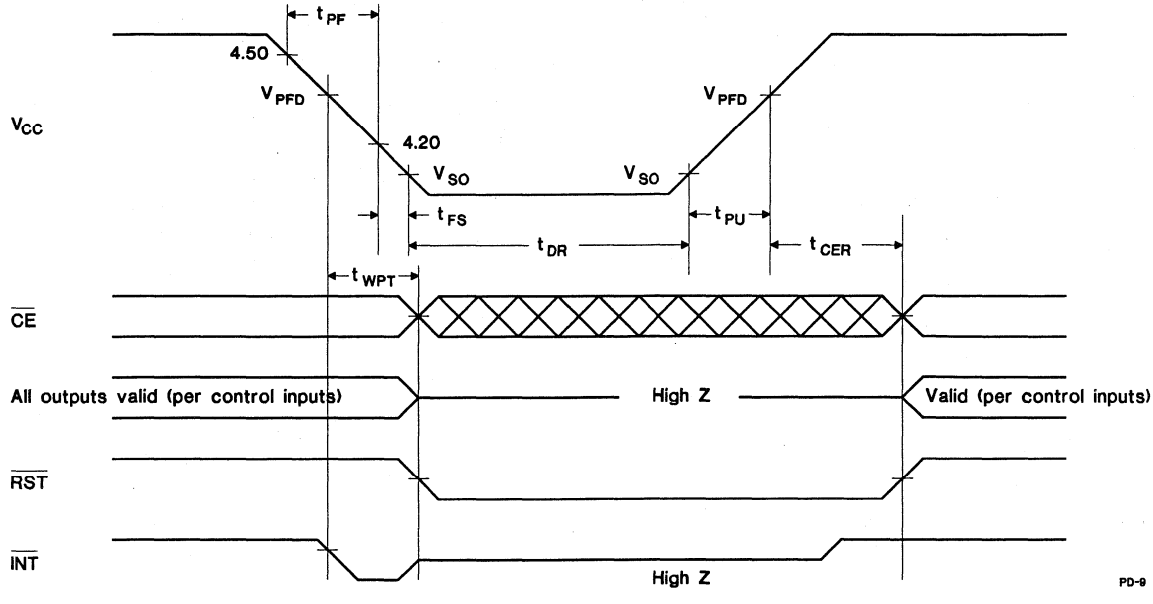
Power-Down/Power-Up Cycle (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.50 to 4.20 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.20 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	160	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

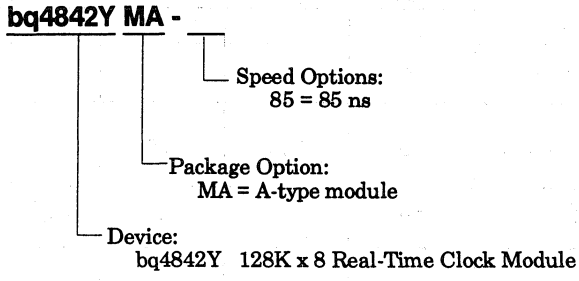
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



Notes:
1. PWRIE is set to "1" to enable power fail interrupt.
2. $\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

Ordering Information



BENCHMARQ

Preliminary **bq4845/bq4845Y**

Parallel RTC With CPU Supervisor

Features

- Real-Time Clock counts seconds through years in BCD format
- On-chip battery-backup switchover circuit with nonvolatile control for external SRAM
- ±1 minute per month clock accuracy
- Less than 500nA of clock operation current in back-up mode
- Microprocessor reset valid to $V_{CC} = V_{SS}$
- Independent watchdog timer with a programmable time-out period
- Power-fail interrupt warning
- Programmable clock alarm interrupt active in battery backup mode
- Programmable periodic interrupt
- Battery-low warning

General Description

The bq4845 Real-Time Clock is a low-power microprocessor peripheral that integrates a time-of-day clock, a 100-year calendar and a CPU supervisor in a 28-pin SOIC or DIP. The bq4845 is ideal for fax machines, copiers, industrial control systems, point-of-sale terminals, data loggers, and computers.

The bq4845 provides direct connections for a 32.768KHz quartz crystal and a 3V backup battery. Through the use of the conditional chip enable output ($\overline{CE}_{OUT}$) and battery voltage output (V_{OUT}) pins, the bq4845 can write-protect and make nonvolatile external SRAMs. The backup cell powers the real-time clock and maintains SRAM information in the absence of system voltage.

The bq4845 contains a temperature-compensated reference and comparator circuit that monitors the status of its voltage supply. When the bq4845 detects an out-of-tolerance condition, it generates an interrupt warning and subsequently a microprocessor reset. The reset stays active for 200ms after V_{CC} rises within tolerance, to allow for power supply and processor stabilization.

The bq4845 also has a built-in watchdog timer to monitor processor operation. If the microprocessor does not toggle the watchdog input (WDI) within the programmed time-out period, the bq4845 asserts $\overline{WDO}$ and $\overline{RST}$. WDI unconnected disables the watchdog timer.

The bq4845 can generate other interrupts based on a clock alarm condition or a periodic setting. The alarm interrupt can be set to occur from once per second to once per month. The alarm can be made active in the battery-backup mode to serve as a system wake-up call. For interrupts at a rate beyond once per second, select a periodic interrupt option for periods of 30.5µs to 500ms.

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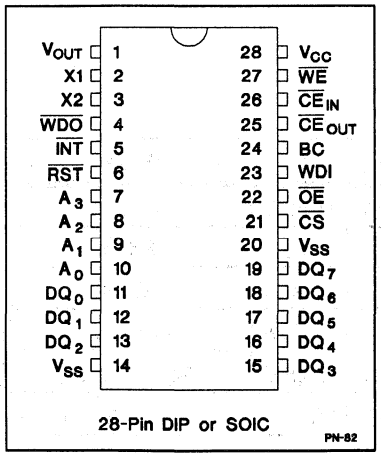
Pin Connections



28-Pin DIP or SOIC

PN-82

Pin Names

A_0-A_3	Clock/control address inputs	BC	Backup battery input
DQ_0-DQ_7	Data inputs/outputs	V_{OUT}	Back-up battery output
$\overline{WE}$	Write enable	$\overline{INT}$	Interrupt output
$\overline{OE}$	Output enable	$\overline{RST}$	Microprocessor reset
$\overline{CS}$	Chip select input	WDI	Watchdog input
$\overline{CE}_{IN}$	External RAM chip enable	$\overline{WDO}$	Watchdog output
$\overline{CE}_{OUT}$	Conditional RAM chip enable	V_{CC}	+5V supply
		V_{SS}	Ground
X1, X2	Crystal inputs		

Functional Description

Figure 1 is a block diagram of the bq4845. The following sections describe the bq4845 functional operation including clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

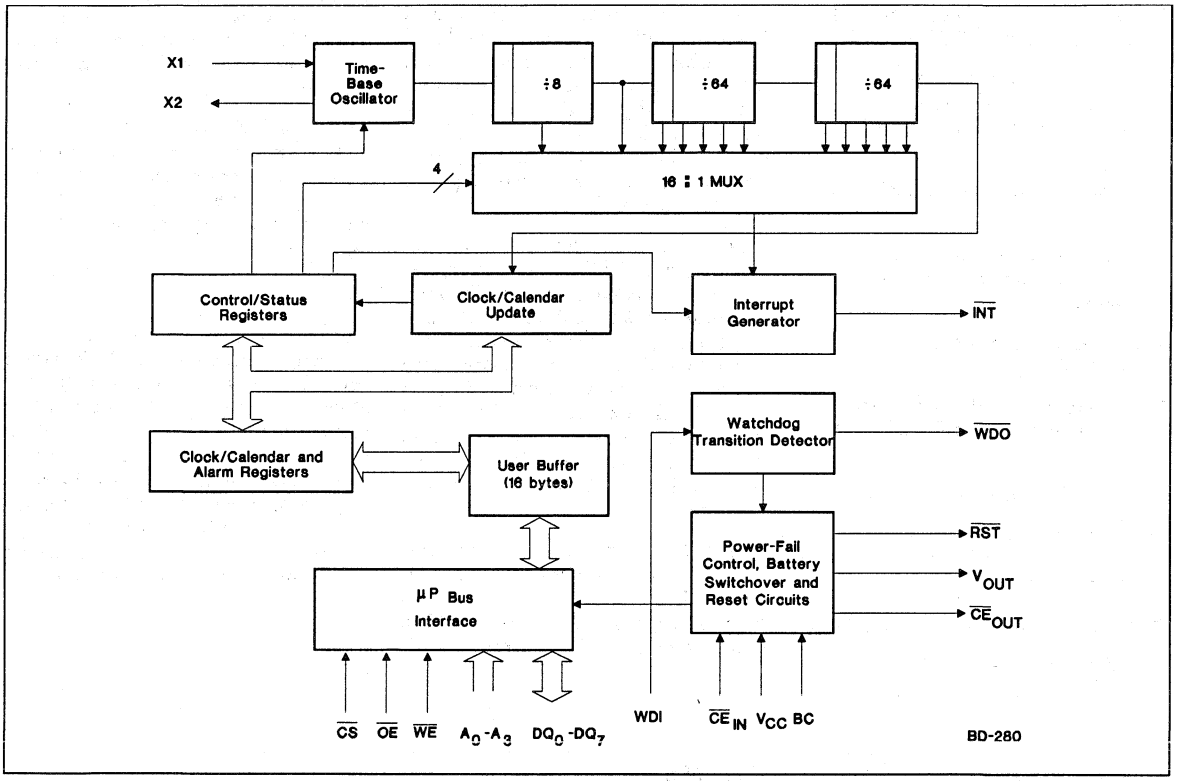


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{CE}_{OUT}$	V_{OUT}	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	$\overline{CE}_{IN}$	V_{OUT1}	Deselect	High Z	Standby
> V_{CC} (min.)	V_{IL}	X	V_{IL}	$\overline{CE}_{IN}$	V_{OUT1}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	$\overline{CE}_{IN}$	V_{OUT1}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	$\overline{CE}_{IN}$	V_{OUT1}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	V_{OH}	V_{OUT2}	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	V_{OHB}	V_{OUT2}	Deselect	High Z	Battery-backup mode

Pin Descriptions

X1, X2 **Crystal inputs**

X1 and X2 are a direct connection for a 32.768kHZ, 6pf crystal.

$\overline{RST}$ **Reset output**

$\overline{RST}$ goes low whenever V_{CC} falls below the power fail threshold. $\overline{RST}$ will remain low for 200ms typical after V_{CC} crosses the threshold on power-up. $\overline{RST}$ is an open-drain output.

$\overline{INT}$ **Interrupt output**

$\overline{INT}$ goes low when a power fail, periodic, or alarm condition occurs. $\overline{INT}$ is an open-drain output.

WDI **Watchdog input**

WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period (1.5 seconds default), $\overline{WDO}$ goes low. $\overline{WDO}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and V_{SS}, which sets it to mid-supply when left unconnected.

$\overline{WDO}$ **Watchdog output**

$\overline{WDO}$ goes low if WDI remains either high or low longer than the watchdog timeout period. $\overline{WDO}$ returns high on the next transition at WDI. $\overline{WDO}$ remains high if WDI is unconnected.

A_0-A_3 **Clock address inputs**

A_0-A_3 allow access to the 16 bytes of real time clock and control registers.

DQ_0-DQ_7 **Data input and output**

DQ_0-DQ_7 provide x8 data for real-time clock information. These pins connect to the memory data bus.

V_{SS} **Ground**

$\overline{CS}$ **Chip select**

$\overline{OE}$ **Output enable**

$\overline{OE}$ provides the read control for the RTC memory locations.

$\overline{CE}_{OUT}$ **Chip enable output**

$\overline{CE}_{OUT}$ goes low only when $\overline{CE}_{IN}$ is low and V_{CC} is above the power fail threshold. If $\overline{CE}_{IN}$ is low, and power fail occurs, $\overline{CE}_{OUT}$ will stay low for 100µs or until $\overline{CE}_{IN}$ goes high, whichever occurs first.

$\overline{CE}_{IN}$ **Chip enable input**

$\overline{CE}_{IN}$ is the input to the chip-enable gating circuit.

BC **Backup battery input**

BC should be connected to a 3V backup cell.

V_{OUT} **Output supply voltage**

V_{OUT} provides the higher of V_{CC} or V_{BC}, switched internally, to supply external RAM.

$\overline{WE}$ **Write enable**

$\overline{WE}$ provides the write control for the RTC memory locations.

V_{CC} **Input supply voltage**

+5V input

Address Map

The bq4845 provides 16 bytes of clock and control status registers. Table 1 is a map of the bq4845 registers, and Table 2 describes the register bits.

Clock Memory Interface

The bq4845 has the same interface for clock/calendar and control information as standard SRAM. To read and write to these locations, the user must put the bq4845 in the proper mode and meet the timing requirements.

Read Mode

The bq4845 is in read mode whenever $\overline{WE}$ (write enable) is high and $\overline{CS}$ (chip select) is low. The unique address, specified by the 4 address inputs, defines which one of the 16 clock/calendar bytes is to be accessed. The bq4845 makes valid data available at the data I/O pins within t_{AA} (address access time). This occurs after the last address input signal is stable, and providing the $\overline{CS}$ and $\overline{OE}$ (output enable) access times are met. If the $\overline{CS}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip select access time (t_{ACS}) or output enable access time (t_{OE}).

$\overline{CS}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the

Table 1. bq4845 Clock and Control Register Map

Address (h)	D7	D6	D5	D4	D3	D2	D1	D0	12-Hour Range (h)	Register
0	*	10-second digit			1-second digit				00–59	Seconds
1	ALM0	10-second digit			1-second digit				0–59 or 80–D9	Seconds alarm
2	*	10-minute digit			1-minute digit				0–59	Minutes
3	ALM1	10-minute digit			1-minute digit				0–59 or 80–D9	Minutes alarm
4	*	PM/AM	10-hour digit		1-hour digit				01–12/41–52	Hours
5	ALM2	PM/AM	10-hour digit		1-hour digit				01–12/41–52 or 81–92/C1–D2	Hours alarm
6	*	*	10-day digit		1-day digit				01–31	Day
7	ALM3	*	10-day digit		1-day digit				01–31 or 81–B1	Day alarm
8	*	*			*	Day-of-week digit			01–07	Day-of-week
9	*	*	*	10 mo.	1-month digit				01–12	Month
A	10-year digit				1-year digit				00–99	Year
B	*	WD2	WD1	WD0	RS3	RS2	RS1	RS0		Programmable rates
C	*	*			AIE	PIE	PWRIE	ABE		Interrupt enables
D	*	*			AF	PF	PWRF	BLF		Flags
E	*	*			UTI	$\overline{STOP}$	24/12	DSE		Control
F	*	*	*	*	*	*	*	*		Unused

Notes: * = Unused bits; unwritable and read as 0.
Clock calendar data in BCD.
PM/AM = 1 for PM; PM/AM = 0 for AM.
DSE = 1 enables daylight savings adjustment.
24/12 = 1 enables 24-hour data representation; 24/12 = 0 enables 12-hour data representation.
Day-of-Week coded as Sunday = 1 through Saturday = 7.
BLF = 1 for valid battery.
$\overline{STOP}$ = 1 turns the RTC on; $\overline{STOP}$ = 0 stops the RTC in back-up mode.
Register C is cleared on power-up.

Table 2. Clock and Control Register Bits

Bits	Description
24/12	24- or 12-hour representation
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM3	Alarm repeat rate
BLF	Battery-low flag
DSE	Daylight savings time enable
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PM/AM	PM or AM indication
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
RS0–RS3	Periodic interrupt rate
$\overline{STOP}$	Oscillator stop and start
UTI	Update transfer inhibit
WD0 - WD2	Watchdog timeout rate

data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CS}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4845 is in write mode whenever $\overline{WE}$ and $\overline{CS}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CS}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CS}$. The addresses must be held valid throughout the cycle. $\overline{CS}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CS}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CS}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Reading the Clock

Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4845 clock registers should be halted. Updating is halted by setting the update transfer inhibit (UTI) bit D3 of the control register E. As long as the UTI bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the UTI bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the UTI bit, reading the clock locations has no effect on clock accuracy. Once the UTI bit is reset to 0, the internal registers update within one second the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

The UTI bit must also be used to set the bq4845 clock. Once set, the locations can be written with the desired information in BCD format. Resetting the UTI bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second.

Stopping and Starting the Clock Oscillator

The bq4845 clock can be programmed to turn off when the part goes into battery back-up mode by setting $\overline{STOP}$ to 0 prior to power down. If the board using the bq4845 is to spend a significant period of time in storage, the $\overline{STOP}$ bit can be used to preserve some battery capacity. $\overline{STOP}$ set to 1 keeps the clock running when V_{CC} drops below V_{SO}. With V_{CC} greater than V_{SO}, the bq4845 clock runs regardless of the state of $\overline{STOP}$.

Power-Down/Power-Up Cycle

The bq4845 continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD}, the bq4845 write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4845. As the voltage input V_{CC} slows down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in progress to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. $\overline{CE}_{OUT}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 10ns.

Figure 2 shows the hardware hookup for the external RAM.

A primary backup energy source input is provided on the bq4845. The BC input accepts a 3V primary battery, typically some type of lithium chemistry. To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{OUT}$ are internally isolated from BC by the initial connection of a battery. Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM.

Power-On Reset

The bq4845 provides a power-on reset, which pulls the $\overline{RST}$ pin low on power-down and remains low on power-up for t_{RST} after V_{CC} passes V_{PFD}. With valid battery voltage on BC, $\overline{RST}$ remains valid for V_{CC}= V_{SS}

Watchdog Timer

The watchdog monitors microprocessor activity through the Watchdog input (WDI). To use the watchdog function, connect WDI to a bus line or a microprocessor I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.5 seconds default), the bq4845 asserts $\overline{WDO}$ and $\overline{RST}$.

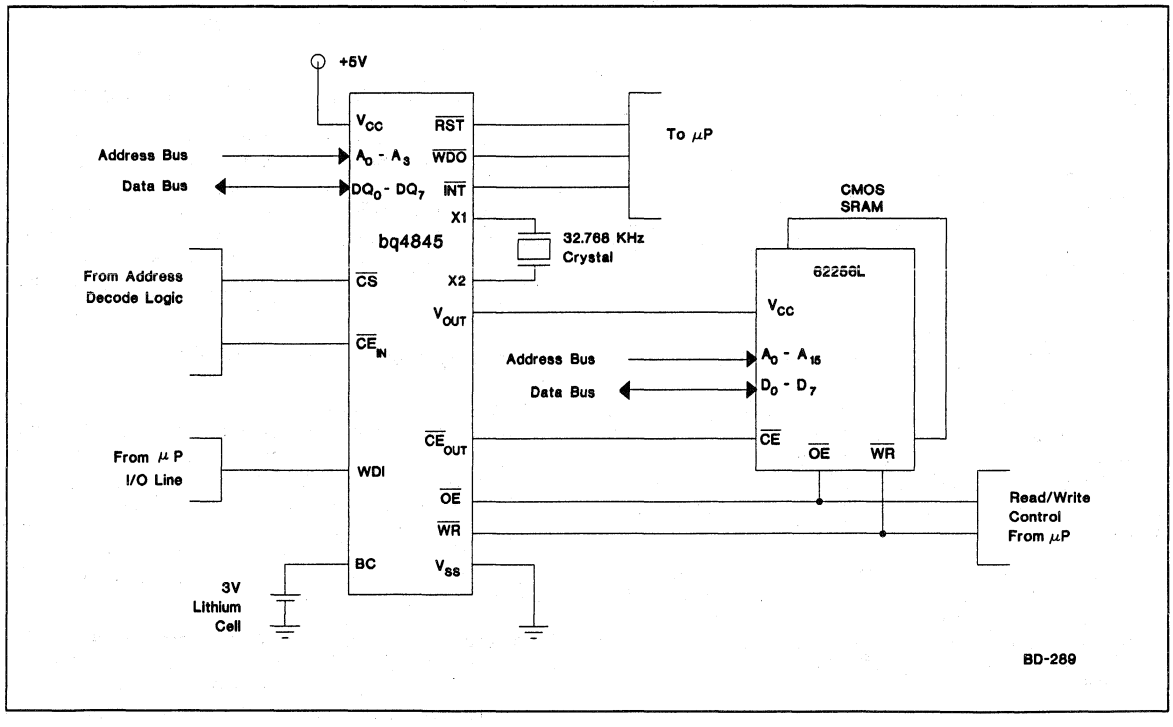


Figure 2. bq4845 Application Circuit

Watchdog Input

The bq4845 resets the watchdog timer if a change of state (high to low, low to high, or a minimum 100ns pulse) occurs at the Watchdog input (WDI) during the watchdog period. The watchdog timeout is set by WD0-WD2 in register B. The bq4845 maintains the watchdog timeout programming through power cycles. The default state (no valid battery power) of WD0-WD2 is 000 or 1.5s on power-up. Table 3 shows the programmable watchdog timeout rates. The watchdog timeout period immediately after a reset is equal to the programmed watchdog timeout.

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the power-fail threshold, the bq4845 disables the watchdog function and disconnects WDI from its internal resistor network, thus making it high impedance.

Watchdog Output

The Watchdog output ($\overline{WDO}$) remains high if there is a transition or pulse at WDI during the watchdog timeout period. The bq4845 disables the watchdog function and $\overline{WDO}$ is a logic high when V_{CC} is below the power fail threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog timeout period, the bq4845 asserts $\overline{RST}$ for the reset timeout period t_1. $\overline{WDO}$ goes low and remains low until the next transition at WDI. If WDI is held high or low indefinitely, $\overline{RST}$ will generate pulses (t_1 seconds wide) every t_3 seconds. Figure 3 shows the watchdog timing.

Interrupts

The bq4845 allows three individually selected interrupt events to generate an interrupt request on the $\overline{INT}$ pin. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 30.5µs to 500ms
- The alarm interrupt, programmable to occur once per second to once per month

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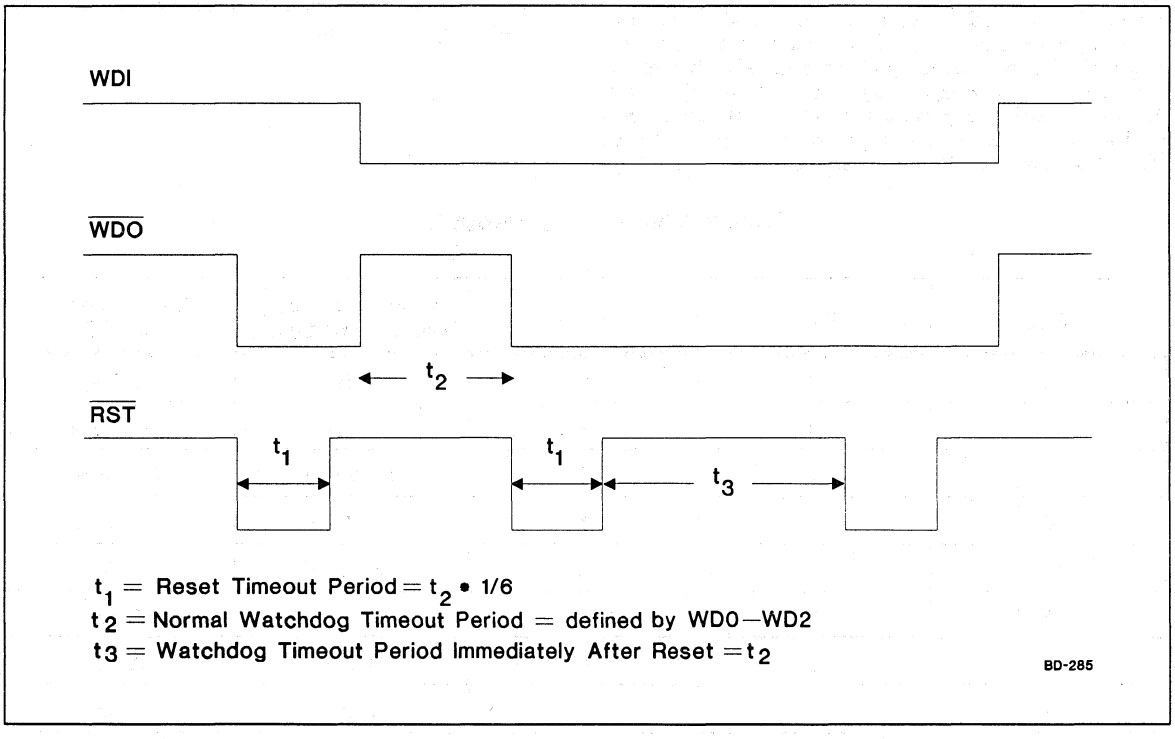

Figure 3. Watchdog Timeout Period and Reset Active Time

- The power-fail interrupt, which can be enabled to be asserted when the bq4845 detects a power failure

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register C, the interrupts register. When an event occurs, its event flag bit in the flags register, register D, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{INT}$ high impedance. To reset the flag register, the bq4845 addresses must be held stable at register D for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{INT}$ goes active when the bq4845 sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{INT}$ to the high-impedance state. Table 4 shows the periodic rates.

Alarm Interrupt

Registers 1, 3, 5, and 7 program the real-time clock alarm. During each update cycle, the bq4845 compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{INT}$. The alarm condition is cleared by a read to the flags register. ALM3–ALM0 puts the alarm into a periodic mode of operation. Table 5 describes the selectable rates.

The alarm interrupt can be made active while the bq4845 is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{INT}$ pin goes high-impedance during battery backup. With ABE set, however, $\overline{INT}$ is driven low if an alarm condition occurs and the AIE bit is set. Because the AIE bit is reset during power-on reset, an alarm generated during power-on reset updates only the flags register. The user can read the flags register during boot-up to determine if an alarm was generated during power-on reset.

Power-Fail Interrupt

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{INT}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4845 generates a reset and deselects. The PWRIE bit is cleared on power-up.

Battery-Low Warning

The bq4845 checks the battery on power-up. If the battery voltage is below 2.4V, the battery-low flag BLF in the flags register is set to a 0 indicating that clock and RAM data may be invalid.

Table 3. Watchdog Timeout Rates

WD2	WD1	WD0	Normal Watchdog Timeout Period (t_2, t_3)	Reset Timeout Period (t_1)
0	0	0	1.5s	0.25s
0	0	1	23.4375ms	3.9063ms
0	1	0	46.875ms	7.8125ms
0	1	1	93.75ms	15.625ms
1	0	0	187.5ms	31.25ms
1	0	1	375ms	62.5ms
1	1	0	750ms	125ms
1	1	1	3s	0.5s

Table 4. Periodic Interrupt Rates

Register B Bits				Periodic Interrupt	
RS3	RS2	RS1	RS0	Period	Units
0	0	0	0	None	
0	0	0	1	30.5175	µs
0	0	1	0	61.035	µs
0	0	1	1	122.070	µs
0	1	0	0	244.141	µs
0	1	0	1	488.281	µs
0	1	1	0	976.5625	µs
0	1	1	1	1.953125	ms
1	0	0	0	3.90625	ms
1	0	0	1	7.8125	ms
1	0	1	0	15.625	ms
1	0	1	1	31.25	ms
1	1	0	0	62.5	ms
1	1	0	1	125	ms
1	1	1	0	250	ms

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Table 5. Alarm Frequency (Alarm Bits D7 of Alarm Registers)

ALM3	ALM2	ALM1	ALM0	Alarm Frequency
1	1	1	1	Once per second
1	1	1	0	Once per minute when seconds match
1	1	0	0	Once per hour when minutes, and seconds match
1	0	0	0	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4845Y
		4.75	5.0	5.5	V	bq4845
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
V_{BC}	Backup cell voltage	2.5	-	4.0	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OHB}	V_{OH}, BC Supply	V_{BC}- 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	12	25	mA	Min. cycle, duty = 100%, $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA
I_{SB1}	Standby supply current	-	3	-	mA	$\overline{CS} = V_{IH}$
I_{SB2}	Standby supply current	-	500	-	µA	$\overline{CS} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4845
	Power-fail-detect voltage	4.30	4.37	4.5	V	bq4845Y
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 100mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V	-	-	V	I_{OUT} = 100µA, $V_{CC} < V_{BC}$
I_{CE}	Chip enable input current			100	µA	Internal 50K pull-up
V_{RST}	$\overline{RST}$ output voltage			0.4V		I_{RST} = 4mA
V_{INT}	$\overline{INT}$ output voltage			0.4V		I_{INT} = 4mA
I_{WDIL}	Watchdog input low current	-50	-10		µA	0 < V_{WDI} < 0.8V
I_{WDIH}	Watchdog input high current		20	50	µA	2.2 < V_{WDI} < V_{CC}

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
$\overline{RST}$ and $\overline{INT}$ are open-drain outputs.

Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	5	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

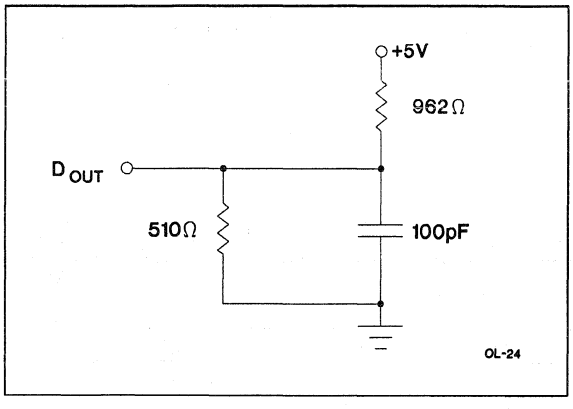


Figure 4. Output Load A

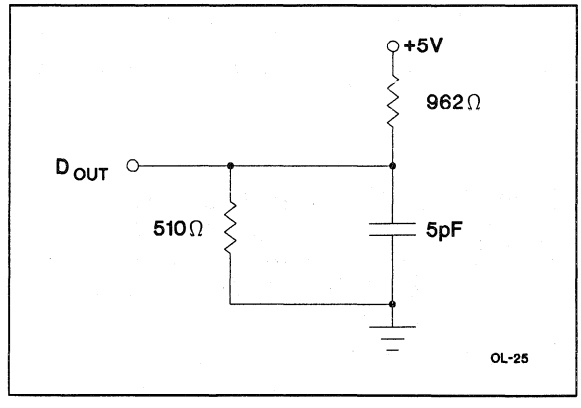


Figure 5. Output Load B

Read Cycle (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RC}	Read cycle time	70	-	ns	
t_{AA}	Address access time	-	70	ns	Output load A
t_{ACS}	Chip select access time	-	70	ns	Output load A
t_{OE}	Output enable to output valid	-	35	ns	Output load A
t_{CLZ}	Chip select to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	ns	Output load B
t_{CHZ}	Chip deselect to output in high Z	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

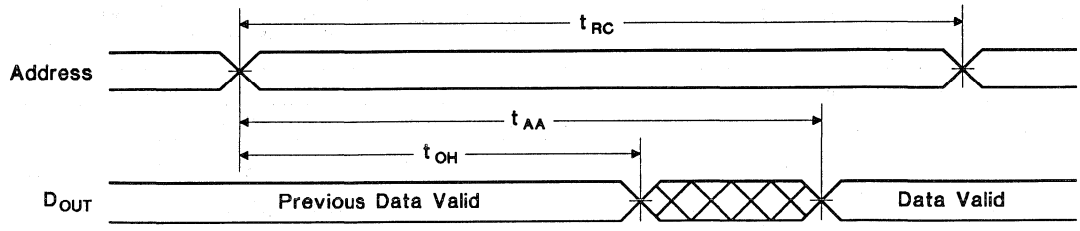
Write Cycle (T_A =TOPR , VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WC}	Write cycle time	70	-	ns	
t_{CW}	Chip select to end of write	65	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	ns	Measured to first low-to-high transition of either $\overline{CS}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

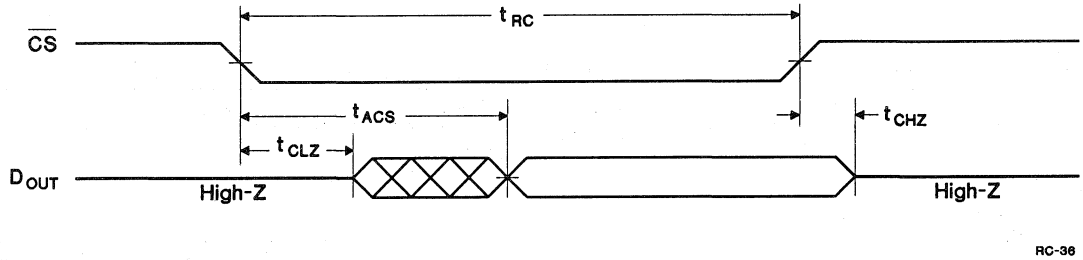
Notes:

1. A write ends at the earlier transition of $\overline{CS}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

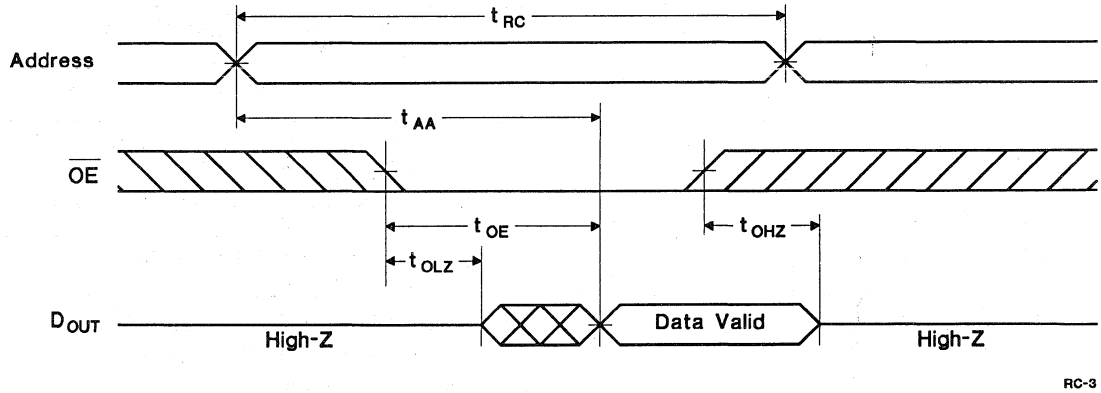
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CS}$ Access) [1,3,4]

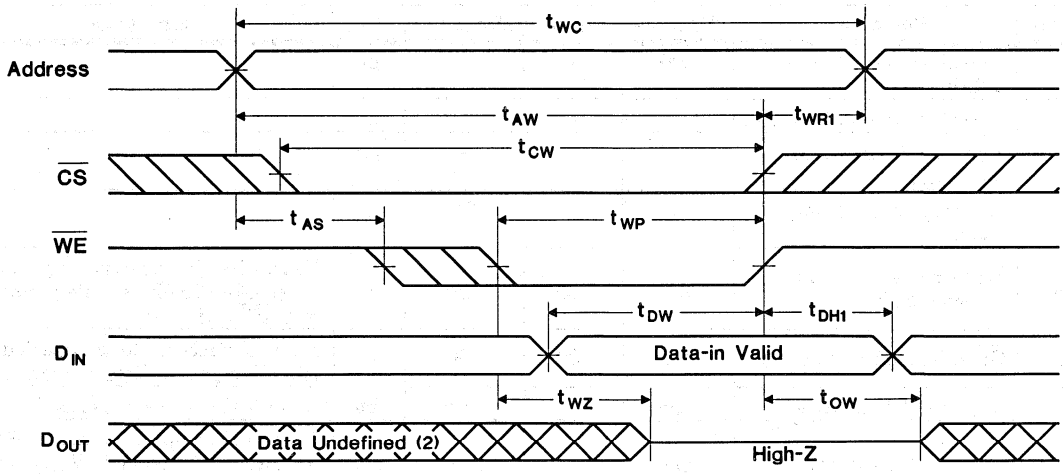


Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]

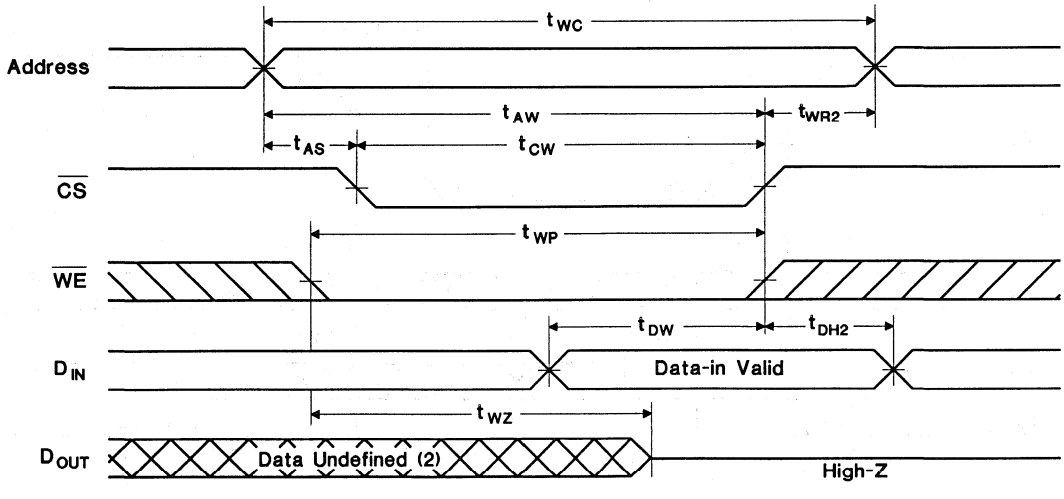


Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CS} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CS} = V_{IL}$.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CS}$-Controlled) [1,2,3,4,5]



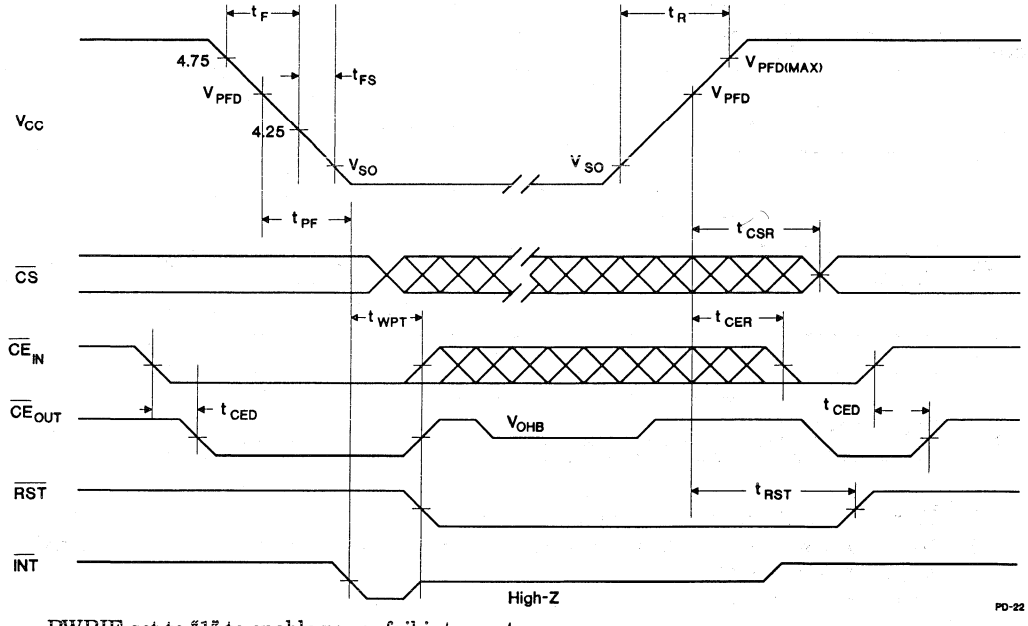
Notes:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.75 to 4.25V	300	-	-	µs	-
t_{FS}	V_{CC} slew from 4.25 to V_{SO}	10	-	-	µs	-
t_R	V_{CC} slew from V_{SO} to $V_{PFD(MAX)}$	100	-	-	µs	-
t_{PF}	Interrupt delay from V_{PFD}	6	-	24	µs	-
t_{WPT}	Write-protect time for external RAM	90	100	120	µs	Delay after V_{CC} slows down past V_{PFD} before SRAM is write-protected and $\overline{RST}$ activated.
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	100	200	300	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{RST}	V_{PFD} to $\overline{RST}$ inactive	t_{CSR}	-	t_{CSR}	ms	Reset active timeout period
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	7	10	ns	Output load A

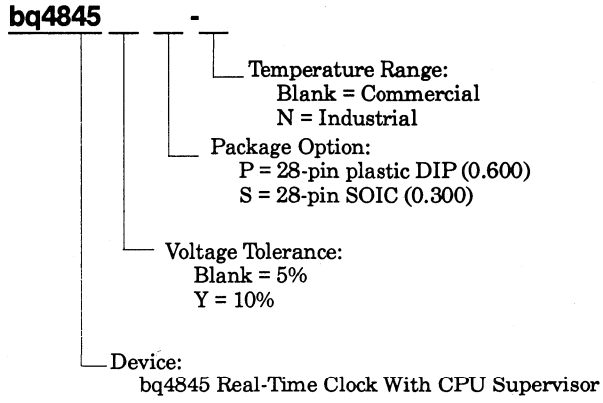
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



Notes: PWRIE set to "1" to enable power fail interrupt.
$\overline{RST}$ and $\overline{INT}$ are open drain and require an external pull-up resistor.

Ordering Information



4

BENCHMARQ

Preliminary **bq4847/bq4847Y**

RTC Module With CPU Supervisor

Features

- Real-Time Clock counts seconds through years in BCD format
- Integrated battery and crystal
- On-chip battery-backup switchover circuit with nonvolatile control for an external SRAM
- 130mAh battery capacity
- ±1 minute per month clock accuracy
- Less than 500nA of clock operation current in backup mode
- Microprocessor reset valid to $V_{CC} = V_{SS}$
- Independent watchdog timer with a programmable time-out period
- Power-fail interrupt warning
- Programmable clock alarm interrupt active in battery-backup mode
- Programmable periodic interrupt
- Battery-low warning

General Description

The bq4847 Real-Time Clock Module is a low-power microprocessor peripheral that integrates a time-of-day clock, a 100-year calendar, a CPU supervisor, a battery, and a crystal in a 28-pin DIP module. The part is ideal for fax machines, copiers, industrial control systems, point-of-sale terminals, data loggers, and computers.

The bq4847 contains an internal battery and crystal. Through the use of the conditional chip enable output ($\overline{CE}_{OUT}$) and battery voltage output (V_{OUT}) pins, the bq4847 can write-protect and make nonvolatile an external SRAM. The backup cell powers the real-time clock and maintains SRAM information in the absence of system voltage.

The bq4847 contains a temperature-compensated reference and comparator circuit that monitors the status of its voltage supply. When an out-of-tolerance condition is detected, the bq4847 generates an interrupt warning and subsequently a microprocessor reset.

The reset stays active for 200ms after V_{CC} rises within tolerance to allow for power supply and processor stabilization.

The bq4847 also has a built-in watchdog timer to monitor processor operation. If the microprocessor does not toggle the watchdog input (WDI) within the programmed time-out, the bq4847 asserts $\overline{WDO}$ and $\overline{RST}$. WDI unconnected disables the watchdog timer.

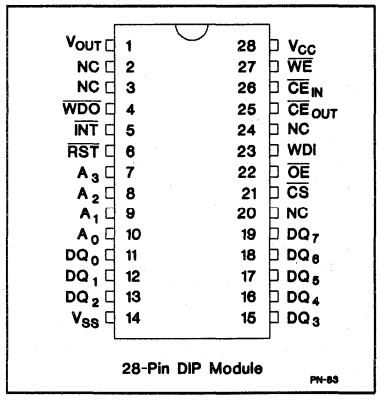
The bq4847 can generate other interrupts based on a clock alarm condition or a periodic setting. The alarm interrupt can be set to occur from once per second to once per month. The alarm can be made active in the battery-backup mode to serve as a system wake-up call. For interrupts at a rate beyond once per second, select a periodic interrupt option for periods of 30.5µs to 500ms.

4

Caution:

Care should be taken to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

Pin Connections



28-Pin DIP Module PN-8S

Pin Names

A_0-A_3	Clock/Control address inputs	NC	No connect
DQ_0-DQ_7	Data inputs/outputs	V_{OUT}	Back-up battery output
$\overline{WE}$	Write enable	$\overline{INT}$	Interrupt output
$\overline{OE}$	Output enable	$\overline{RST}$	Microprocessor reset
$\overline{CS}$	Chip select input	WDI	Watchdog input
$\overline{CE}_{IN}$	External RAM chip enable	$\overline{WDO}$	Watchdog output
$\overline{CE}_{OUT}$	Conditional RAM chip enable	V_{CC}	+5V supply
		V_{SS}	Ground

Functional Description

Figure 1 is a block diagram of the bq4847. For a complete description of operating conditions, electrical characteristics, and bus timing, see the bq4845 data sheet.

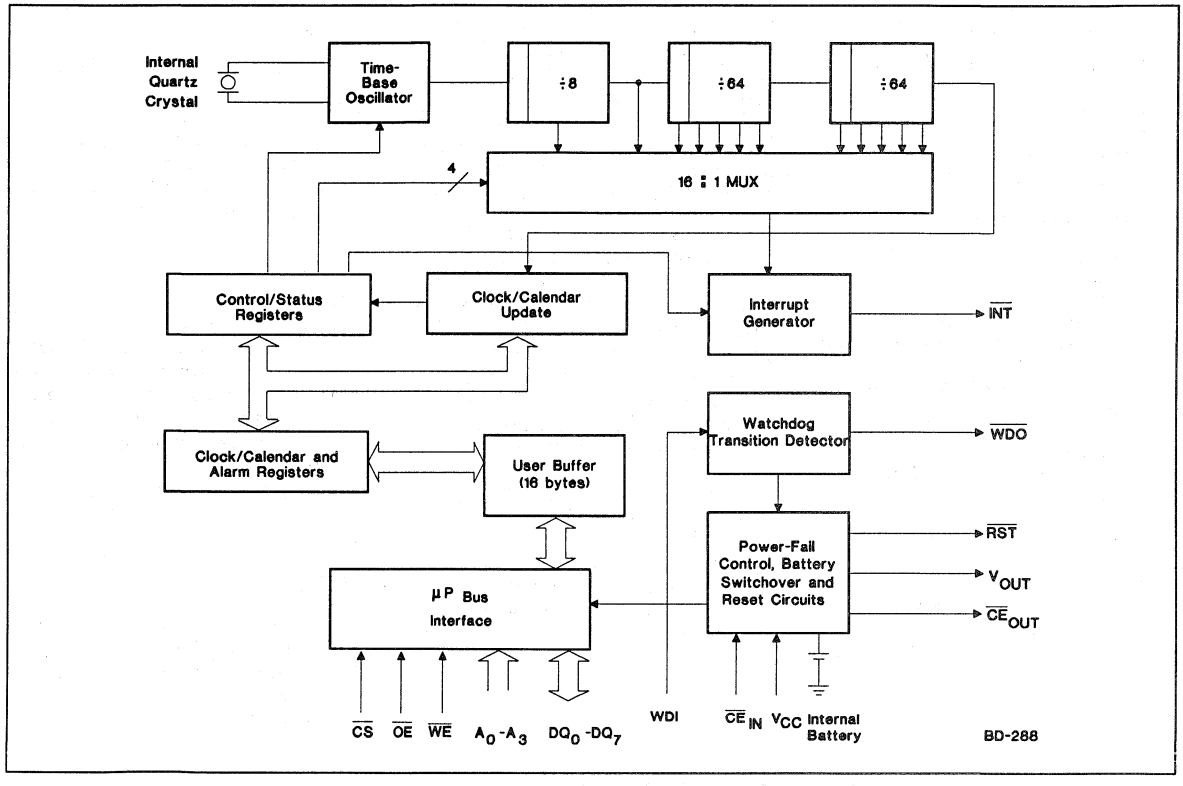


Figure 1. Block Diagram

Truth Table

Vcc	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{CE}_{OUT}$	V_{OUT}	Mode	DQ	Power
< Vcc (max.)	V_{IH}	X	X	$\overline{CE}_{IN}$	V_{OUT1}	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	$\overline{CE}_{IN}$	V_{OUT1}	Write	D_{IN}	Active
> Vcc (min.)	V_{IL}	V_{IL}	V_{IH}	$\overline{CE}_{IN}$	V_{OUT1}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	$\overline{CE}_{IN}$	V_{OUT1}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	V_{OH}	V_{OUT2}	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	V_{OHB}	V_{OUT2}	Deselect	High Z	Battery-backup mode

Typical PC Hookups For Real-Time Clocks

Introduction

The following pages contain diagrams showing how Benchmarq's Real-Time Clocks are used in existing circuits with minor or no redesign. Parts lists are included for each diagram.

The circuits shown are actual PC implementations of Motorola RTCs. The proposed Benchmarq replacements save numerous components and reduce the cost of the motherboard. Pin conversions from the MC146818A to the bq3285 and bq3287/A are shown in Tables 1 and 2.

All of Benchmarq module products are U.L. recognized under U.L. file number E1340146.

Remember that the bq3285/87/87A are socket replacements for the DS1285/87/87A/885/887/887A and MK48T85/87/87A. See Chapter 1 for the RTC cross-reference table.

Examples are included for ISA and EISA PC systems.

- ISA (PC/AT) systems:
  - Example MC146818A PC/AT design (Figure 1, Table 3)
  - Equivalent bq3285 design (Figure 2, Table 4)
  - MC146818A/bq3285 design (Figure 3, Table 4)
  - Equivalent bq3287 design (Figure 4 , Table 5)
- EISA or MCA systems:
  - Example MC146818A plus external 8Kx8 SRAM design (Figure 5, Table 6)
  - Example DS1287 plus external 8Kx8 NVSRAM design (Figure 6, Table 7)
  - Equivalent bq4285 design (Figure 7, Table 8)
  - Equivalent bq4287 design (Figure 8, Table 9)

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Table 1. Converting MC146818A to bq3285/87/87A

MC146818 Pin No.		DIP and SOIC Packages		
		bq3285P/S Pin No.	bq3287MT Pin No.	bq3287AMT Pin No.
1–15	→	No change	No change	No change
16	→	No connect	No change	No change
17–19	→	No change	No change	No change
20	→	< 4.0V	No change	No change
21	→	Tie to V_{CC}	No change	Tie to V_{CC}
22–24	→	No change	No change	No change

Table 2. Converting MC146818A to bq4285/87

MC146818 Pin No.		DIP and SOIC Packages	
		bq4285P/S Pin No.	bq4287MT Pin No.
1	→	V_{OUT}	V_{OUT}
2–20	→	No change	No change
21	→	$\overline{CE}_{IN}$: Tied to V_{SS}	$\overline{CE}_{IN}$: Tied to V_{SS}
22	→	$\overline{CE}_{OUT}$	$\overline{CE}_{OUT}$
23–24	→	No change	No change

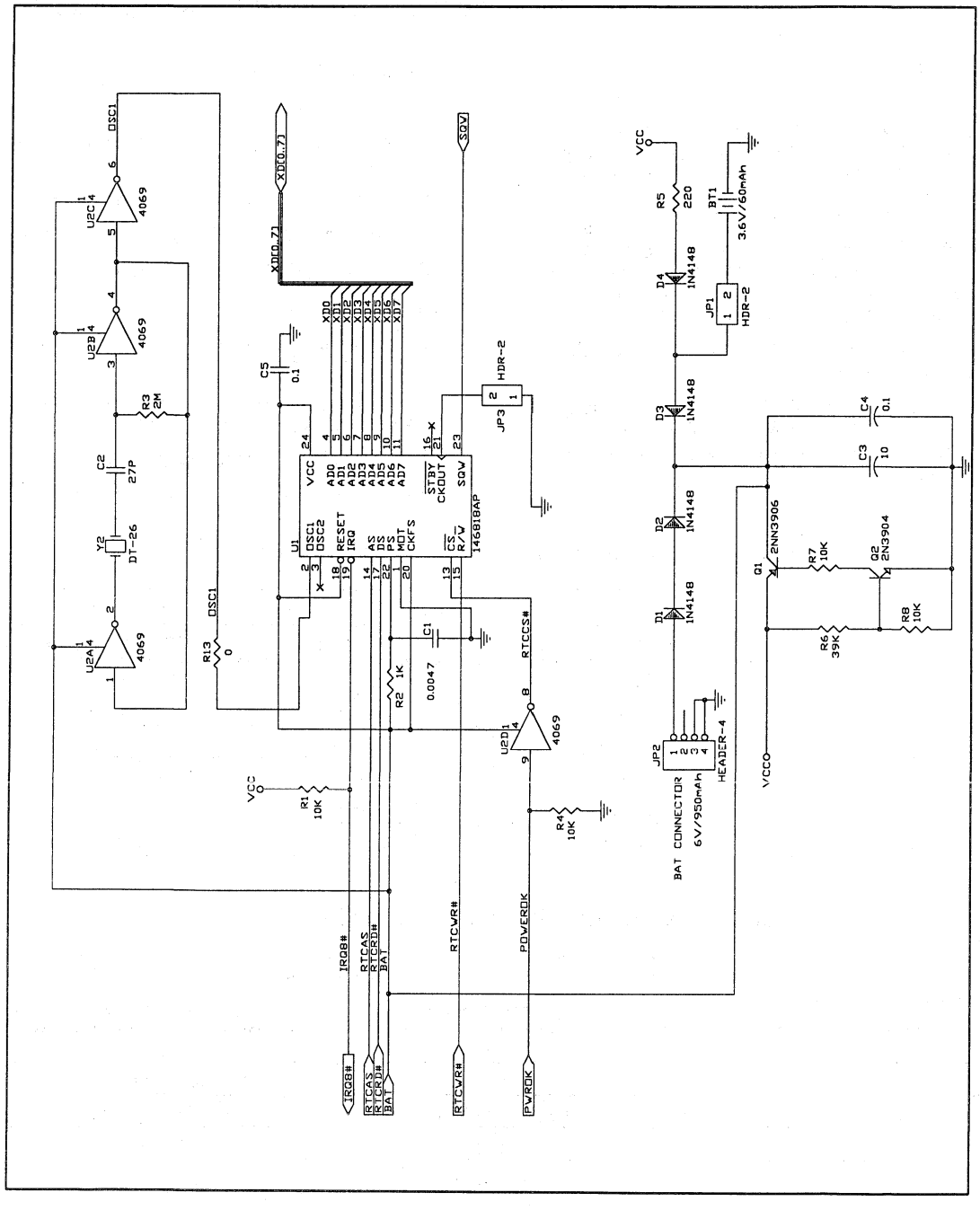

Figure 1. MC146818A ISA (PC/AT) Example

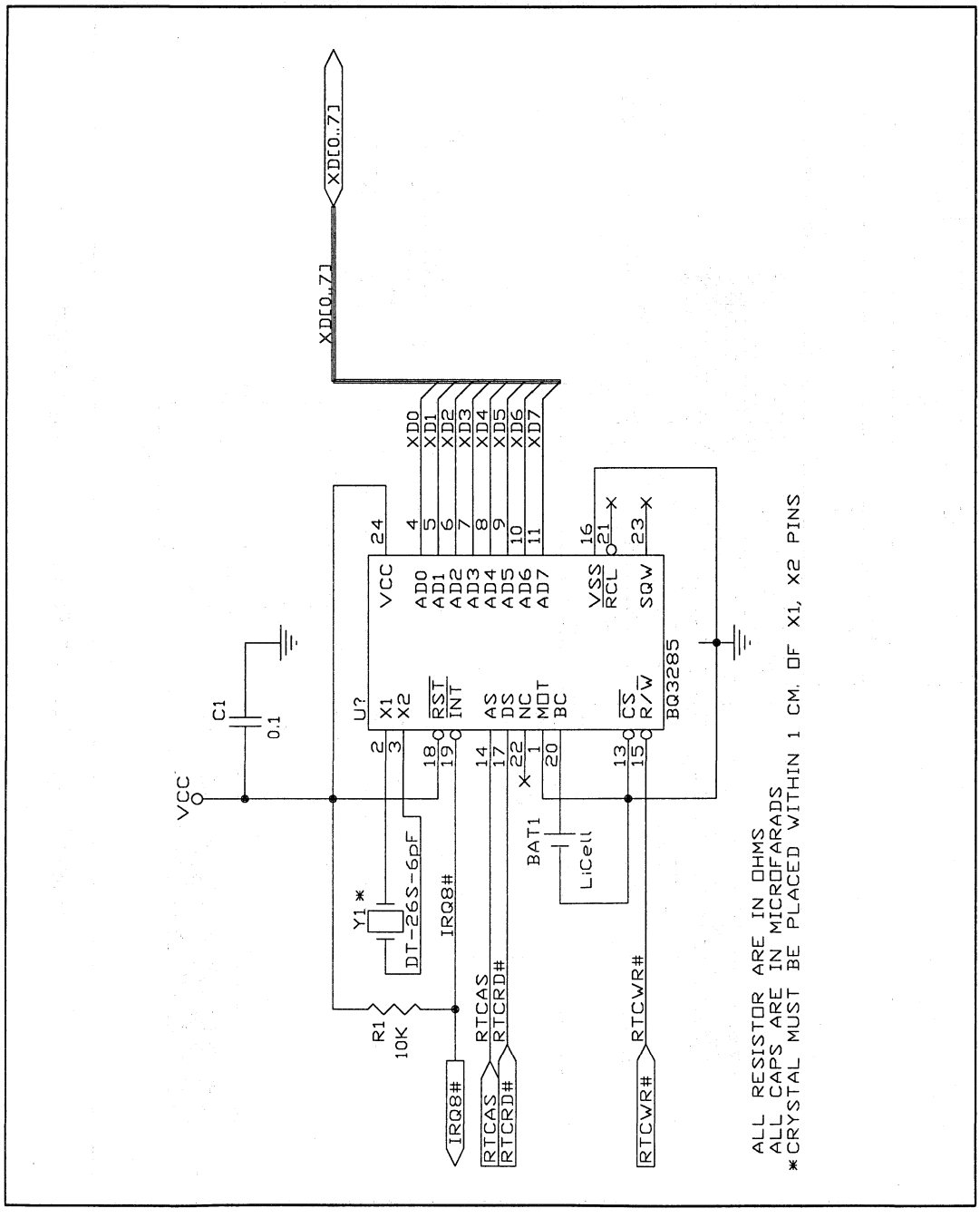

Figure 2. bq3285 ISA (PC/AT) Example

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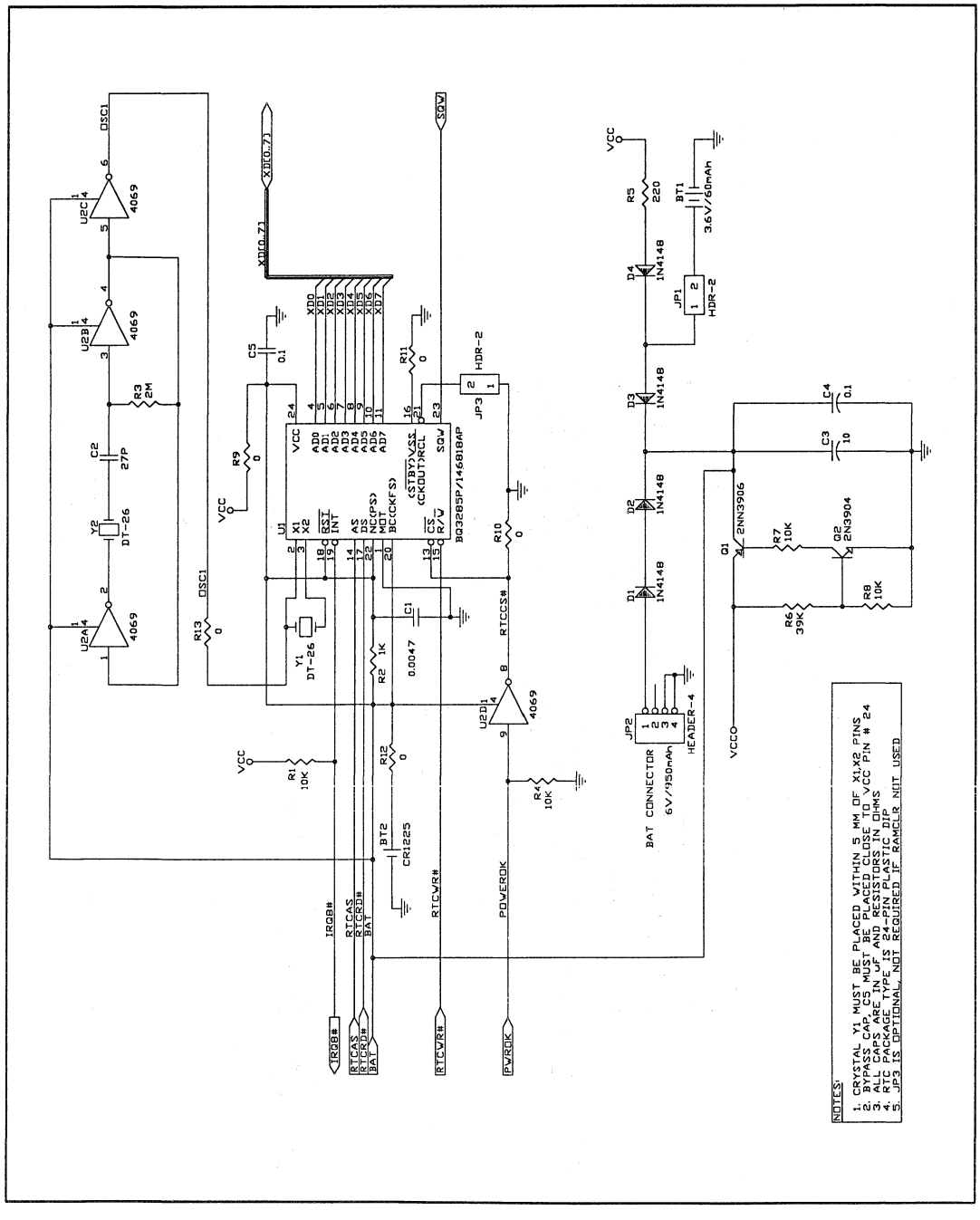

Figure 3. bq3285 or MC146818A ISA (PC/AT) Example

Table 3. MC146818A ISA (PC/AT) Parts List (Figures 1 and 3)

Item	Quantity	Reference	Part
1	1	BT1	3.6V/60mAh
2	1	C1	0.0047
3	1	C2	27P
4	1	C3	10
5	1	C4	0.1
6	4	D1, D2, D3, D4	1N4148
7	1	JP1	HEADER-2
8	1	JP2	HEADER-4
9	1	Q1	2NN3906
10	1	Q2	2N3904
11	4	R1, R4, R7, R8	10K
12	1	R2	1K
13	1	R3	2M
14	1	R5	220
15	1	R6	39K
16	1	U1	MC146818A
17	1	U2	4069
18	1	Y1	DT-26

Table 4. bq3285 ISA (PC/AT) Parts List (Figures 2 and 3)

Item	Quantity	Reference	Part
1	1	R1	10K
2	1	U1	bq3285
3	1	BT1	Li cell
4	1	Y1	DT-26
5	1	C1	0.0047

Notes: Possible crystal/battery suppliers include:

- Daiwa DT-26 or equivalent crystal
- Rayovac/Panasonic lithium coin cells:

  BR1225 38–39mAh
  BR2032 180–200mAh
  BR2325 165–180mAh

  These cells and cells of other sizes are available "tabbed" for soldering directly into boards. These types of lithium coin cells are safe for all modes of transportation per U.S. Department of Transportation records.

- Rayovac U.L. #MH12542
- Panasonic U.L. #MH12210

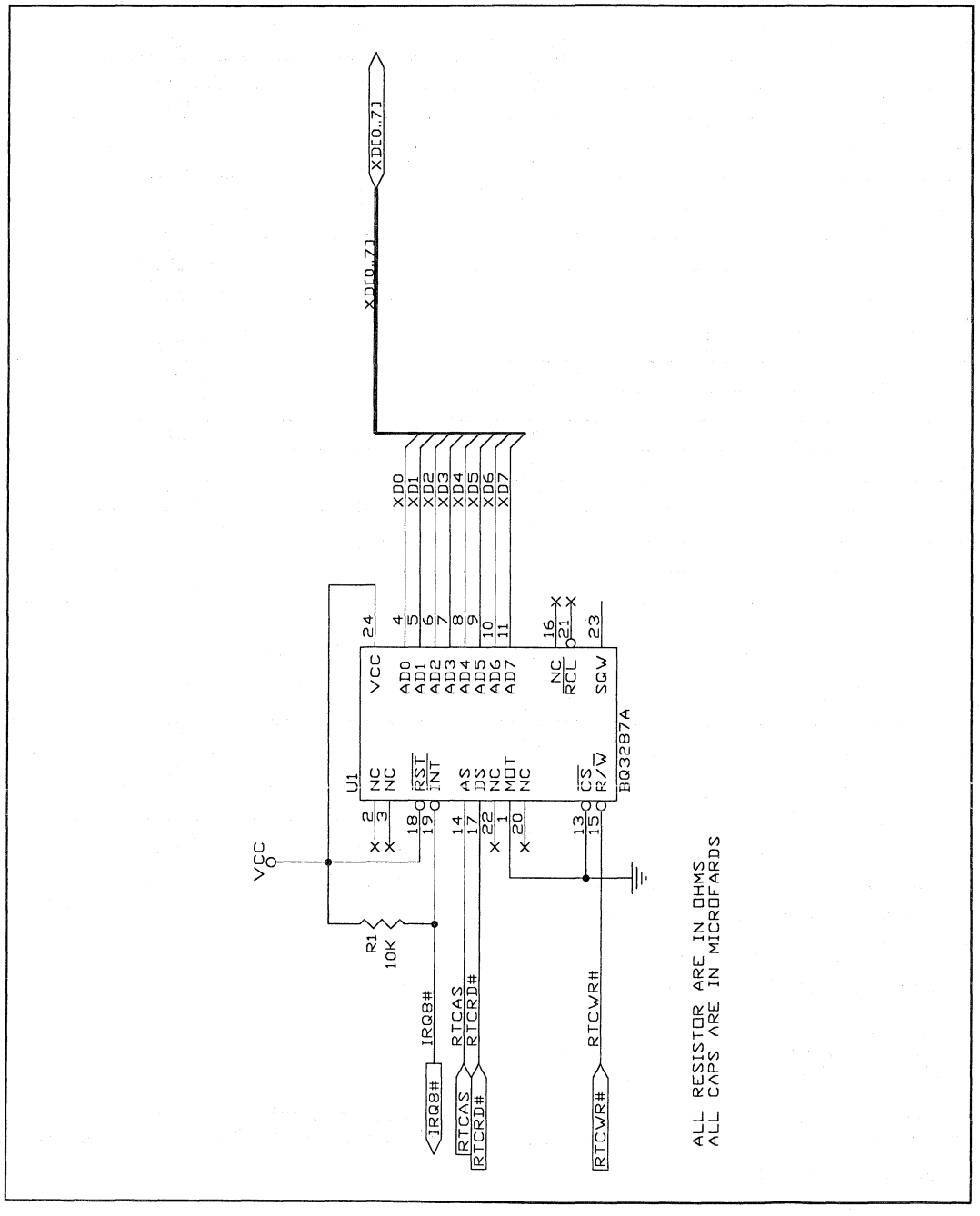

Figure 4. bq3287 ISA (PC/AT) Example

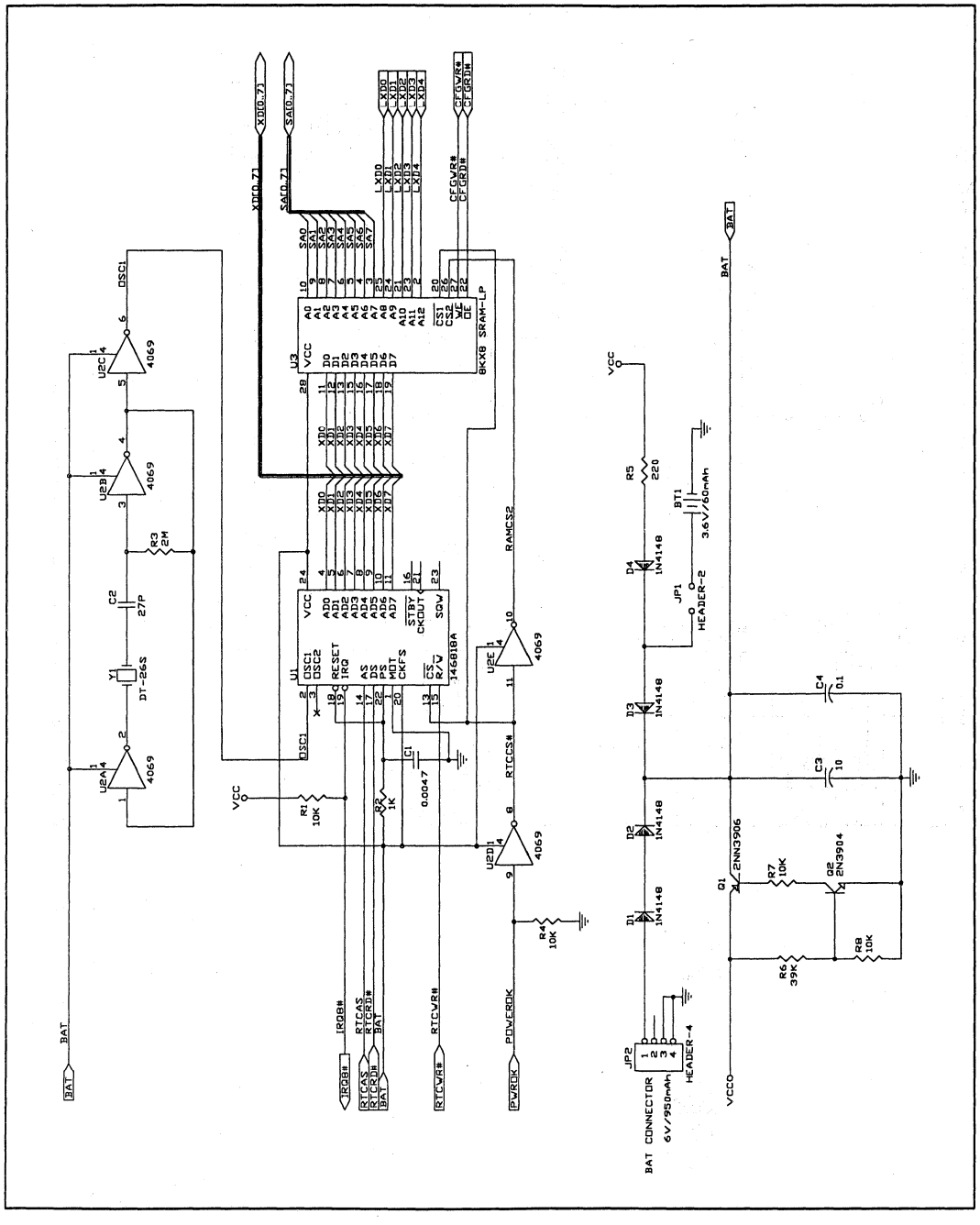

Figure 5. MC146818A w/ External SRAM EISA or MCA Example

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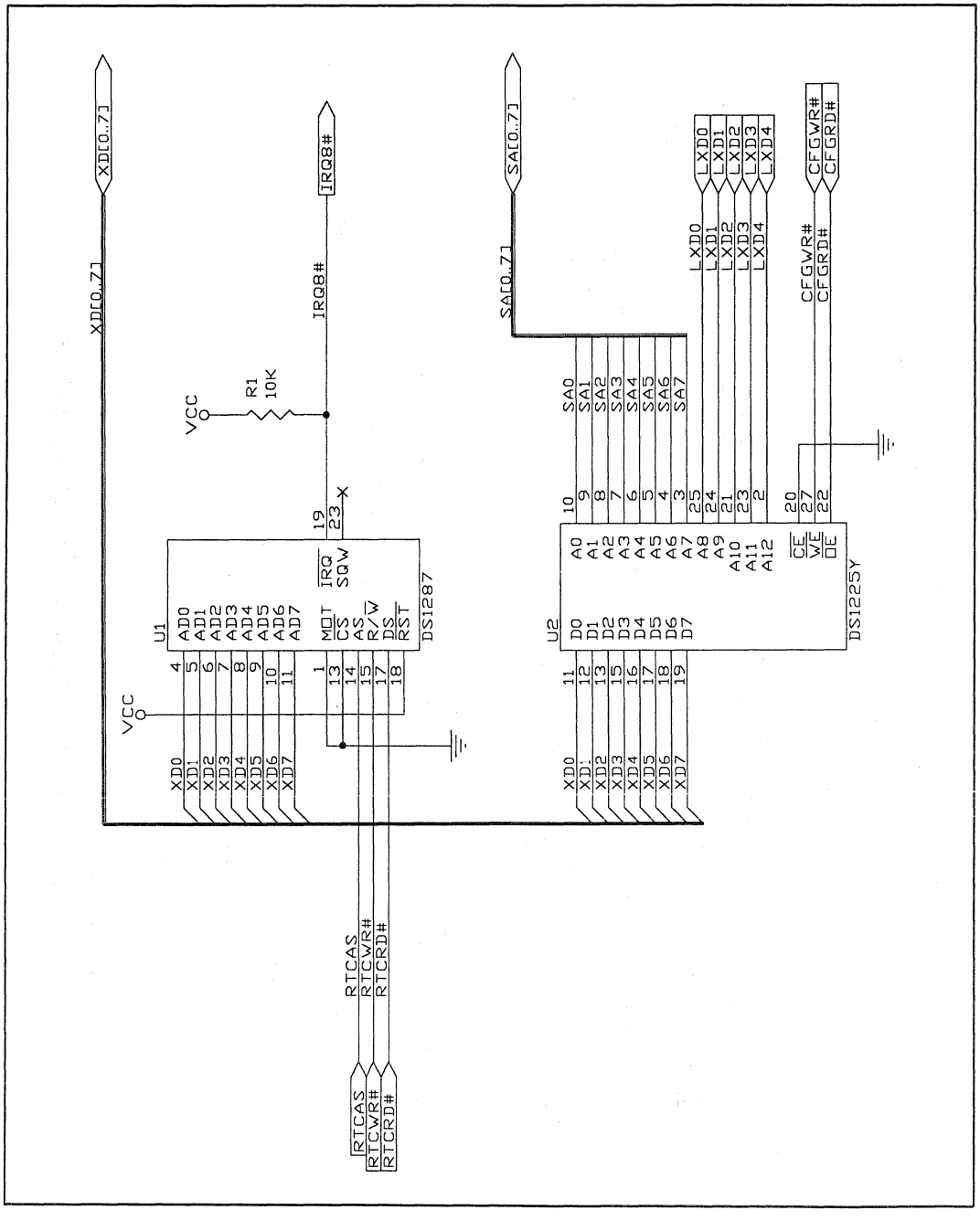

Figure 6. DS1287 w/ NVSRAM EISA or MCA Example

Table 5. bq3287 ISA (PC/AT) Parts List (Figure 4)

Item	Quantity	Reference	Part
1	1	R1	10K
2	1	U1	bq3287

Table 6. MC146818A w/ External SRAM Parts List (Figure 5)

Item	Quantity	Reference	Part
1	1	BT1	3.6V/60mAh
2	1	C1	0.0047
3	1	C2	27P
4	1	C3	10
5	1	C4	0.1
6	4	D1, D2, D3, D4	1N4148
7	1	JP1	HEADER-2
8	1	JP2	HEADER-4
9	1	Q1	2NN3906
10	1	Q2	2N3904
11	4	R1, R4, R7, R8	10K
12	1	R2	1K
13	1	R3	2M
14	1	R5	220
15	1	R6	39K
16	1	U1	MC146818A
17	1	U2	4069
18	1	U3	8Kx8 SRAM-LP
19	1	Y1	DT-26

Table 7. DS1287 w/ NVSRAM EISA or MCA Parts List (Figure 6)

Item	Quantity	Reference	Part
1	1	R1	10K
2	1	U1	DS1287 or bq3287
3	1	U2	DS1225Y or bq4010Y

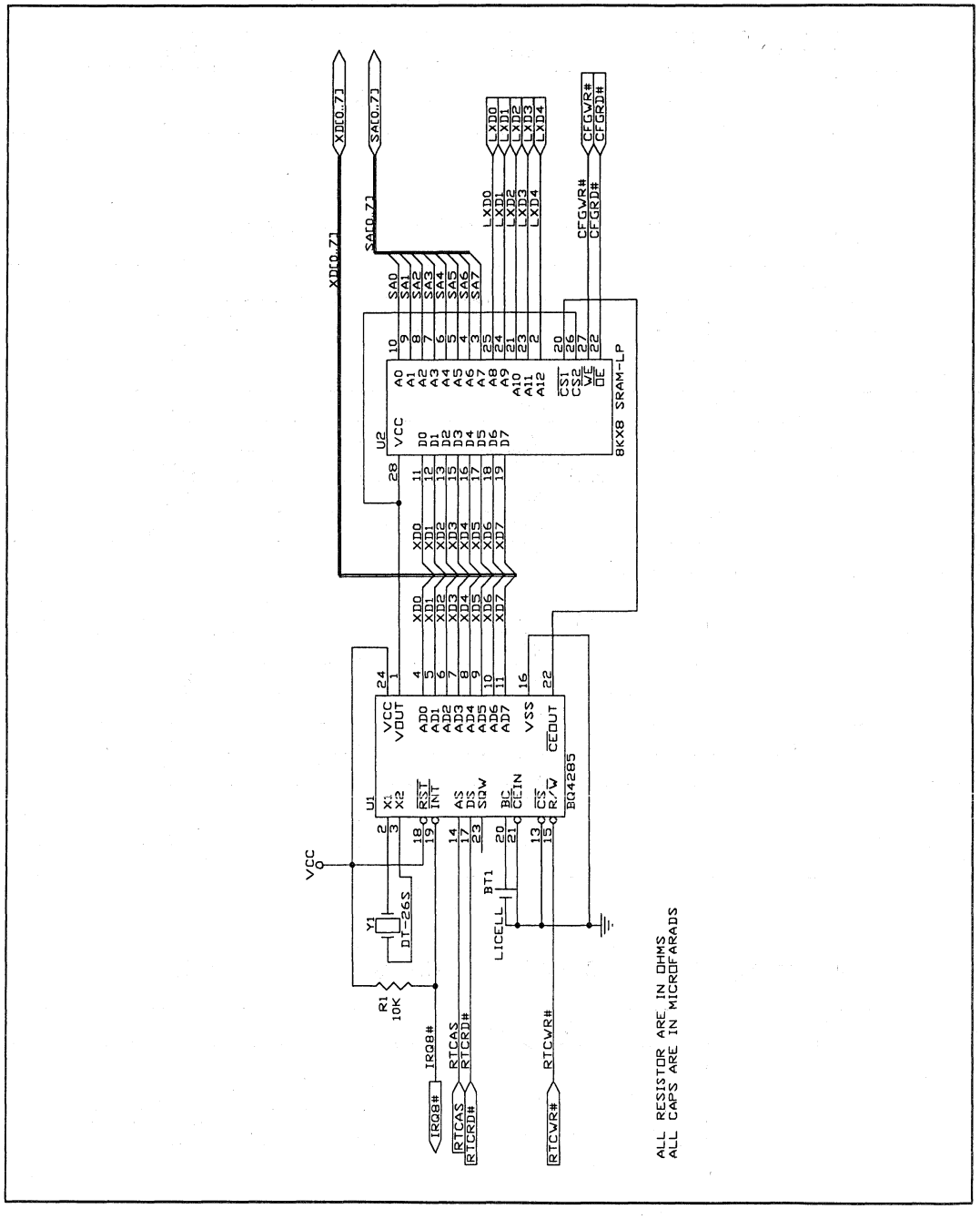

Figure 7. bq4285 EISA or MCA Example

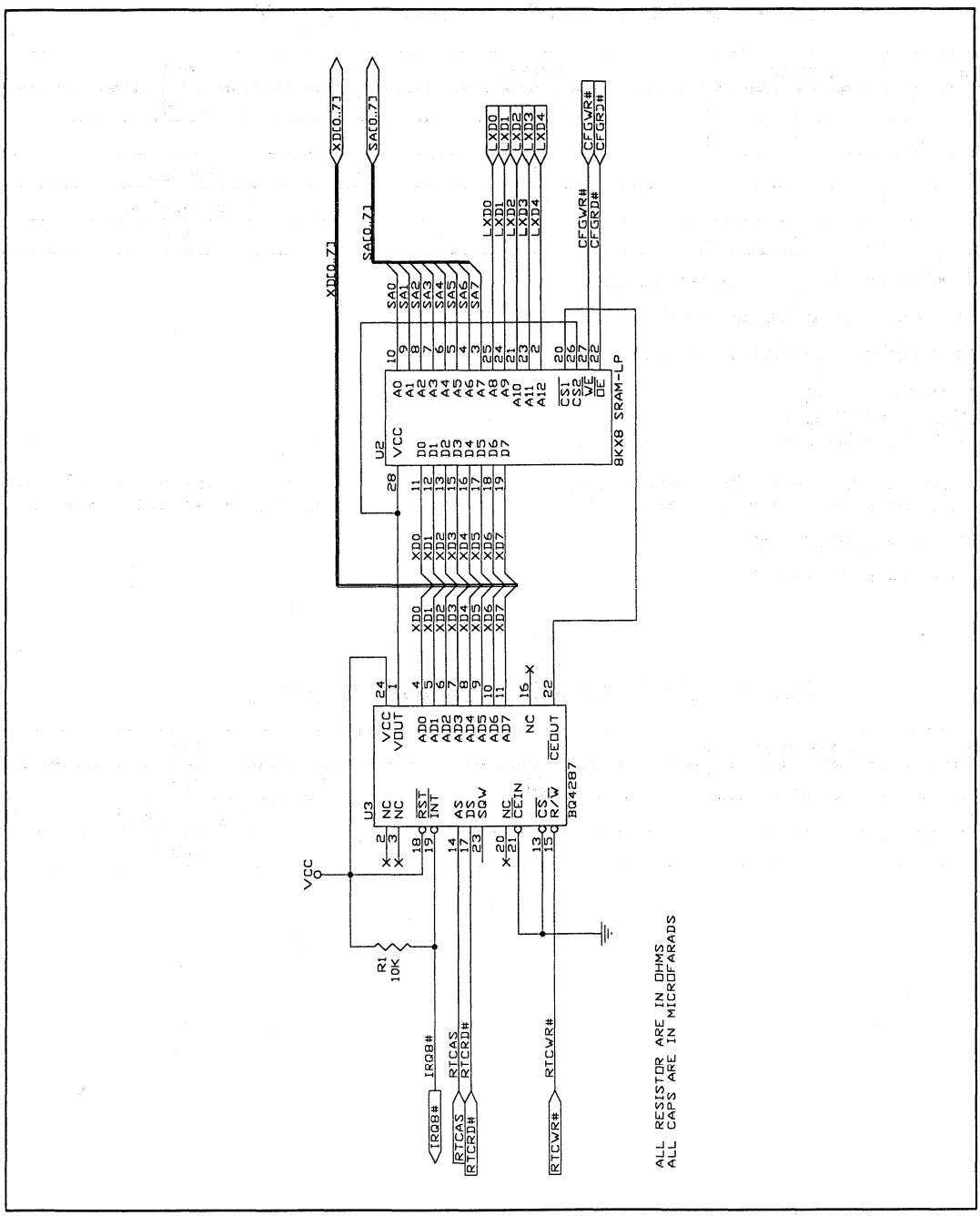

Figure 8. bq4287 EISA or MCA Example

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Table 8. bq4285 EISA or MCA Parts List (Figure 7)

Item	Quantity	Reference	Part
1	1	BT1	Li cell
2	1	R1	10K
3	1	U1	bq4285
4	1	U2	8Kx8 SRAM-LP
5	1	Y1	DT-26

Notes: Possible crystal/battery suppliers include:

- Daiwa DT-26 or equivalent crystal
- Rayovac/Panasonic lithium coin cells:

  BR1225 38–39mAh
  BR2032 180–200mAh
  BR2325 165–180mAh

  These cells and cells of other sizes are available "tabbed" for soldering directly into boards. These types of lithium coin cells are safe for all modes of transportation per U.S. Department of Transportation records.

- Rayovac U.L. #MH12542
- Panasonic U.L. #MH12210

Table 9. bq4287 EISA or MCA Parts List (Figure 8)

Item	Quantity	Reference	Part
1	1	R1	10K
2	1	U2	8Kx8 SRAM-LP
3	1	U3	bq4287

Using RAM Clear Function With bq3285/bq3287A RTCs

Introduction

The RAM clear function is useful for resetting data in battery-backed CMOS RAM. This function can, however, be detrimental when inadvertently activated. When activated, the RAM clear function on the bq3285 and bq3287A RTCs sets the contents of the 114 (or 242) bytes of CMOS RAM to "FF" (hex).

Figure 1 shows the circuit configuration required to use the RAM clear function. The Benchmarq RTC uses the on-chip time-base oscillator to de-bounce the momentary switch, SW1, over a period of 100 ms. This requires that the time-base oscillator and the divider chain must be turned on by writing a 02 (hex) in bit locations OSC2–OSC0 of register A. Although Figure 1 shows a momentary switch, an electronic signal can also be used with the same considerations.

All CMOS RAM locations are "cleared" when the Benchmarq RTC senses a low-level pulse of at least 100ms on the RAM clear pin, $\overline{RCL}$, when V_{CC} = 5V.

Clearing RAM

Follow these steps to clear RAM using the Benchmarq and Dallas Semiconductor RTCs:

1. Turn on the oscillator (this is a normal part of initialization when power is on).

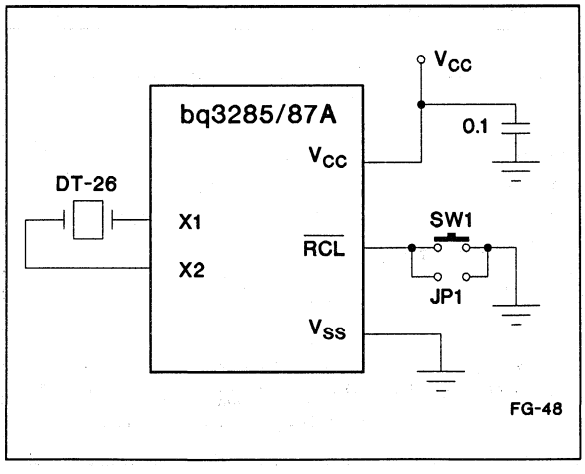


Figure 1. Recommended Hookup for RAM Clear Function

2. Clear the RAM: Jumper JP1.
3. Remove the JP1 jumper.

Implementation Differences

Although the hardware requirements for activating the Dallas Semiconductor RAM clear pin, $\overline{RCLR}$, are identical to those for activating the Benchmarq $\overline{RCL}$ pin, the function is implemented differently:

- Dallas Semiconductor's RAM clear function provides access to the internal lithium power source. ***Shorting $\overline{RCLR}$ to ground drains the lithium cell.***
- Benchmarq's $\overline{RCL}$ pin is internally de-bounced (oscillator on).
- Benchmarq's $\overline{RCL}$ pin is active when power is on.

Benchmarq Advantages

The Benchmarq RTCs have the following advantages over the Dallas Semiconductor parts:

1. When the Dallas Semiconductor $\overline{RCLR}$ pin is exposed to any low-impedance path including metal trays, conductive bags, conductive foam, ground, etc., the battery will be drained. This may severely limit the battery life of the RTC. The battery in the Benchmarq RTC will not be drained.
2. The Dallas Semiconductor RTC is prone to inadvertent clearing of RAM while the system is off because the RAM clear function is active when power is not valid.
3. The de-bouncing capability of the Benchmarq RTC prevents inadvertent clearing of the CMOS RAM as a result of spurious noise on the $\overline{RCL}$ pin.

BENCHMARQ

Time-Base Oscillator For bq3285/E/L/bq4285 RTCs

Introduction

The operation of the time-base oscillator is critical to the time-keeping functions of the bq3285/E/L and bq4285 series of Real-Time-Clocks. For simplicity, the term "RTC" refers to this product family.

This application note describes the on-chip crystal oscillator circuitry designed into the RTC and includes suggestions for achieving time-keeping accuracy and circumventing oscillator start-up problems.

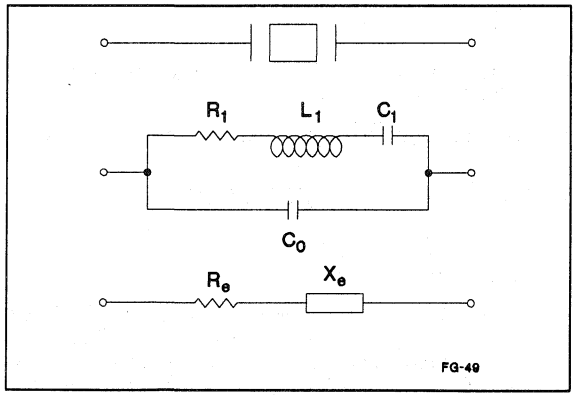


Figure 1. Equivalent Circuit of a Quartz Crystal

Time-Base Crystal

The RTC time-base oscillator is designed to work with an external piezoelectric 32.768kHz crystal. A crystal can be represented by its electrical equivalent circuit and associated parameters as shown in Figure 1 and Table 1, respectively.

L1, C1, and R1 form what is known as the motional arm of the circuit. C_0 is the sum of the capacitance between electrodes and the capacitance added by the leads and mounting structure of the crystal. The equivalent impedance of the crystal varies with the frequency of oscillation. Figure 2 shows the variation of the equivalent reactance, X_e, with respect to frequency.

Table 1. Crystal Parameters

Parameter	Symbol	Value	Unit
Nominal frequency	F	32.768	kHz
Load capacitance	C_L	6	pF
Motional inductance	L_1	9076.66	H
Motional capacitance	C_1	2.6×10^{-3}	pF
Motional resistance	R_1	27	KΩ
Shunt capacitance	C_0	1.1	pF

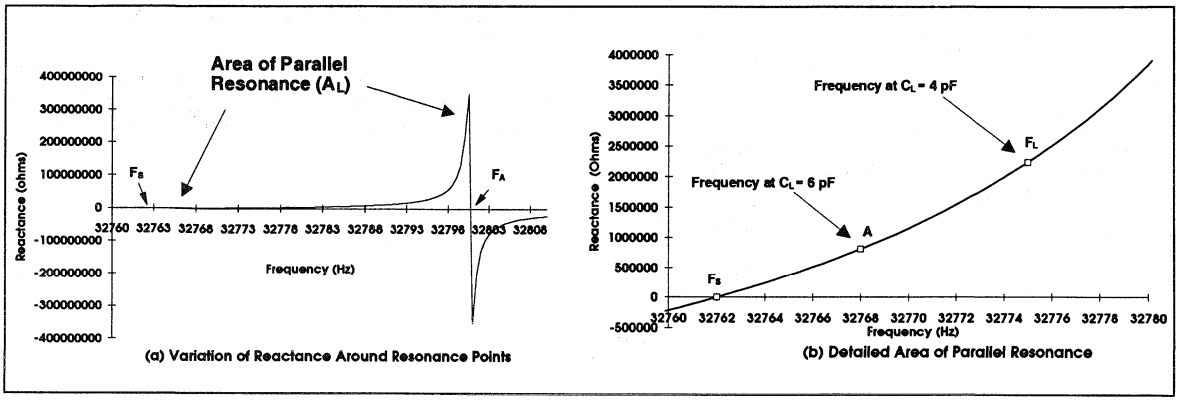


Figure 2. Equivalent Reactance Versus Frequency

There are two frequencies at which the crystal impedance appears purely resistive (X_e = 0). They are indicated by two points on the graph, known as the series resonant (F_S) and anti-resonant (F_A) frequencies. Oscillators operating the crystal at the resonant frequency (F_S) are termed series resonant circuits, whereas those that operate the crystal around Fa are termed parallel resonant. The Benchmarq RTC uses a parallel resonant oscillator circuit. The frequency of oscillation in this mode lies between F_S and F_A and is dictated by the effective load capacitance appearing across the crystal inputs, as explained below.

Benchmarq RTC Oscillator

The parallel resonant RTC oscillator circuit is comprised of an inverting micro-power amplifier with a PI-type feedback network. Figure 3 illustrates a block diagram of the oscillator circuit with the crystal as part of the PI-feedback network. The oscillator circuit ensures that the crystal is operating in the parallel resonance region (A_L in Figure 2) of the impedance curve.

The actual frequency at which the circuit will oscillate depends on the load capacitance, C_L. This parameter is the dynamic capacitance of the total circuit as measured or computed across the crystal terminals. A parallel resonant crystal like the DT-26 is calibrated at this load using a parallel resonant oscillator circuit. C_L is computed from C_{L1} and C_{L2} as given below:

$$C_L = (C_{L1} * C_{L2}) / (C_{L1} + C_{L2})$$

The RTC C_{L1} and C_{L2} values are trimmed to provide approximately a load capacitance (C_L) of 6pF across the crystal terminals. This is to match the specified load capacitance (6pF) at which the recommended DT-26 crystal is calibrated to resonate at the nominal frequency of 32.768kHz. Referring to the impedance graph of Figure 2, "A" indicates the point of resonance when C_L equals the specified load capacitance of the crystal.

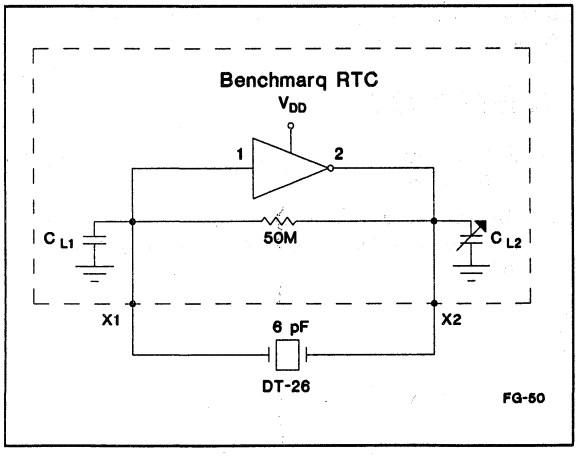


Figure 3. RTC Oscillator Circuit Block Diagram

Time-Keeping Accuracy

The accuracy of the frequency of oscillation depends on:

- Crystal frequency tolerance
- Crystal frequency stability
- Crystal aging
- Effective load capacitance in oscillator circuit
- Board layout

Crystal Frequency Tolerance

The frequency tolerance parameter is the maximum frequency deviation from the nominal frequency (in this case, 32.768 kHz) at a specified temperature, expressed in ppm of nominal frequency. In the case of the Grade A DT-26 crystal, this parameter is ± 20 ppm at 25°C.

Crystal Frequency Stability

This parameter, dependent on the angle and type of cut, is defined as the maximum frequency deviation from the nominal frequency over a specified temperature range, expressed in ppm or percentage of nominal frequency.

Figure 4 shows a typical curve of frequency variation with temperature for the KDS DT-26 crystal.

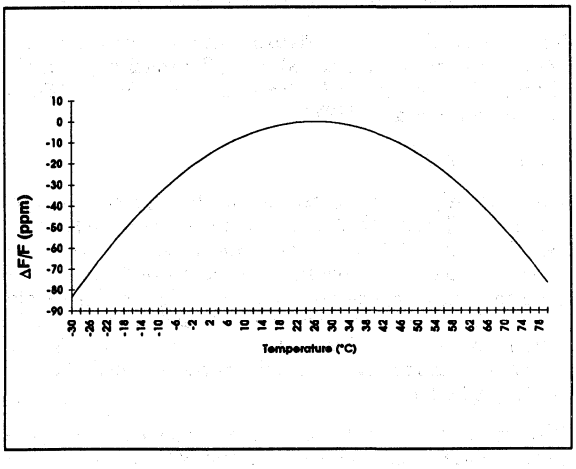


Figure 4. Typical Temperature Characteristics

Crystal Aging

As a crystal ages, some frequency shift may be observed. Drift with age is specified to be typically 4 ppm for the first year and 2 ppm per year for the life of the KDS DT-26 crystal.

Load Capacitance

For a parallel resonant calibrated crystal, the crystal manufacturer specifies the load capacitance at which the crystal will "parallel" resonate at the nominal frequency. From the graph of Figure 2, increasing the effective load capacitance by hanging additional capacitors on either of the X1 or the X2 pin will effectively lower the resonant frequency point "A" toward Fs. The deviation of the frequency F_L with load capacitance is given by:

$$F_L = F_S (1 + C_1 / (2 (C_0 + C_L)))$$

where C_1 is the crystal motional capacitance and C_0 is the crystal shunt stray capacitance, as explained above. C_L is the effective load capacitance across the crystal inputs.

Allowing for capacitance due to board layout traces leading to the X1 and X2 pins, the RTC is trimmed internally to provide an effective load capacitance of less than 6pF. Connecting a 6pF crystal directly to the X1 and X2 pins will cause the clock to oscillate approximately 24 ppm faster than the nominal frequency of 32.768kHz, for reasons explained earlier.

For maximum accuracy, it is recommended that a small trim capacitor (< 8pF) be hooked to the X2 pin to move the resonant point closer to the nominal frequency. The graph of Figure 5 shows the variation of frequency with additional load capacitance on the X2 pin of the RTC.

Translating the data in Figure 5 into a practical rule of thumb: for every additional 1.54pF capacitance on the X2 pin, the frequency will decrease by 0.8Hz or a ΔF/F of -24.4ppm around 32.768kHz.

Board Layout

Given the high-input impedance of the crystal input pins X1 and X2, care should be taken to route high-speed switching signal traces away from them. Preferably a ground-plane layer should be used around the crystal area to isolate capacitive-coupling of high-frequency signals. The traces from the crystal leads to the X1, X2 pins must be kept short with minimal bends. A good rule of thumb is to keep the crystal traces within 5mm of the X1, X2 pins.

Finally, a 0.1μF ceramic by-pass capacitor should be placed close to the V_{CC} pin of the RTC to provide an improved supply into the clock.

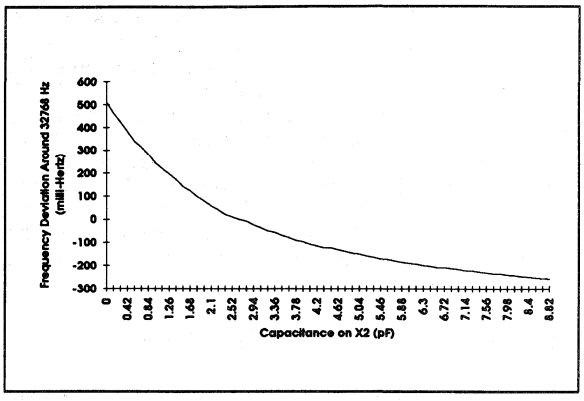


Figure 5. Frequency Variation Versus Load Capacitance

Oscillator Start-up

Barring accuracy issues, the RTC will oscillate with any 32.768kHz crystal. When hooked to the X1, X2 pins in certain configurations, however, passive components can lead to oscillator start-up problems:

- Excessive loading on the crystal input, pins X1, X2.
- Use of a resistive feedback element across the crystal.

Figure 6 shows "good" and "bad" circuit configurations for the RTC oscillator.

Values above 10pF on either the X1 or X2 pin must be avoided. The feedback element is built into the RTC for start-up, and no resistive feedback external to the part is required.

References

1. KDS America, *Quartz Crystals and Oscillators User's Guide.*
2. Eaton, S. S., *Timekeeping Advances Through COS/MOS Technology*, RCA Application Note ICAN 6086.

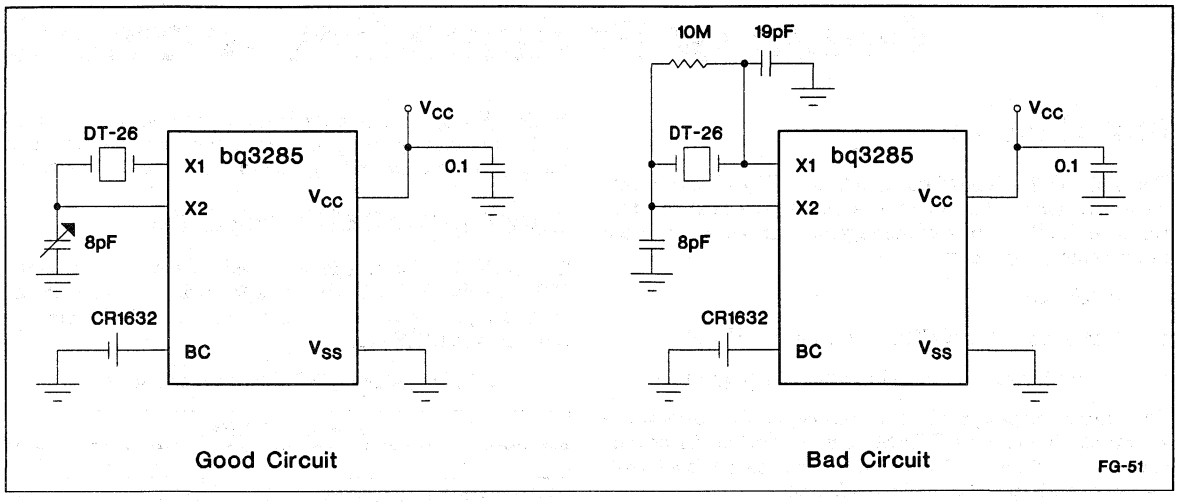


Figure 6. Typical Crystal Hookup Circuits

4

BENCHMARQ Using the bq3285/7E in a Green or Portable Environment

Introduction

The bq3285/7E Real-Time Clock is a PC/AT-compatible real-time clock that incorporates three enhanced features to facilitate power management in Green desktop or portable computers:

- 32kHz output
- 128 extra bytes of CMOS nonvolatile SRAM
- Alarm interrupt active in battery-backup mode

The 32kHz output provides a clock signal for power management timers and DRAM refresh control in power-sensitive systems. The output must be enabled with software and appears on the SQW pin.

Most RTCs and chip sets on the market have 114 bytes of general-purpose CMOS RAM. The bq3285/7E adds 128 additional bytes of memory to give the designer and user greater flexibility in defining system configuration settings. The added CMOS RAM is paged to by asserting the EXTRAM pin on the bq3285/7E. It can be used to store power management time-out settings, plug-and-play configuration data, or additional chip set parameters.

The bq3285/7E allows the alarm interrupt from the real-time clock to be active when no power is applied to the part. This enables a properly designed system to be programmed to "wake-up" from a power-off state and perform a function, minimizing the system on time.

32.768kHz Output

The bq3285/7E can be configured to generate a buffered 32.768kHz output on the SQW pin. This signal can be used as a timebase for system timers in a power management environment and as a clock reference for DRAM refresh.

In a Green or portable system, a number of timers are needed to track system and peripheral activity in order to enter different power states and turn off peripherals like hard drives and monitors. For example, a power-managed system may require countdown power state timers to transition the computer from full operation to doze, standby, and suspend states. Peripheral timers may be needed to count how long each peripheral has been inactive. Some chip sets allow the DRAM refresh rate to be slowed to rates based on the 32kHz timer when in suspended states. The power management controller (PMC) on the core logic takes the timer inputs and minimizes system power consumption by generating the appropriate control signals to the rest of the system.

Enabling the 32.768kHz Output

The 32.768kHz output is only available when V_{CC} to the RTC is valid (5V ± 10%). The following settings in the control registers A, B, and C enable the 32.768kHz output onto the SQW pin.

1. Set the Register A OS2–OS0 bits as shown:

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0
-	0	1	1	-	-	-	-

2. Set the Register B SQWE bit as shown:

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	HF	DSE	RS0
-	-	-	-	1	-	-	-

3. Set the Register C 32KE bit as shown:

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0
-	-	-	-	-	1	-	-

The above settings do not affect the periodic interrupt rate or other time-keeping functions.

Disabling the 32.768kHz Output

The 32.768kHz output is disabled under the following conditions.

1. Clearing either of the SQWE/32KE bits or the OS1/OS0 bits in the above registers.
2. Asserting the $\overline{RST}$ pin low.
3. Putting the device in battery-backup mode ($V_{CC} < V_{BC}$).

Extra CMOS NVSRAM

Because bit 7 at I/O port address 70H in a PC/AT environment is the NMI, additional I/O ports are needed to access the extra 128 bytes of CMOS RAM. The following table shows the I/O ports used by the PC/AT BIOS to access CMOS RAM. Note the CMOS RAM includes the RTC information in the uppermost 14 locations.

I/O Address	Read/ Write	Description
070H	W	CMOS RAM address register port, where: Bit 7 = 1; NMI disabled = 0; NMI enabled Bits 6–0 = Register and CMOS RAM address
071H	R/W	CMOS RAM data register port
074H	W	Extended CMOS RAM address register port, least-significant byte
075H	W	Extended CMOS RAM address register port, most-significant byte
076H	R/W	Extended CMOS RAM data register port

The two CMOS RAM data areas are shown below.

Data Area	I/O Locations	Size (bytes)	Description
Default CMOS Data Area	070H and 071H	Default: 64 Maximum: 128	All BIOS variations use this area to store RTC, POST, and system configuration data.
Extended CMOS RAM Data Area	074H, 075H, and 076H	Default: 2K Maximum: 64K	The PS/2 uses this area to store POS data. The Intel SL uses 074H and 076H to provide "extended" 128 CMOS RAM bytes for APM data.

The EXTRAM pin controls access to the extra 128 bytes of memory on the bq3285/7E. The EXTRAM signal can be generated in two ways:

1. Hook up SA3, SA2, or SA1 from the ISA address bus to the EXTRAM pin. The address/data ports through which the "extra" 128 bytes are accessed depend on which address line is used, as shown in the following table.

Address Line	I/O Ports	Read/ Write	Description
SA3	078H	W	Extra CMOS RAM address register port, where: Bit 7 = Reserved Bits 6–0 = Extra CMOS RAM address
SA3	079H	R/W	Extra CMOS RAM data register port
SA2	074H	W	Same as 078H
SA2	075H	R/W	Same as 079H
SA1	072H	W	Same as 078H
SA1	073H	R/W	Same as 079H

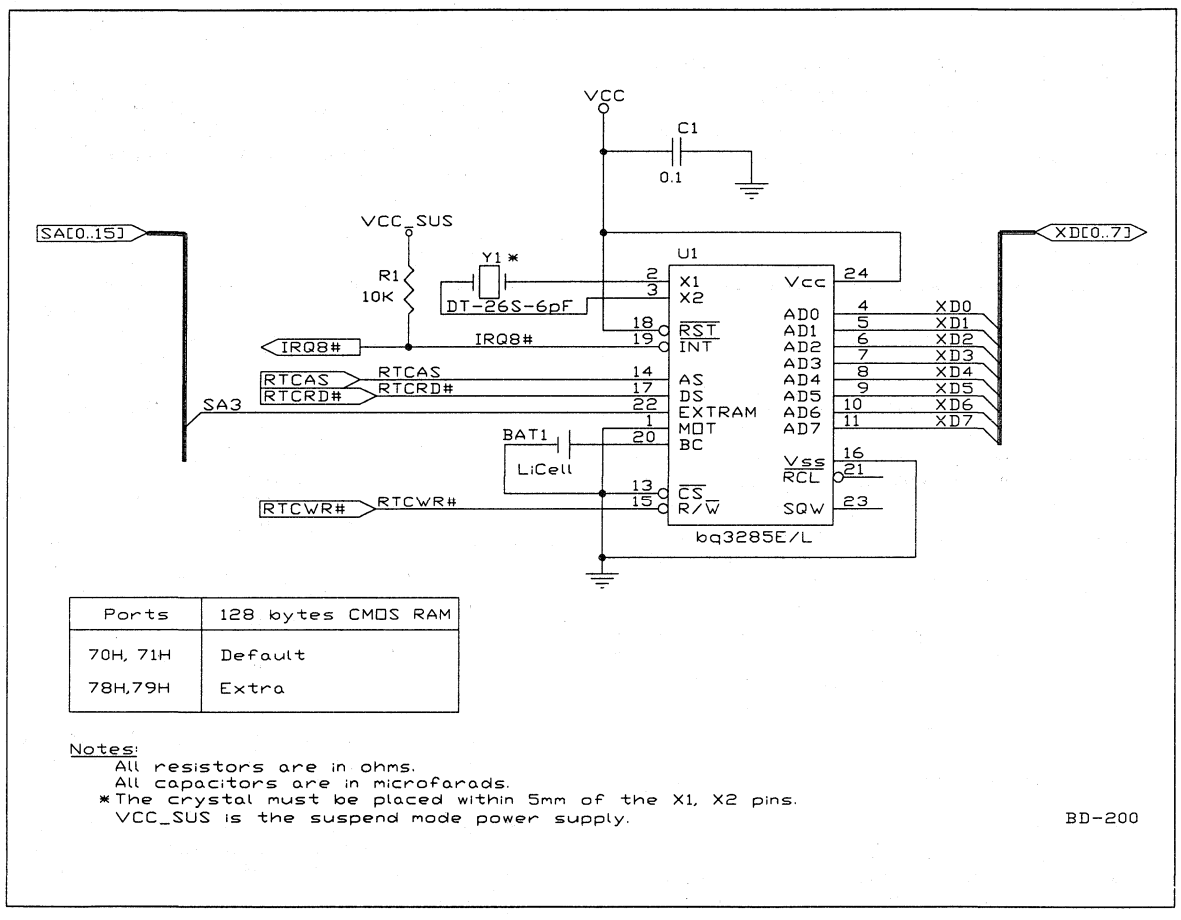
   Any one of the above I/O port pairs that asserts RTC control signal AS, DS, or $\overline{WR}$ should be selected.

2. Hook up an unused general-purpose I/O port pin to EXTRAM pin. When this pin is asserted high on a write to the assigned I/O port, successive accesses to port 070H and 071H are directed to the extra 128-byte RAM bank.

Refer to Figure 1 for a diagram of a complete PC/AT interface.

Alarm Interrupt

The alarm interrupt on the bq3285/7E functions with or without V_{CC} power. It can be used in a power-managed system to wake the system up from suspend mode or turn the system or parts of the system on from the power-off mode. In suspend mode, most of the computer is shut down except for the power management controller and the DRAM. The PMC needs an interrupt from a push-button resume switch, an incoming modem ring, or the RTC to resume operation. The bq3285/7E RTC can either be left on or turned off during suspend mode depending on the level of functionality required. In 0V suspend mode, the 32kHz output may not be needed because all the DRAM information is stored to disk and refresh is not required. In this case, the bq3285/7E can



Ports	128 bytes CMOS RAM
70H, 71H	Default
78H,79H	Extra

Notes:
All resistors are in ohms.
All capacitors are in microfarads.
*The crystal must be placed within 5mm of the X1, X2 pins.
VCC_SUS is the suspend mode power supply.

BD-200

Figure 1. bq3285/7E PC/AT Design Example

be powered off during suspend and still be able to supply the alarm interrupt to the power management controller. In 3V/5V suspend where the DRAM is kept alive, the bq3285/7E should be in the powered-up mode. This has little impact on power consumption, however, because the bq3285/7E has low standby current when deselected.

The bq3285/7E can be also be used to turn a system on from the power-off mode for periods of short duration. Figure 2 shows how this could be implemented. The $\overline{INT}$ pin alerts the power management controller, which in turn activates a p-FET to turn on the necessary subsystems to perform the required function. After completion of the task, the system shuts down except for the power management controller.

PC/AT Environment

Most advanced power-managed chip sets have a direct input for a 32kHz signal. A common way of generating this signal is to use a CMOS buffered inverter like the MC14069 with a 32.768kHz quartz crystal and R-C components. The bq3285/7E contains its own built-in 32.768kHz quartz crystal for the real-time clock oscillator. To eliminate redundancy and component count, the 32kHz output on the bq3285/7E SQW pin can be used in place of the MC14069, external crystal, and other passive components. The SQW pin has not been used in PC/AT designs in the past, so using it for this function does not impact other aspects of the motherboard design.

Figure 3 shows a real-time clock and timer generation using the MC146818A and the MC14069 in conjunction with Green core logic chips. Figure 4 shows the much simplified bq3285/7E design using the 32kHz output on the SQW pin and the extra NVSRAM enabled. Ports 70H and 71H address the upper 128 bytes of CMOS RAM including the RTC information. Ports 78H and 79H address the extra 128 bytes of CMOS RAM.

From a software standpoint, the PC BIOS must incorporate the appropriate routine to enable the 32kHz output and use the extra NVSRAM. The 32kHz enable routine should be placed as part of the system cold-boot initialization procedure.

Other Considerations

If the height of the bq3285/7E DIP module is an issue in portable designs, the part is also available in a 300-mil SOIC and a 150-mil SSOP (bq3285ES and bq3285ESS). Both variations provide direct connections for an external crystal and battery. The devices are also available with 3V V_{CC} operation (bq3285LS and bq3285LSS) for use in 3V systems.

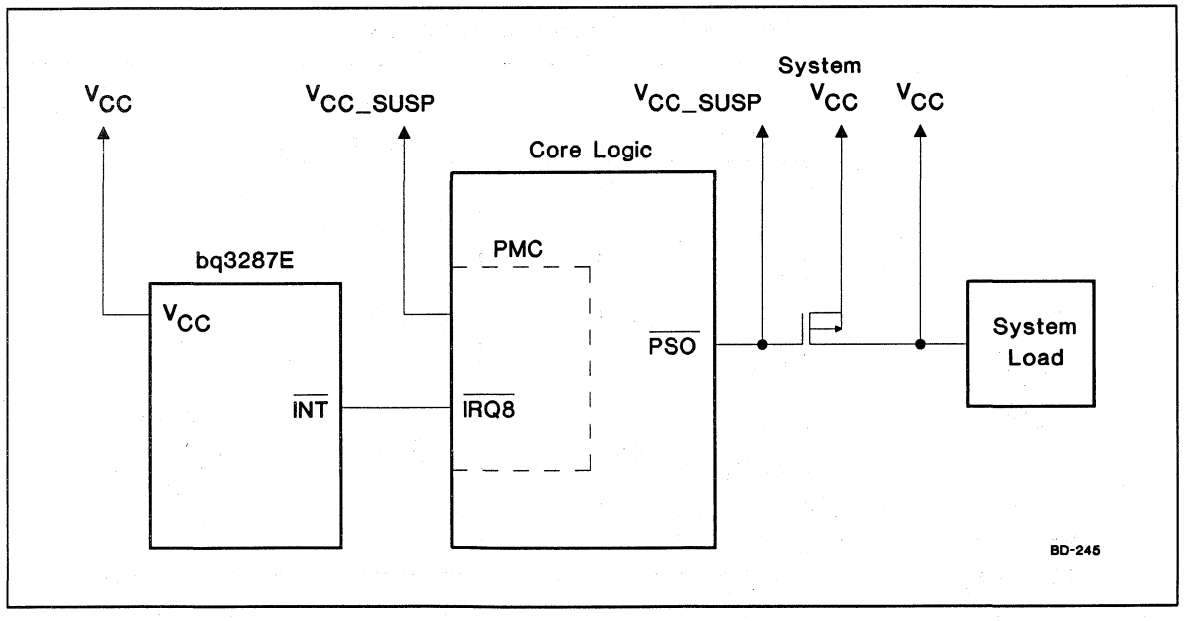


Figure 2. System Wake-up Alarm

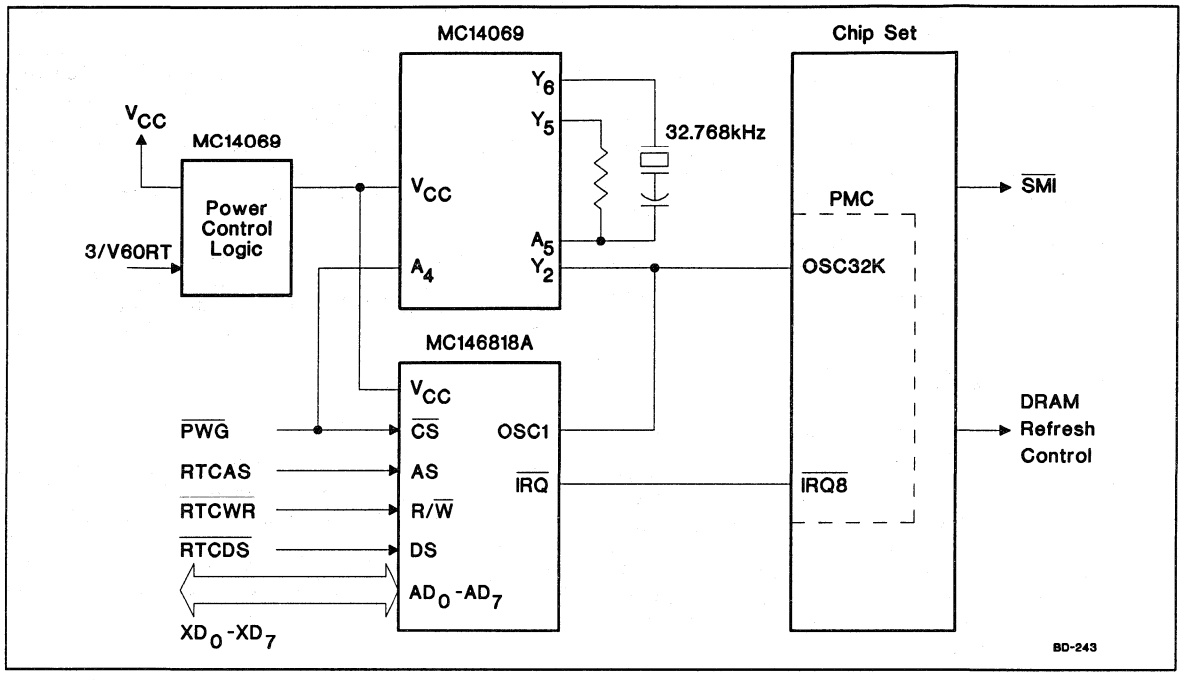


Figure 3. MC14069 Implementation

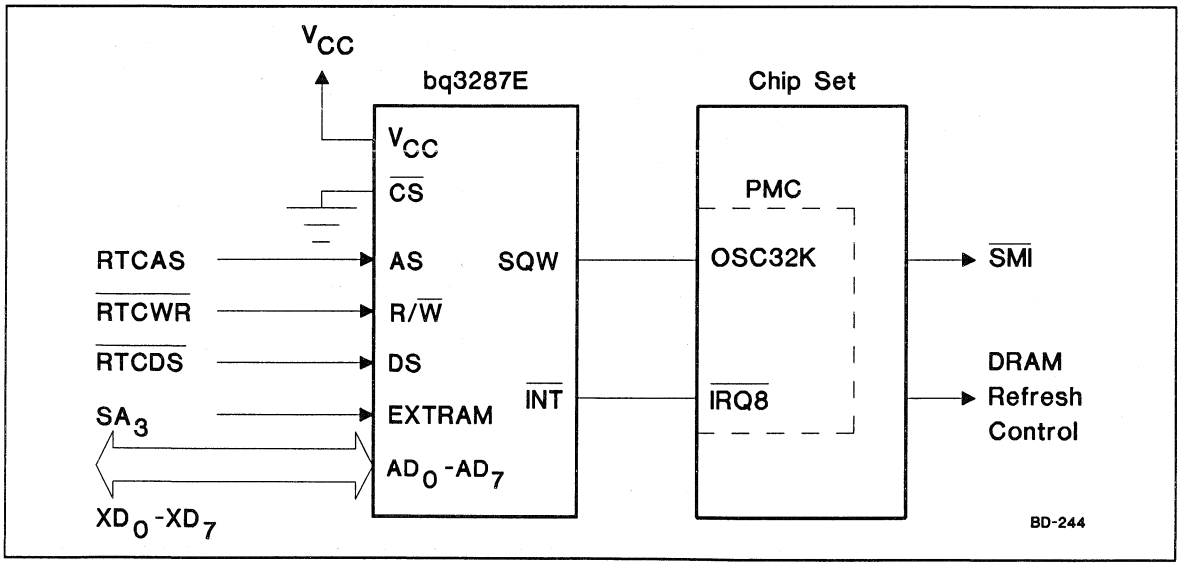


Figure 4. bq3285/7E Implementation

bq4010/bq4010Y

8Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 8K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

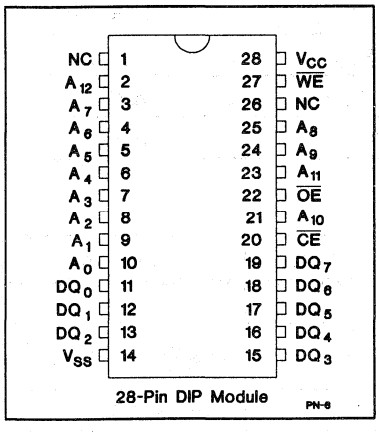
The CMOS bq4010 is a nonvolatile 65,536-bit static RAM organized as 8,192 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4010 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4010 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

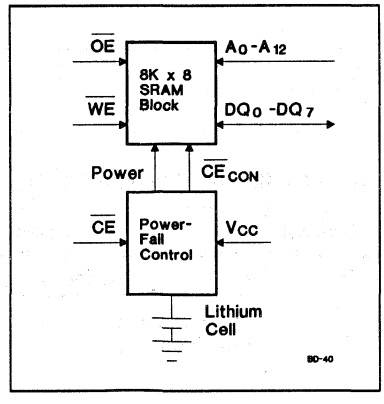
Pin Connections



Pin Names

A_0 -A_{12}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4010 -70	70	-5%	bq4010Y -70	70	-10%
bq4010 -85	85	-5%	bq4010Y -85	85	-10%
bq4010 -150	150	-5%	bq4010Y -150	150	-10%
bq4010 -200	200	-5%	bq4010Y -200	200	-10%

Functional Description

When power is valid, the bq4010 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4010 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4010 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4010Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4010 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4010Y/bq4010Y-xxxN
		4.75	5.0	5.5	V	bq4010
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	65	75	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4010
		4.30	4.37	4.50	V	bq4010Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

5

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

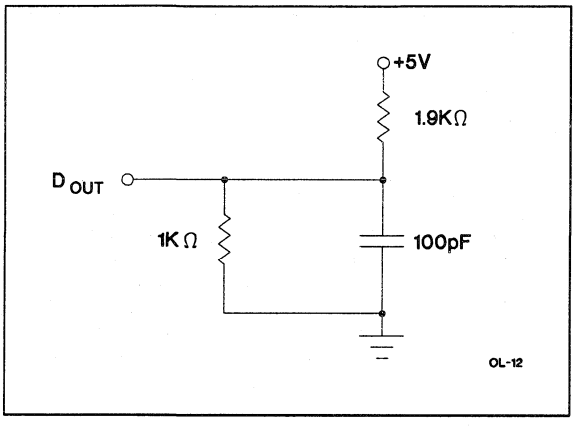


Figure 1. Output Load A

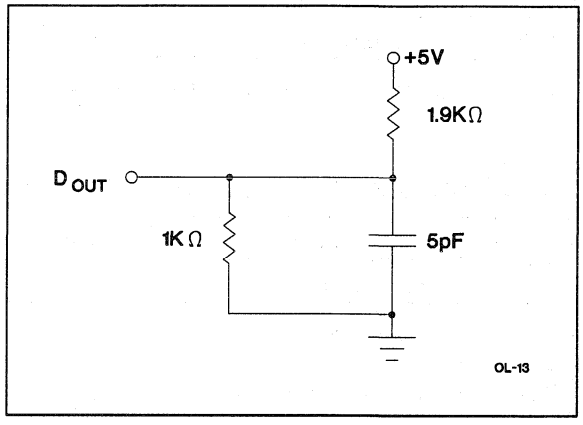
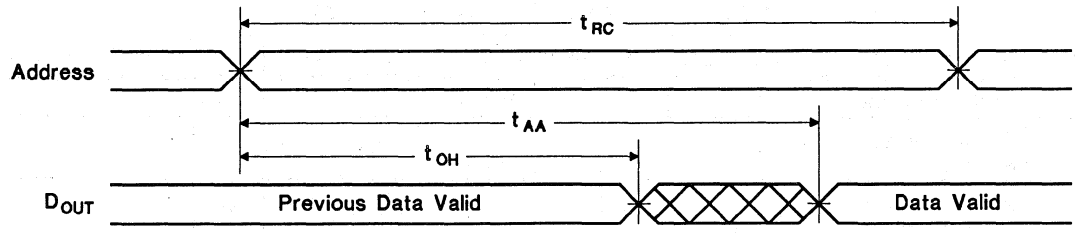


Figure 2. Output Load B

Read Cycle (T_A = TOPR, V_{CC}min ≤ V_{CC} ≤ V_{CC}max)

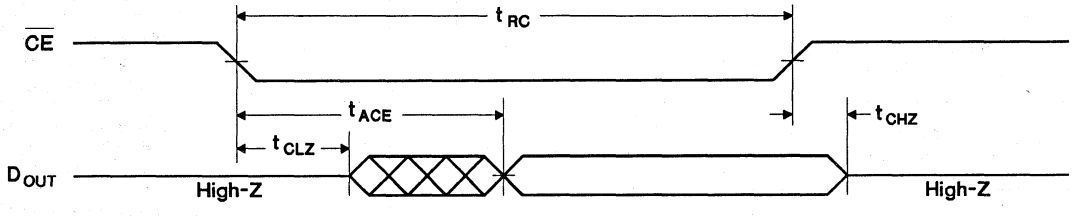
Symbol	Parameter	-70/-70N		-85/-85N		-150/-150N		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	85	-	150	-	200	-	ns	
t_{AA}	Address access time	-	70	-	85	-	150	-	200	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	85	-	150	-	200	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	45	-	70	-	90	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	10	-	10	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	40	0	60	0	70	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	30	0	50	0	70	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



RC-1

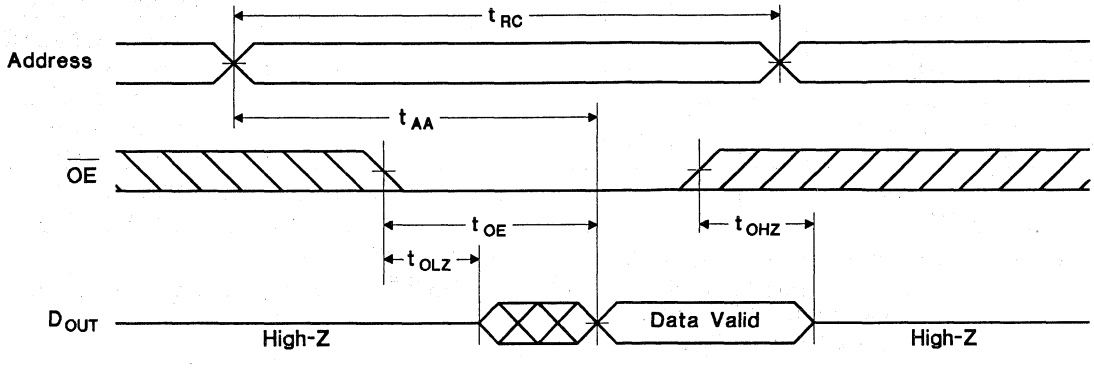
Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

5

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

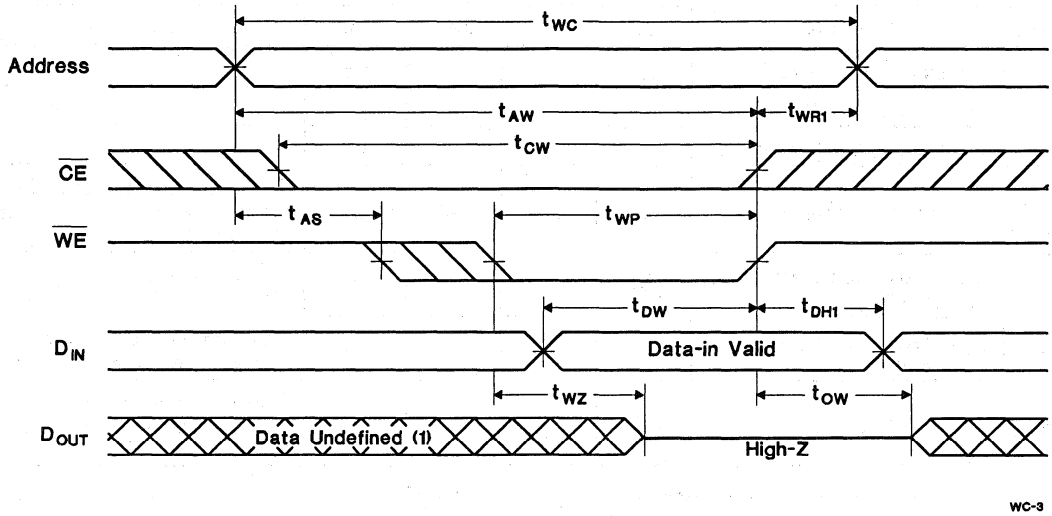
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	-70/-70N		-85/-85N		-150/-150N		-200		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	85	-	150	-	200	-	ns	
t_{CW}	Chip enable to end of write	55	-	75	-	100	-	150	-	ns	(1)
t_{AW}	Address valid to end of write	55	-	75	-	90	-	150	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	65	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	35	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	0	-	0	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	0	30	0	50	0	70	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	5	-	5	-	5	-	ns	I/O pins are in output state. (5)

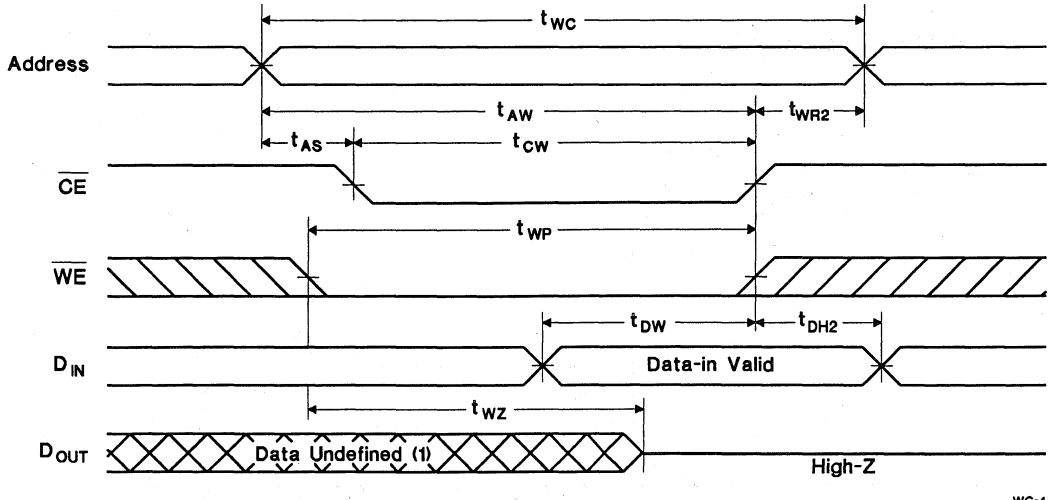
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

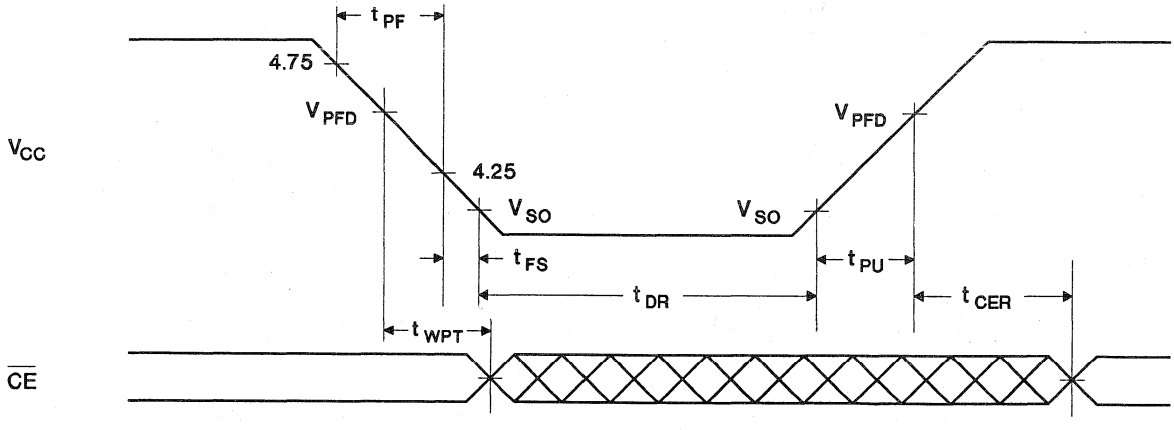
Power-Down/Power-Up Cycle ($T_A = T_{OPR}$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{DR-N}	Data-retention time in absence of V_{CC}	6	-	-	years	T_A = 25°C (2); industrial temperature range (-N) only.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-8

Data Sheet Revision History

Change No.	Page No.	Description
1	5-2, 5-3, 5-4, 5-6, 5-8, 5-9	Added industrial temperature range for bq4010YMA-85N and -150N.
2	5-1, 5-4, 5-6, 5-9	Added 70 ns speed grade for bq4010-70 and bq4010Y-70 and added industrial temperature range for bq4010YMA-70N.

Notes: Change 1 = Sept 1991 B changes from Sept. 1990 A.
Change 2 = Feb. 1994 C changes from Sept. 1991 B.

Ordering Information

bq4010 MA -

- Temperature:
  - blank = Commercial (0 to +70°C)
  - N = Industrial (-40 to +85°C)*
- Speed Options:
  - 70 = 70 ns
  - 85 = 85 ns
  - 150 = 150 ns
  - 200 = 200 ns
- Package Option:
  - MA = A-type module
- Supply Tolerance:
  - no mark = 5% negative supply tolerance
  - Y = 10% negative supply tolerance
- Device:
  - bq4010 8K x 8 NVSRAM

*Note: Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

5

bq4011/bq4011Y

32Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 28-pin 32K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

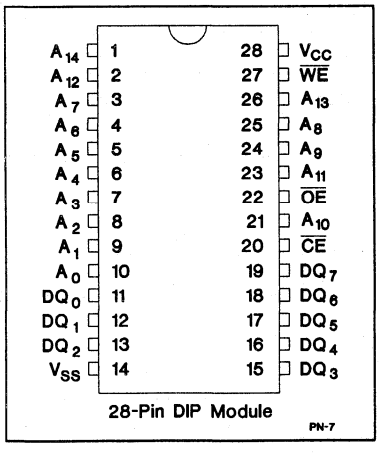
The CMOS bq4011 is a nonvolatile 262,144-bit static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4011 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4011 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

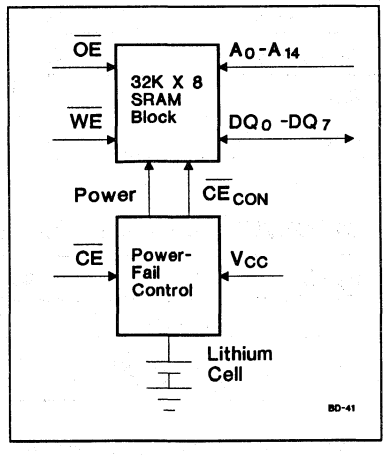
Pin Connections



Pin Names

A_0 -A_{14}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4011 -70	70	-5%	bq4011Y -70	70	-10%
bq4011 -100	100	-5%	bq4011Y -100	100	-10%
bq4011 -150	150	-5%	bq4011Y -150	150	-10%
bq4011 -200	200	-5%	bq4011Y -200	200	-10%

Functional Description

When power is valid, the bq4011 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4011 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4011 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4011Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4011 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4011Y/bq4011Y-xxxN
		4.75	5.0	5.5	V	bq4011
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2V
I_{CC}	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4011
		4.30	4.37	4.50	V	bq4011Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

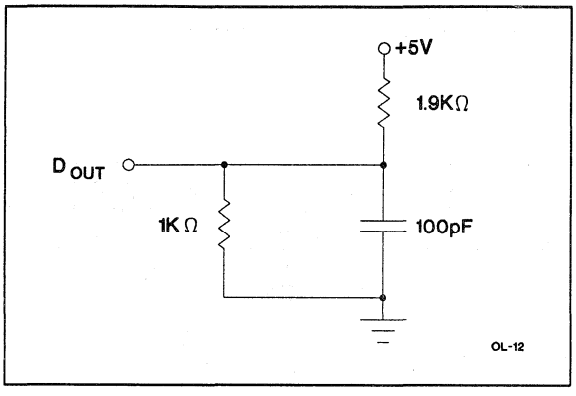


Figure 1. Output Load A

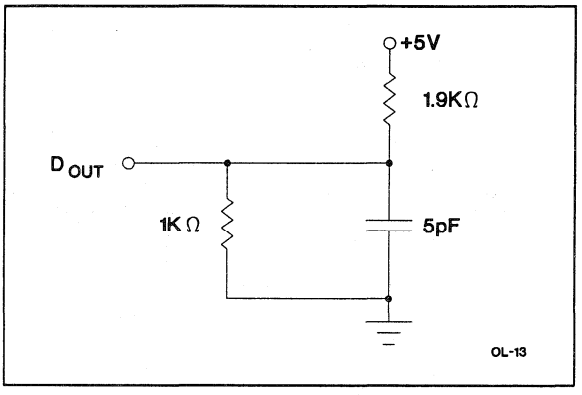
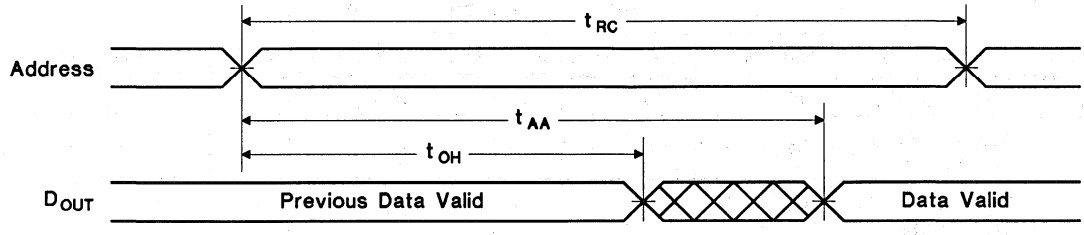


Figure 2. Output Load B

Read Cycle ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

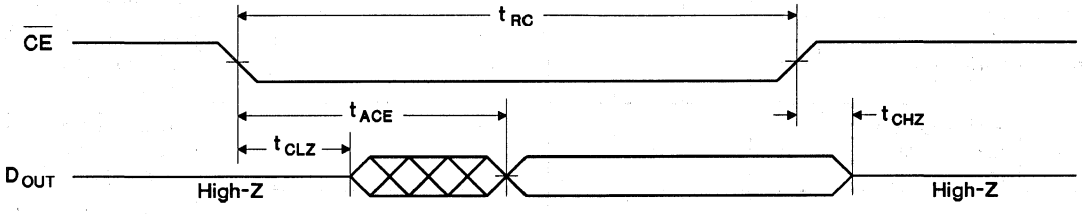
Symbol	Parameter	-70/-70N		-100		-150/-150N		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	100	-	150	-	200	-	ns	
t_{AA}	Address access time	-	70	-	100	-	150	-	200	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	100	-	150	-	200	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	50	-	70	-	90	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	10	-	10	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	5	-	5	-	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	40	0	60	0	70	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	0	50	0	70	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



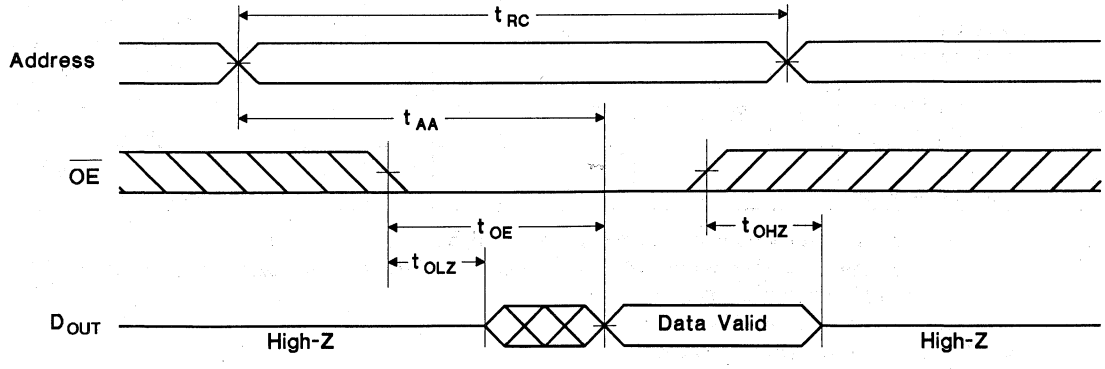
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

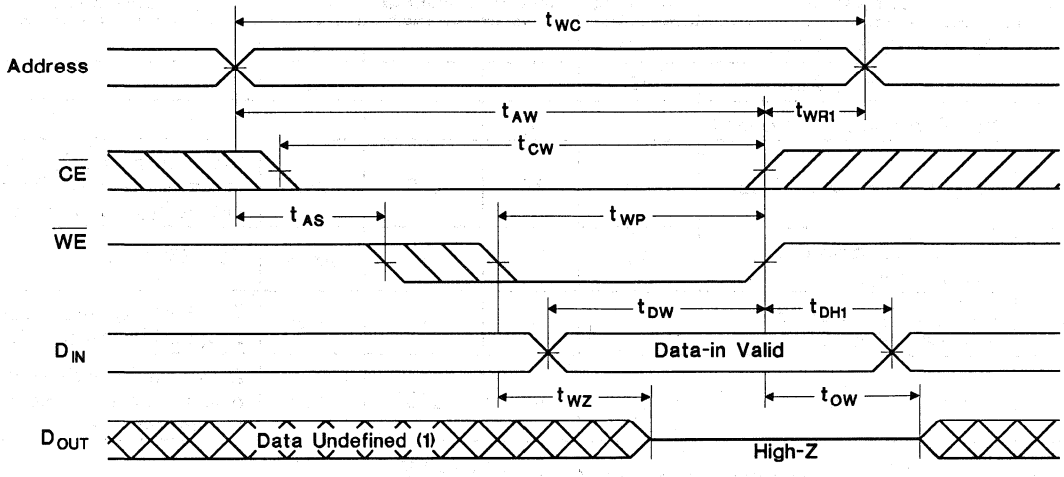
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	-70		-100		-150/-150N		-200		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	100	-	150	-	200	-	ns	
t_{CW}	Chip enable to end of write	55	-	90	-	100	-	150	-	ns	(1)
t_{AW}	Address valid to end of write	55	-	80	-	90	-	150	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	75	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	40	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{CE}$ going high to end of write cycle.(4)
t_{WZ}	Write enabled to output in high Z	0	25	0	35	0	50	0	70	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	5	-	5	-	5	-	ns	I/O pins are in output state. (5)

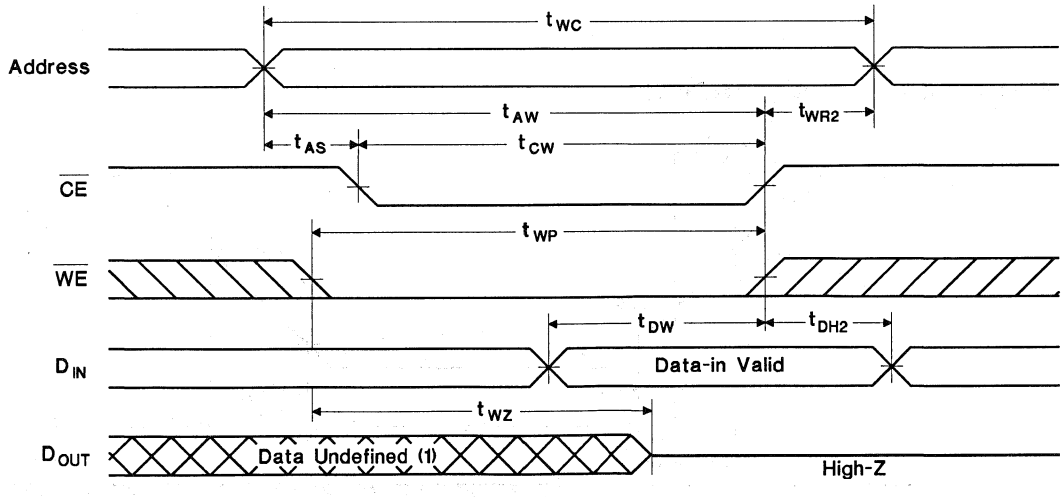
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

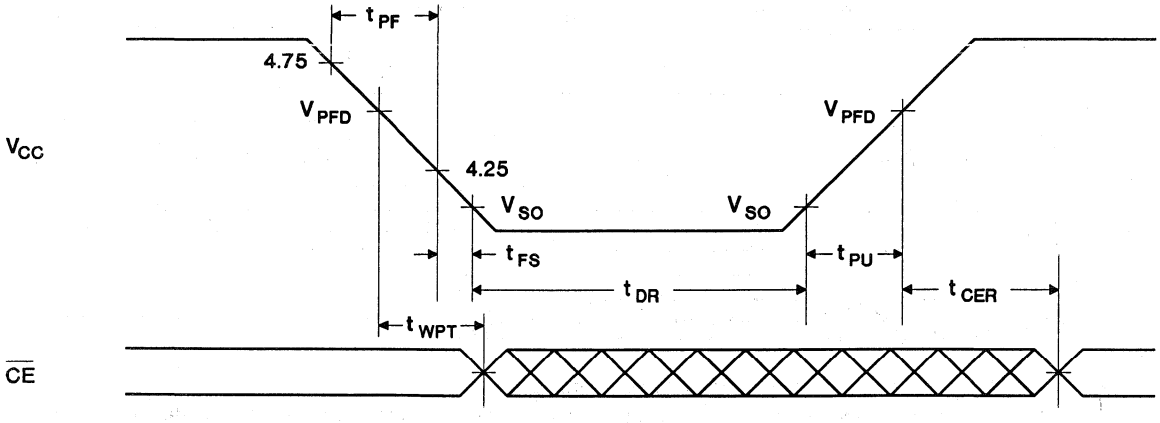
Power-Down/Power-Up Cycle (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	TA = 25°C. (2)
t_{DR-N}	Data-retention time in absence of V_{CC}	6	-	-	years	T_A = 25°C (2); industrial temperature range (-N) only.
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



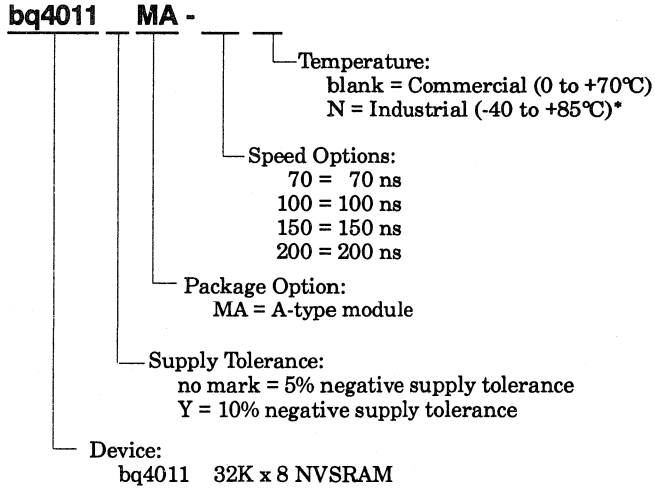
PD-B

Data Sheet Revision History

Change No.	Page No.	Description
1	5-12, 5-13, 5-14, 5-16, 5-18, 5-19	Added industrial temperature range for bq4011YMA-150N.
2	5-11, 5-14, 5-16, 5-19	Added 70 ns speed grade for bq4011-70 and bq4011Y-70 and added industrial temperature range for bq4011YMA-70N.

Notes: Change 1 = Sept 1992 B changes from Sept. 1990 A.
Change 2 = Aug. 1993 C changes from Sept. 1991 B.

Ordering Information



***Note:** Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

5

bq4013/bq4013Y

128Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 128K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4013 is a nonvolatile 1,048,576-bit static RAM organized as 131,072 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

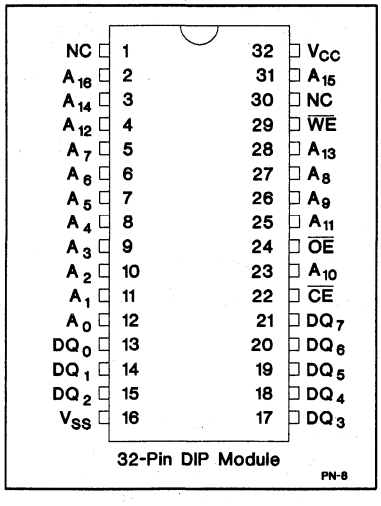
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4013 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4013 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

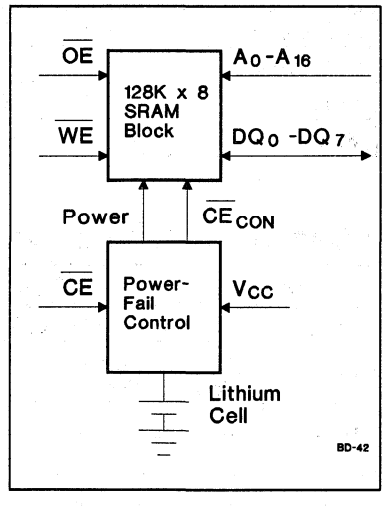
Pin Connections



Pin Names

A_0-A_{16}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4013-70	70	-5%	bq4013Y-70	70	-10%
bq4013-85	85	-5%	bq4013Y-85	85	-10%
bq4013-120	120	-5%	bq4013Y-120	120	-10%

Functional Description

When power is valid, the bq4013 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4013 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4013 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4013Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4013 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4013Y/bq4013Y-xxxN
		4.75	5.0	5.5	V	bq4013
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	4	7	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, 0V ≤ $V_{IN} \leq$ 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	75	105	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4013
		4.30	4.37	4.50	V	bq4013Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	10	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

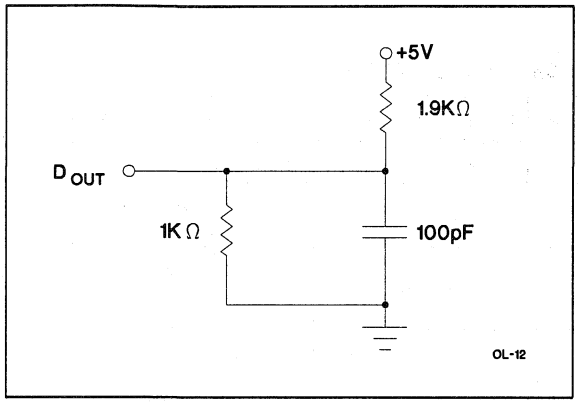


Figure 1. Output Load A

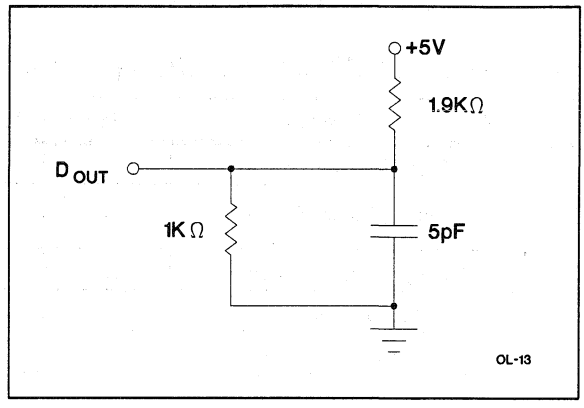
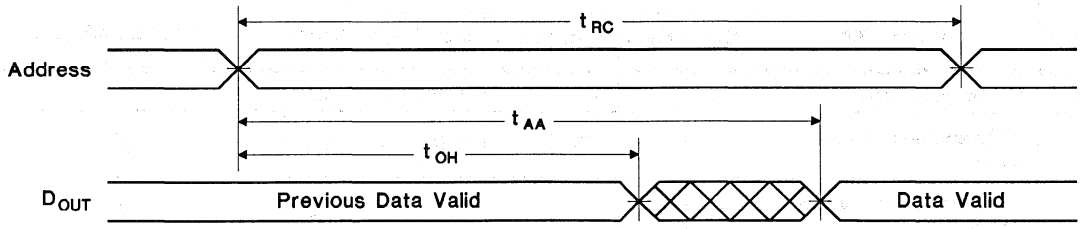


Figure 2. Output Load B

Read Cycle (T_A = TOPR, VCCmin ≤ VCC ≤ VCCmax)

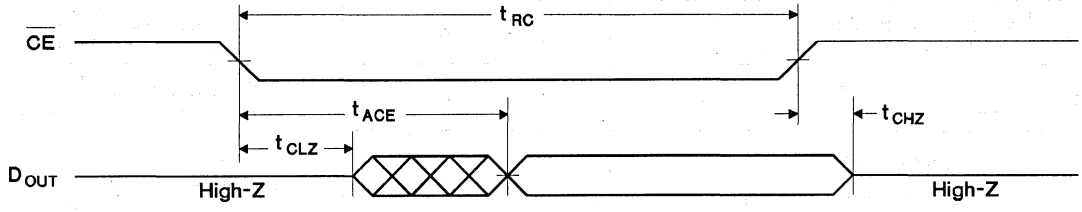
Symbol	Parameter	-70		-85		-120/-120N		Unit	Conditions
		Min.	Min.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	85	-	120	-	ns	
t_{AA}	Address access time	-	70	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



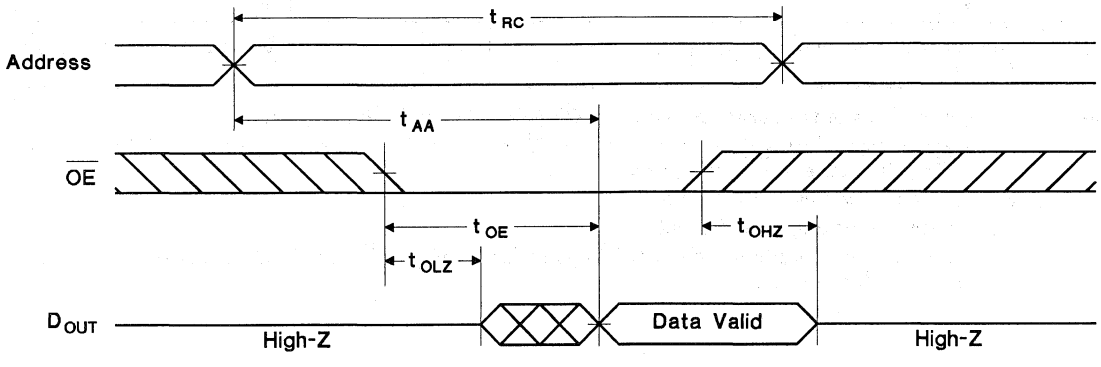
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

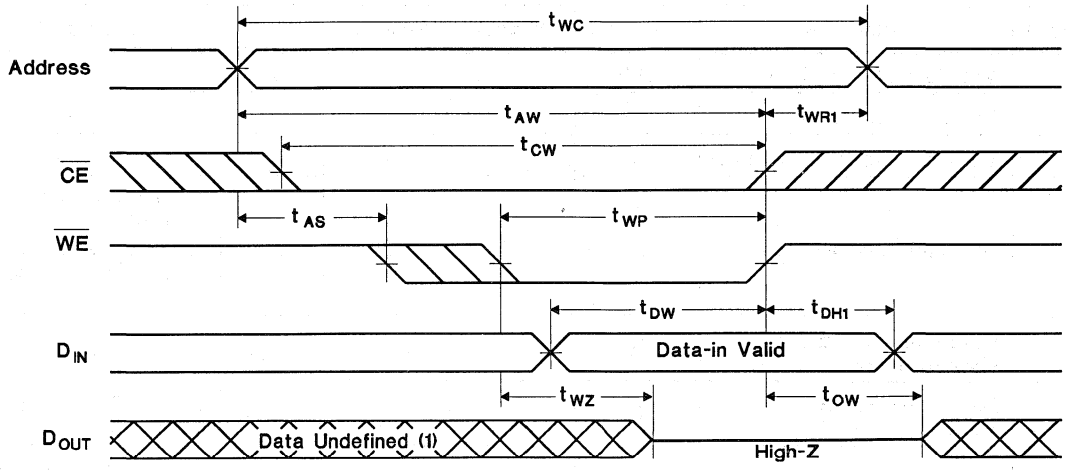
Write Cycle ($T_A = T_{OPR}$, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-70		-85		-120/-120N		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	65	-	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:

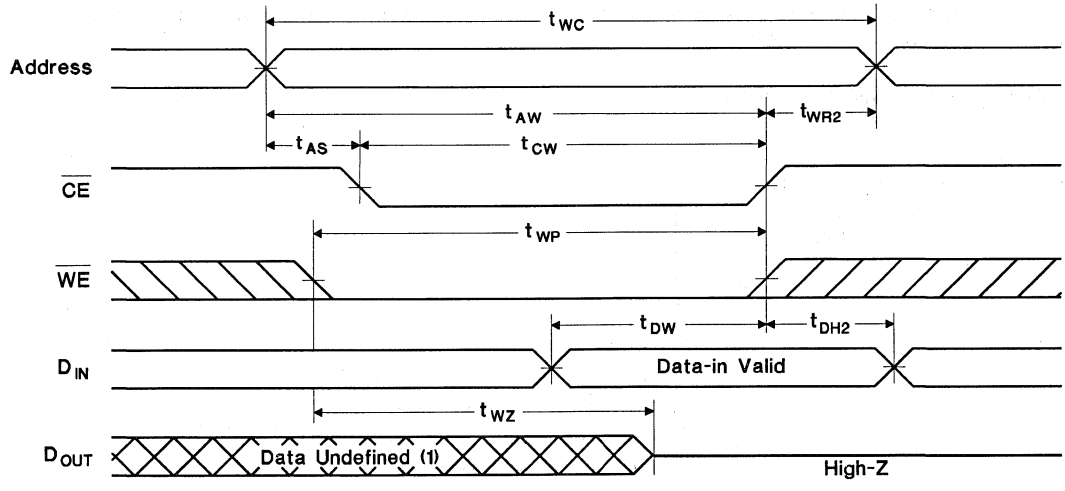
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

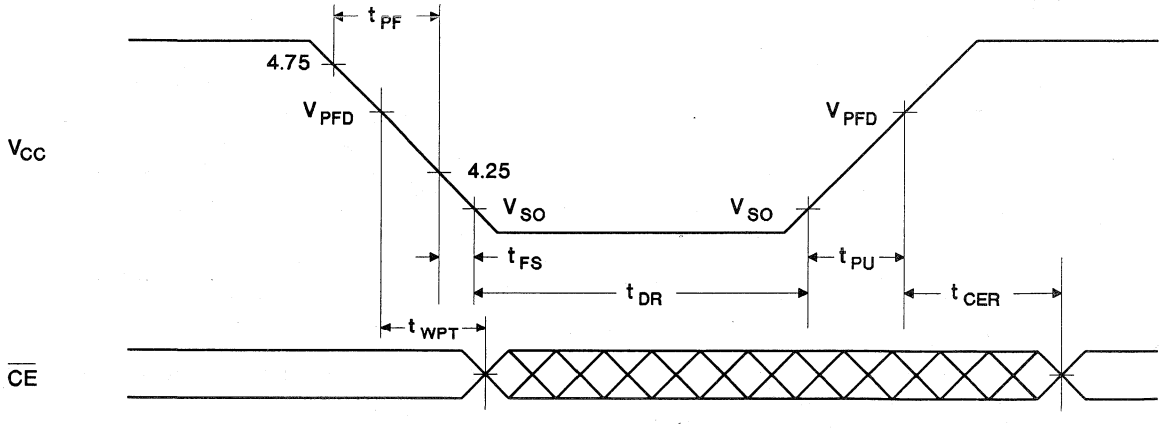
Power-Down/Power-Up Cycle ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{DR-N}	Data-retention time in absence of V_{CC}	6	-	-	years	T_A = 25°C (2); industrial temperature range only
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Battery is disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



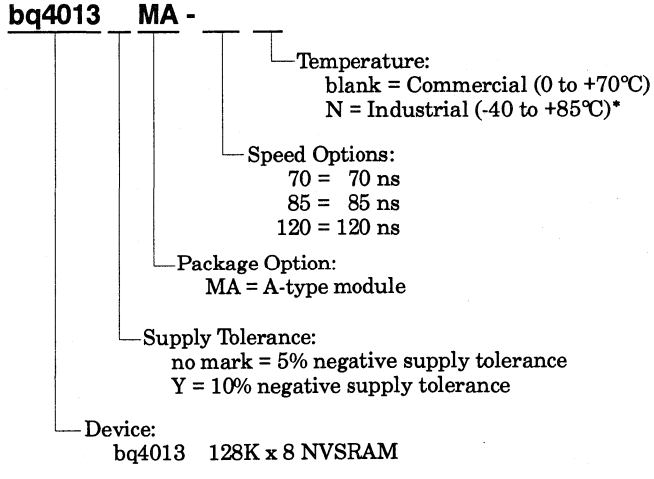
PD-B

Data Sheet Revision History

Change No.	Page No.	Description
1	5-22, 5-23, 5-24, 5-26, 5-28, 5-29	Added industrial temperature range for bq4013YMA-120N.
2	5-21, 5-24, 5-26, 5-29	Added 70 ns speed grade for bq4013-70 and bq4013Y-70.

Notes: Change 1 = Sept 1992 B changes from Sept. 1990 A.
Change 2 = Aug. 1993 C changes from Sept. 1991 B.

Ordering Information



***Note:** Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

5

bq4014/bq4014Y

256Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 256K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

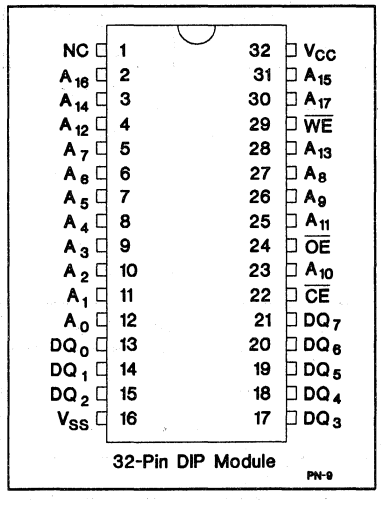
The CMOS bq4014 is a nonvolatile 2,097,152-bit static RAM organized as 262,144 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4014 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4014 requires no external circuitry and is compatible with the industry-standard 2Mb SRAM pinout.

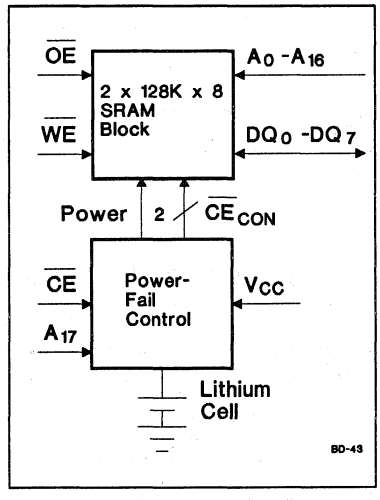
Pin Connections



Pin Names

A_0-A_{17}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4014 -85	85	-5%	bq4014Y -85	85	-10%
bq4014 -120	120	-5%	bq4014Y -120	120	-10%

Functional Description

When power is valid, the bq4014 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4014 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4014 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4014Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4014 have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4014Y
		4.75	5.0	5.5	V	bq4014
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CC}min \leq V_{CC} \leq V_{CC}max$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	5	12	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2
I_{CC}	Operating supply current	-	75	110	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mAV, A17 < V_{IL} or A17 > V_{IH}
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4014
		4.30	4.37	4.50	V	bq4014Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	40	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	40	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

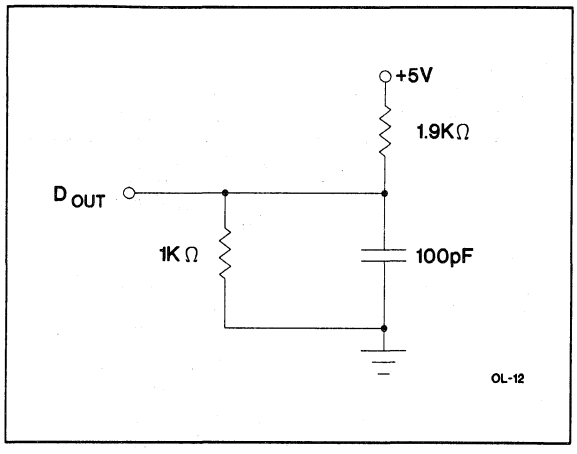


Figure 1. Output Load A

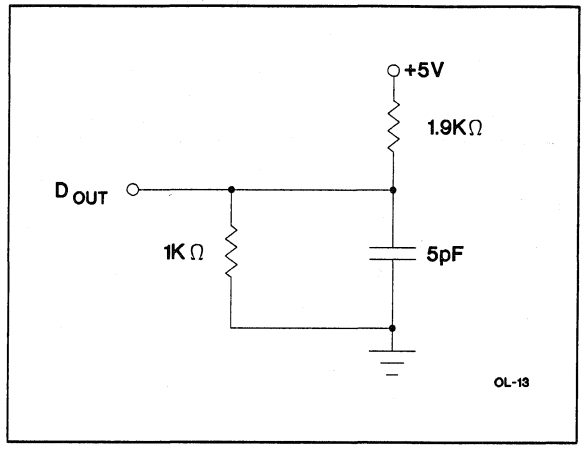
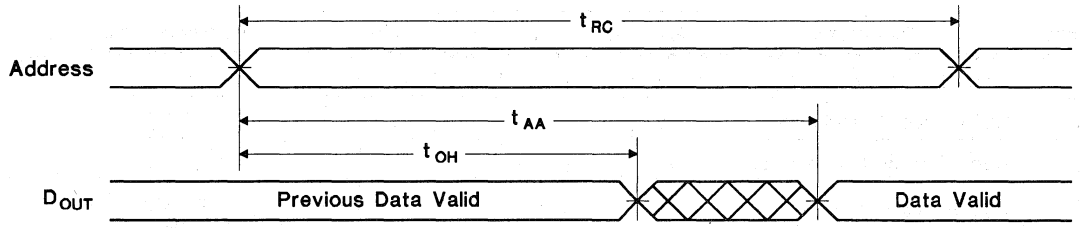


Figure 2. Output Load B

Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

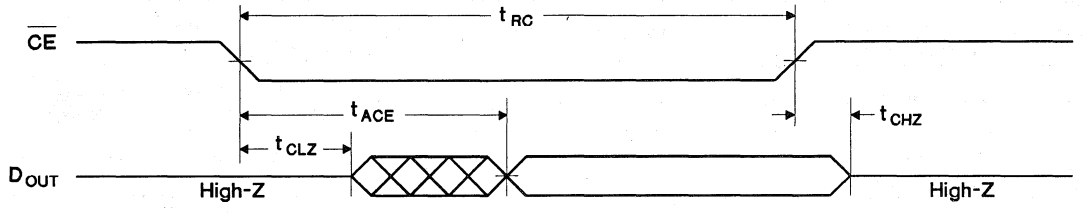
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



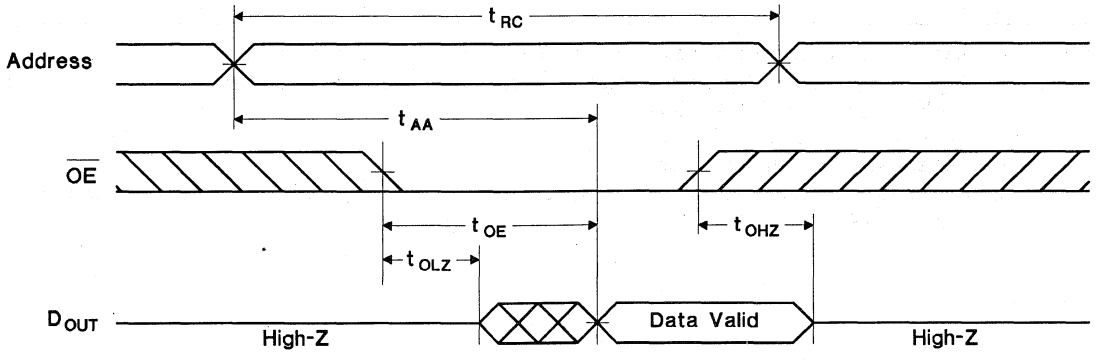
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

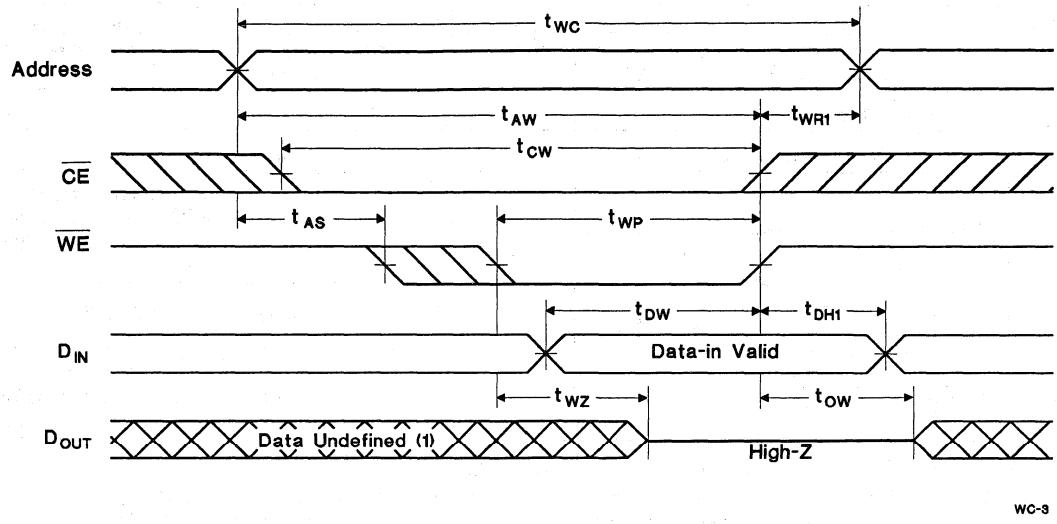
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	-85		-120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

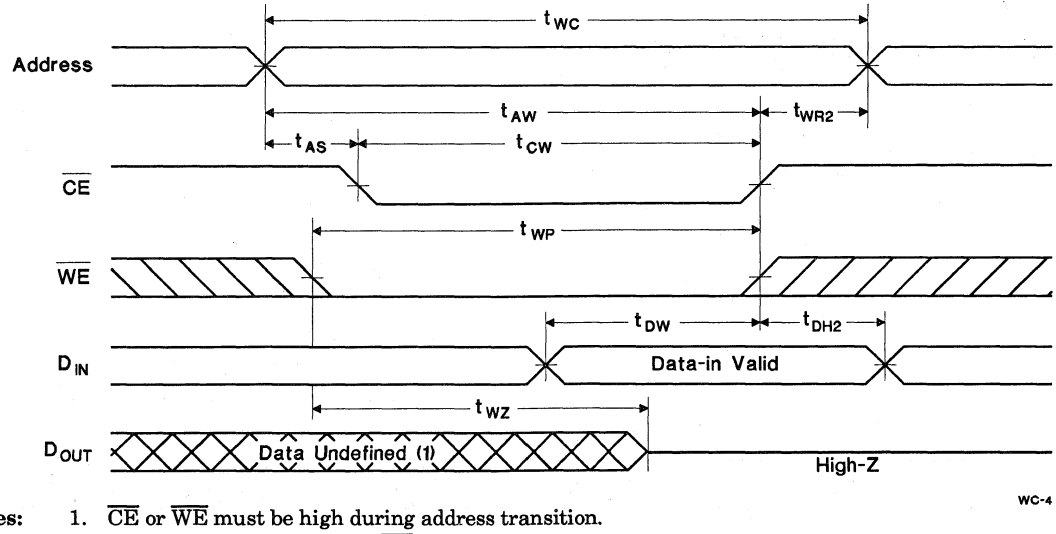
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

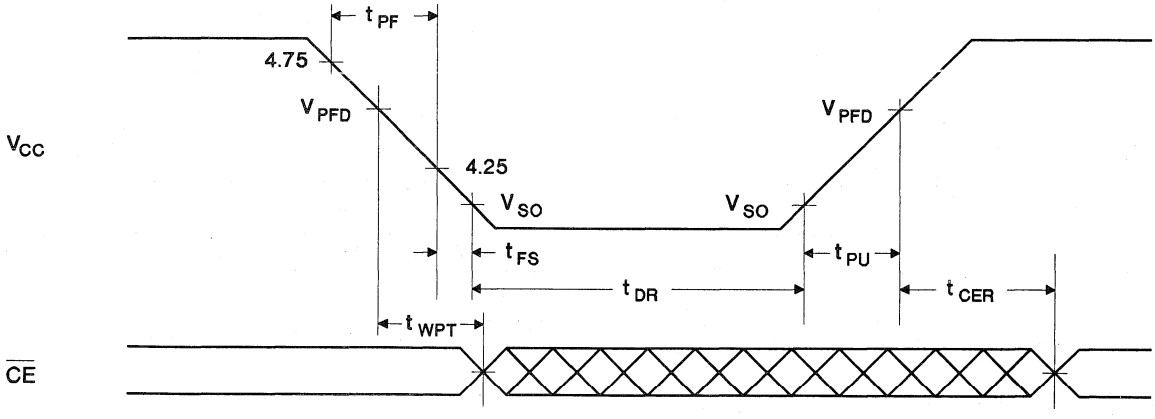
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing

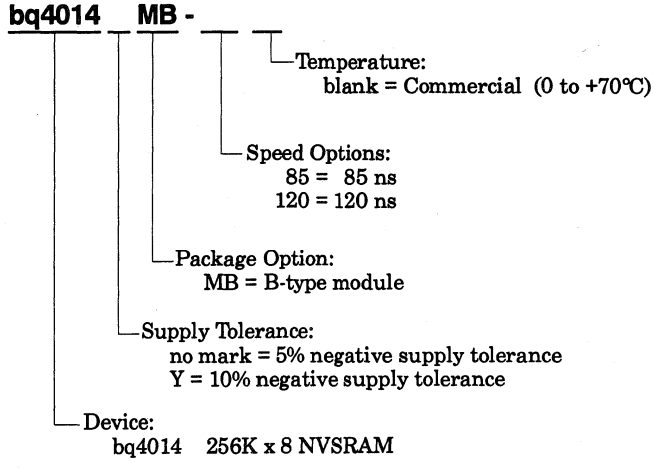


PD-B

Data Sheet Revision History (Sept. 1992 Changes From Sept. 1990)

Clarification of I_{CC} test conditions, page 5-33.

Ordering Information



5

bq4015/bq4015Y

512Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 512K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 5-year (bq4015MB) or 10-year (bq4015MA) minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4015 is a nonvolatile 4,194,304-bit static RAM organized as 524,288 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

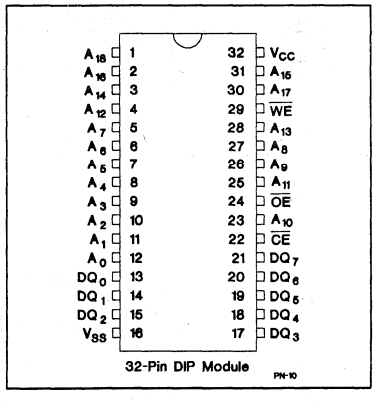
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4015 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4015 requires no external circuitry and is compatible with the industry-standard 4Mb SRAM pinout.

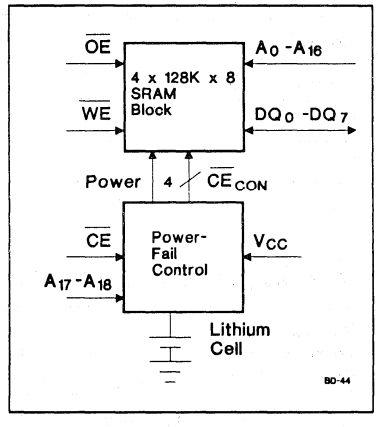
Pin Connections



Pin Names

A_0-A_{18}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



5

Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4015MA-70	70	-5%	bq4015YMA-70	70	-10%
bq4015MA-85 bq4015MB-85	85	-5%	bq4015YMA-85 bq4015YMB-85	85	-10%
bq4015MB-120	120	-5%	bq4015YMB-120	120	-10%

Functional Description

When power is valid, the bq4015 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4015 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4015 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4015Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4015 have an extremely long shelf life. The bq4015MB provides data retention for more than 5 years in the absence of system power. Because the SRAMs in the bq4015MA draw less current, the bq4015MA provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4015Y
		4.75	5.0	5.5	V	bq4015
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current (bq4015MA)	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
	Input leakage current (bq4015MB)	-	-	± 4	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current (bq4015MA)	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
	Output leakage current (bq4015MB)	-	-	± 4	µA	
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current (bq4015MA)	-	3	5	mA	$\overline{CE}$ = V_{IH}
	Standby supply current (bq4015MB)	-	7	17	mA	
I_{SB2}	Standby supply current (bq4015MA)	-	0.1	1	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2
	Standby supply current (bq4015MB)	-	2.5	5	mA	
I_{CC}	Operating supply current (bq4015MA)	-	-	90	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA, A17 < V_{IL} or A17 > V_{IH}, A18 < V_{IL} or A18 > V_{IH}
	Operating supply current (bq4015MB)	-	75	115	mA	
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4015
		4.30	4.37	4.50	V	bq4015Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

5

Capacitance (TA = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance (bq4015MA)	-	-	8	pF	Output voltage = 0V
	Input/output capacitance (bq4015MB)	-	-	40	pF	
C_{IN}	Input capacitance (bq4015MA)	-	-	10	pF	Input voltage = 0V
	Input capacitance (bq4015MB)	-	-	40	pF	

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

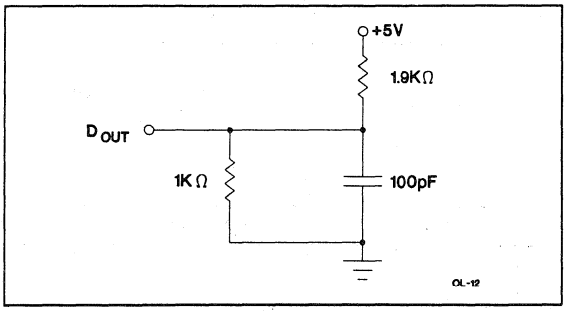


Figure 1. Output Load A

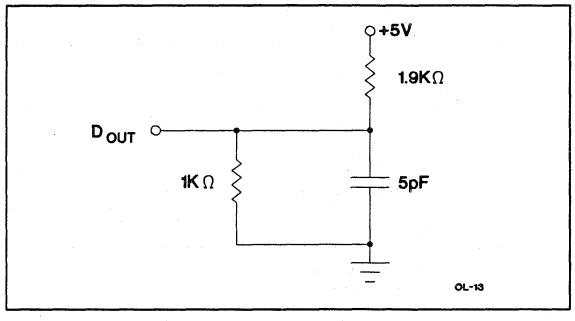
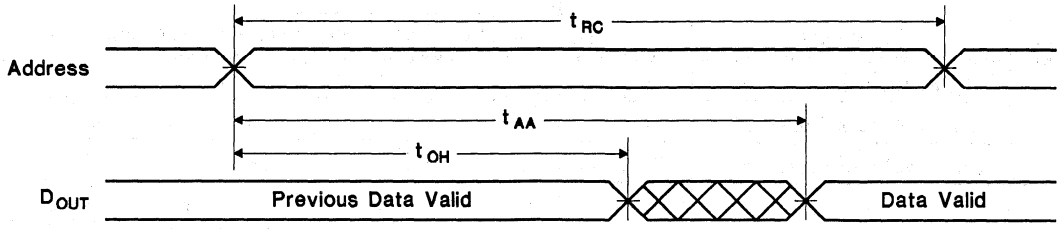


Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

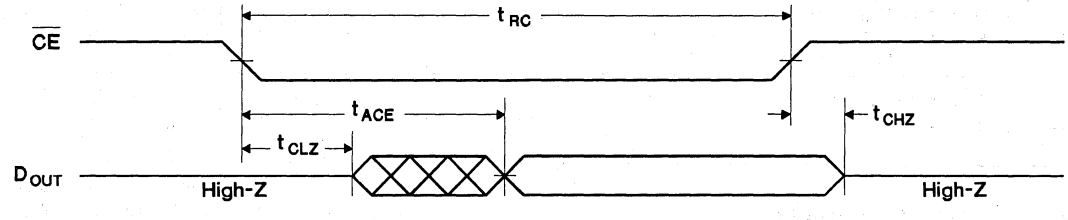
Symbol	Parameter	-70		-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	70	-	85	-	120	-	ns	
t_{AA}	Address access time	-	70	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	70	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	35	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



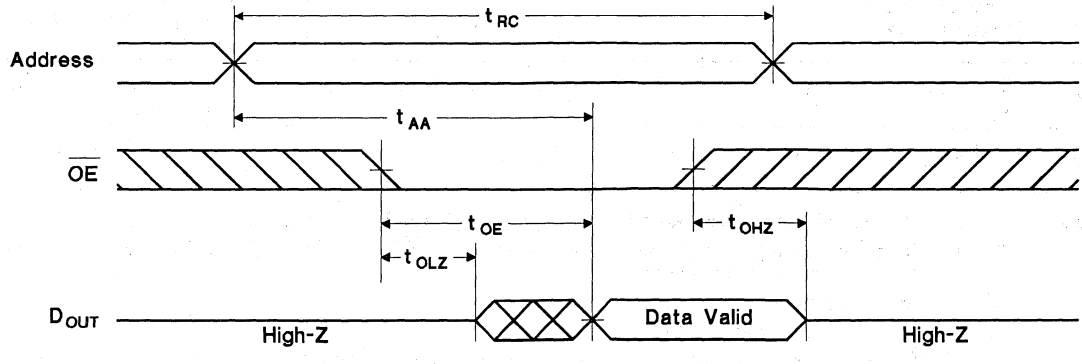
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

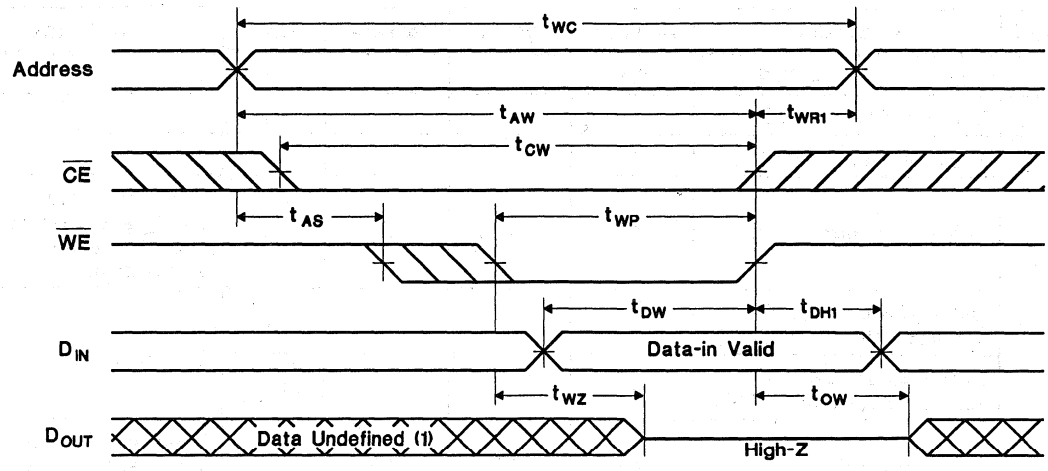
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	-70		-85		-120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	70	-	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	65	-	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:

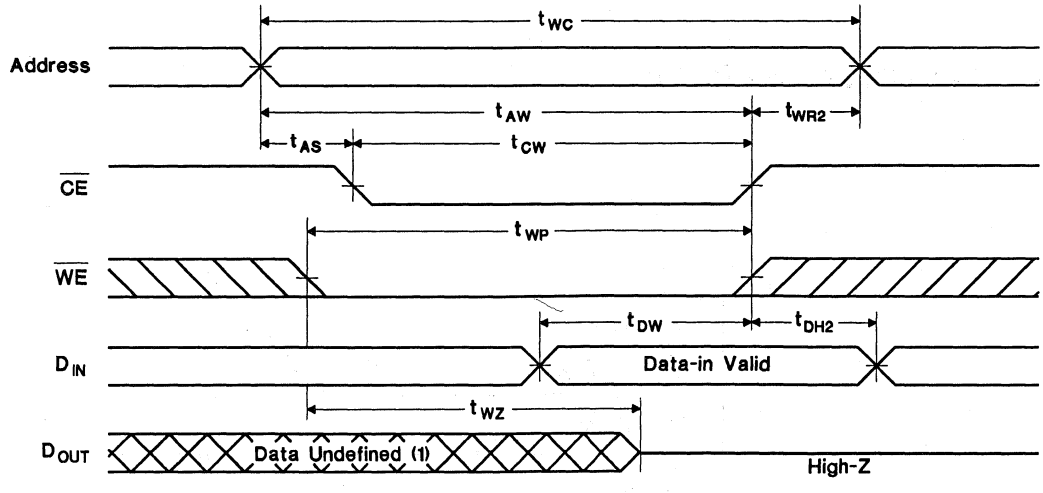
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



WC-3

Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



WC-4

Notes:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

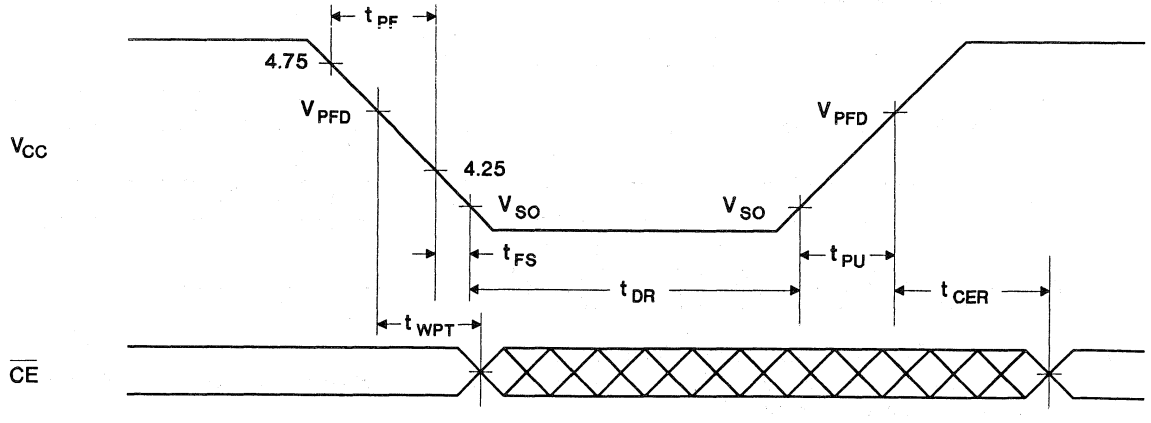
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC} (bq4015MA)	10	-	-	years	T_A = 25°C. (2)
	Data-retention time in absence of V_{CC} (bq4015MB)	5	-	-	years	
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



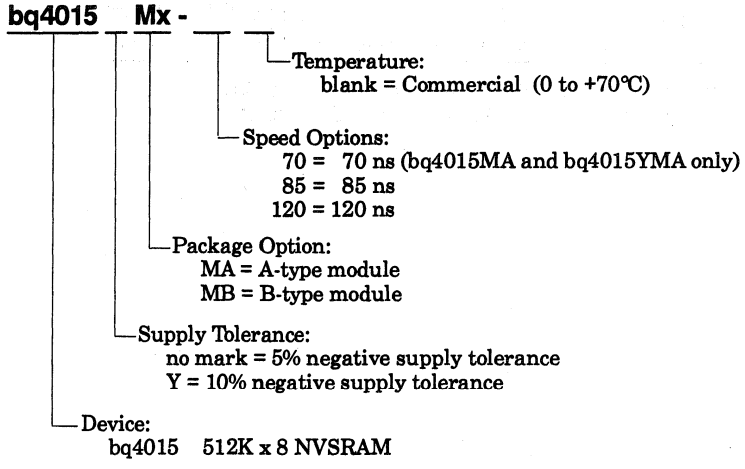
PD-B

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5-43	I_{CC} test conditions	Clarification
2	5-41, 5-42, 5-43, 5-44, 5-47, 5-48, 5-50	bq4015MA part	Addition

Note: Change 1 = Sept. 1992 B changes from Sept. 1990 A.
Change 2 = Nov. 1993 C changes from Sept. 1992 B.

Ordering Information



bq4024/bq4024Y

128Kx16 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 40-pin 128K x 16 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4024 is a nonvolatile 2,097,152-bit static RAM organized as 131,072 words by 16 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

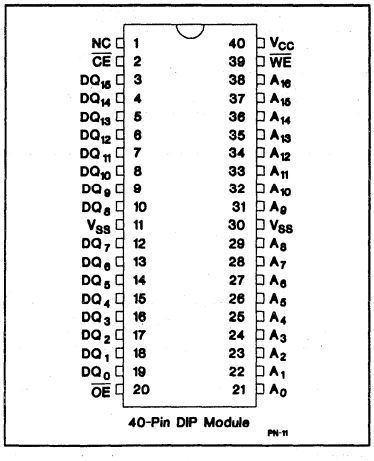
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4024 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4024 requires no external circuitry and is compatible with the industry-standard 2Mb SRAM pinout.

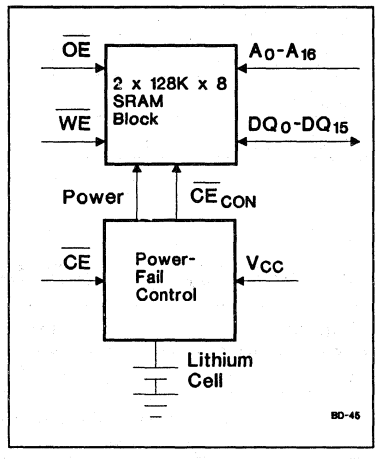
Pin Connections



Pin Names

A_0-A_{16}	Address inputs
DQ_0-DQ_{15}	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4024 -85	85	-5%	bq4024Y -85	85	-10%
bq4024 -120	120	-5%	bq4024Y -120	120	-10%

Functional Description

When power is valid, the bq4024 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4024 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4024 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4024Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4024 have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4024Y
		4.75	5.0	5.5	V	bq4024
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	5	11	mA	$\overline{CE}$ = V_{IH}
I_{SB2}	Standby supply current	-	2.5	5	mA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} - 0.2V
I_{CC}	Operating supply current	-	95	200	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4024
		4.30	4.37	4.50	V	bq4024Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, VCC = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	20	pF	Input voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

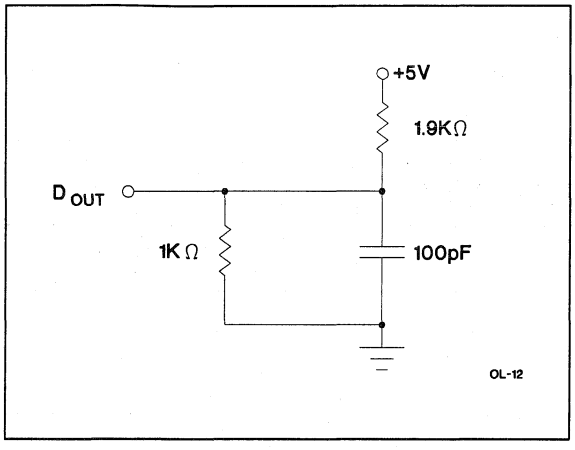


Figure 1. Output Load A

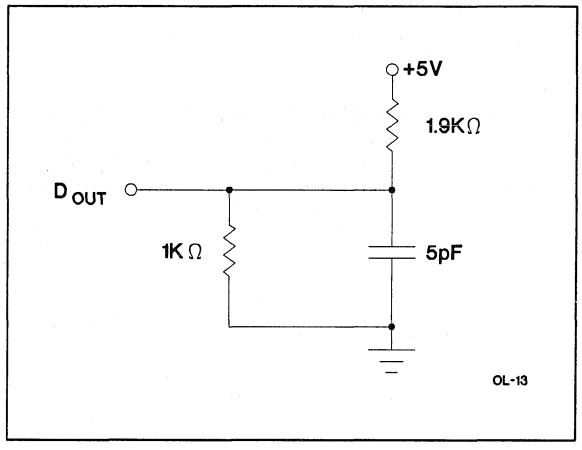
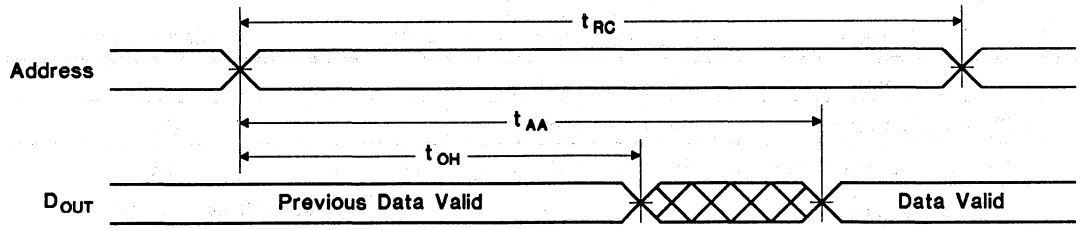


Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

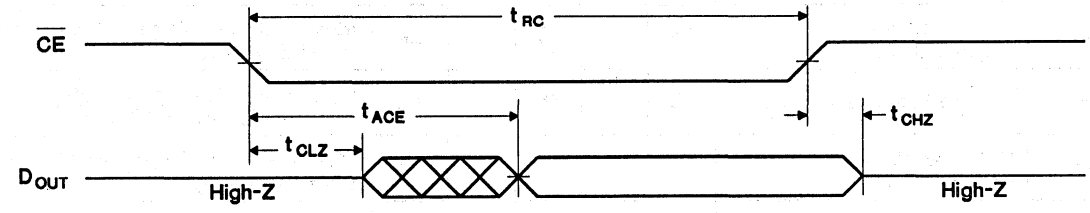
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



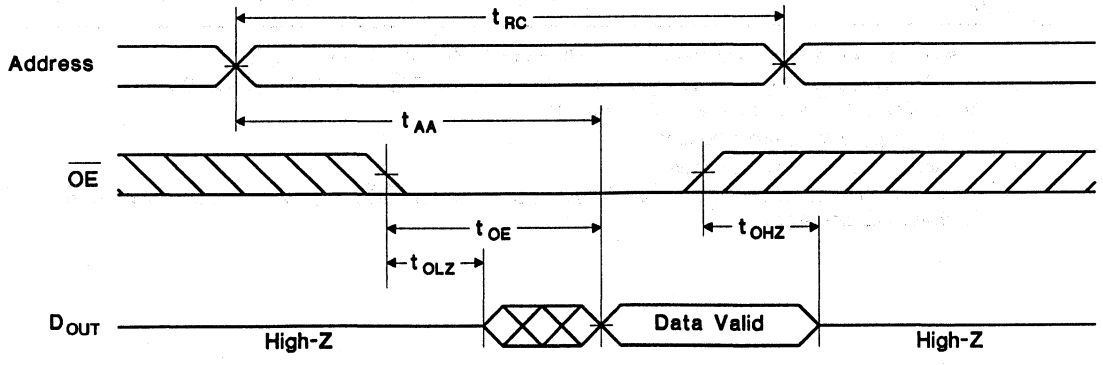
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

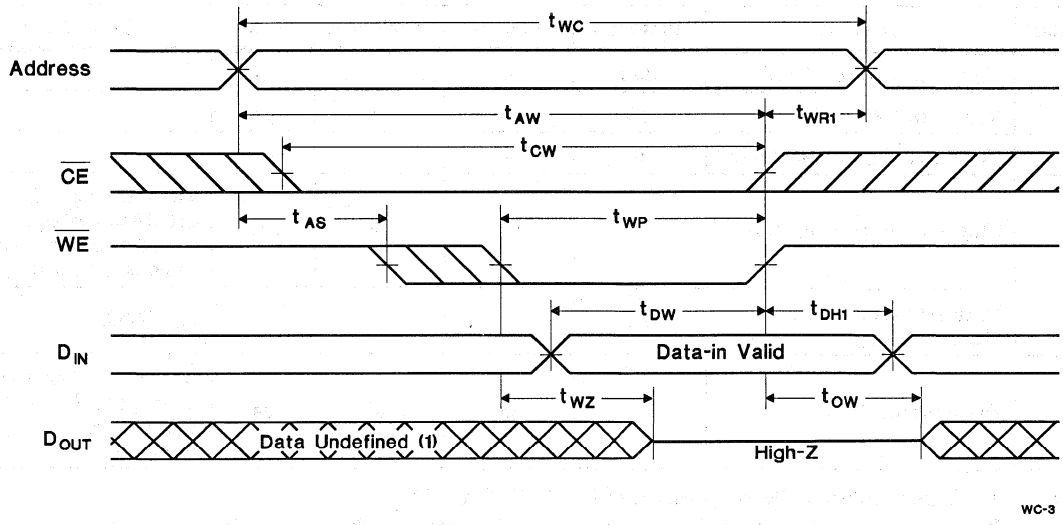
Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Device is continuously selected: $\overline{CE}$ = V_{IL}.

Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

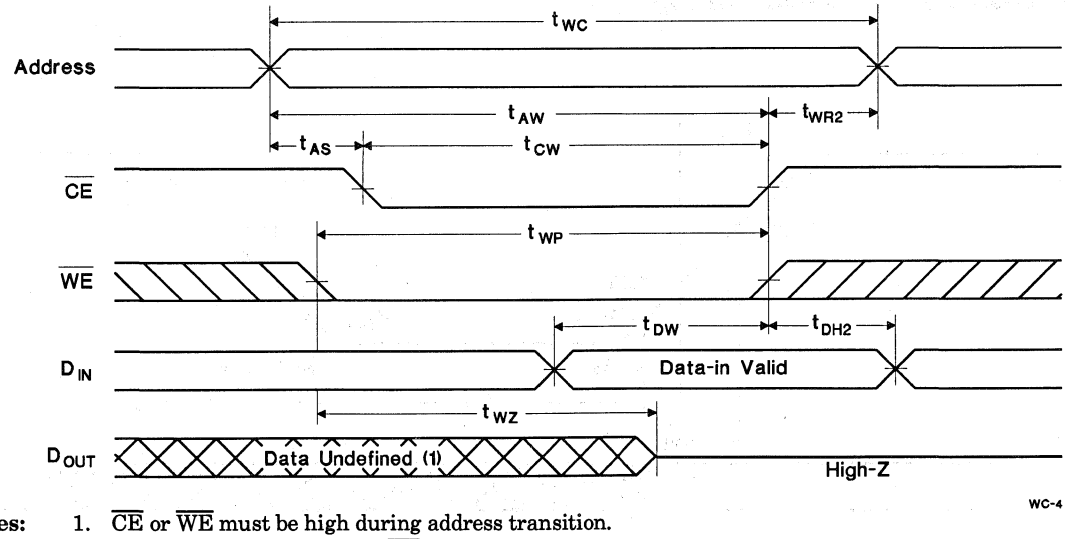
Symbol	Parameter	-85		-120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle.(4)]
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high-Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

Notes:
1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

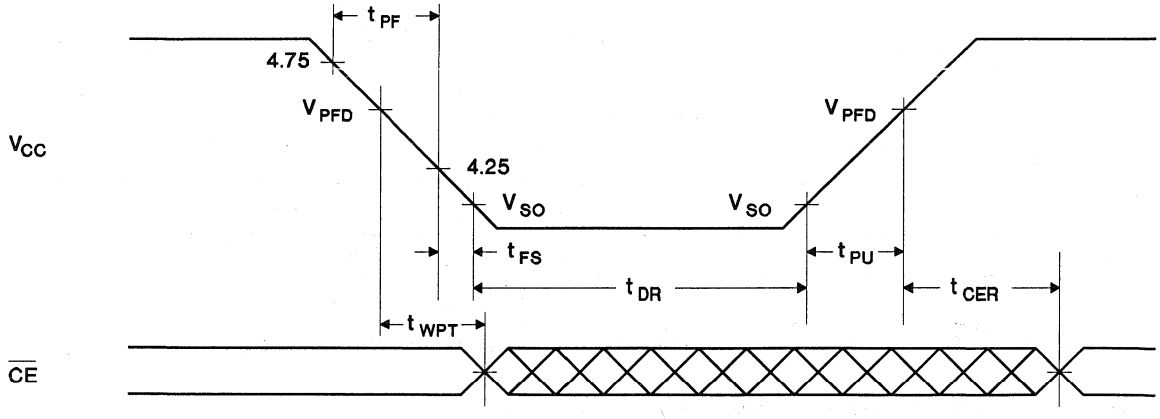
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A =25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

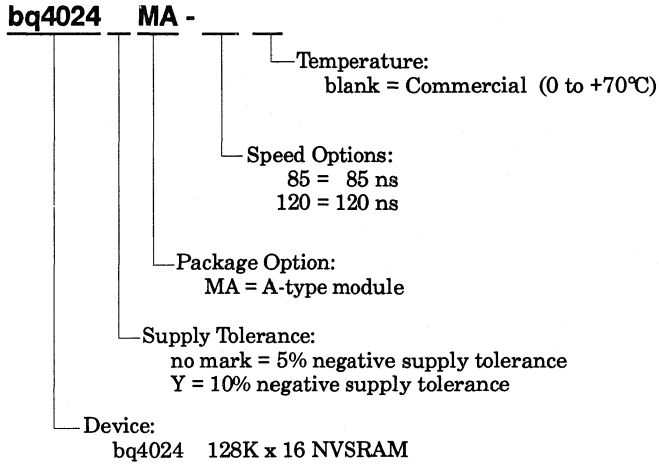
Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-B

Ordering Information



5

bq4025/bq4025Y

256Kx16 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 40-pin 256K x 16 pinout
- Conventional SRAM operation; unlimited write cycles
- 5-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4025 is a nonvolatile 4,194,304-bit static RAM organized as 262,144 words by 16 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

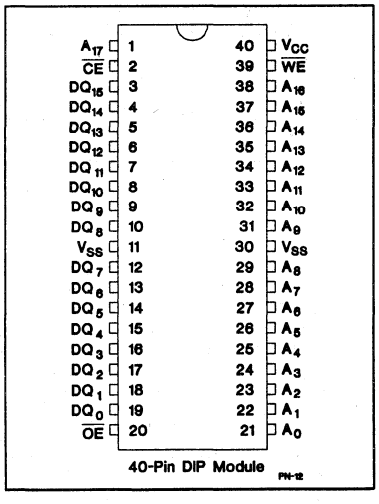
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4025 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4025 requires no external circuitry and is compatible with the industry-standard 4Mb SRAM pinout.

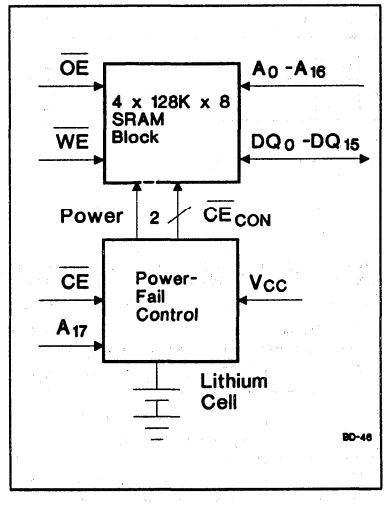
Pin Connections



Pin Names

A_0-A_{17}	Address inputs
DQ_0-DQ_{15}	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4025-85	85	-5%	bq4025Y-85	85	-10%
bq4025-120	120	-5%	bq4025Y-120	120	-10%

Functional Description

When power is valid, the bq4025 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4025 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4025 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4025Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4025 have an extremely long shelf life and provide data retention for more than 5 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4025Y
		4.75	5.0	5.5	V	bq4025
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C,

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 4	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	7	18	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$\overline{CE} \geq V_{CC}$ - 0.2V, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC}$ - 0.2V
I_{CC}	Operating supply current	-	95	200	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA, A17 < V_{IL} or A17 > V_{IH}
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4025
		4.30	4.37	4.50	V	bq4025Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	20	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	40	pF	Input voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

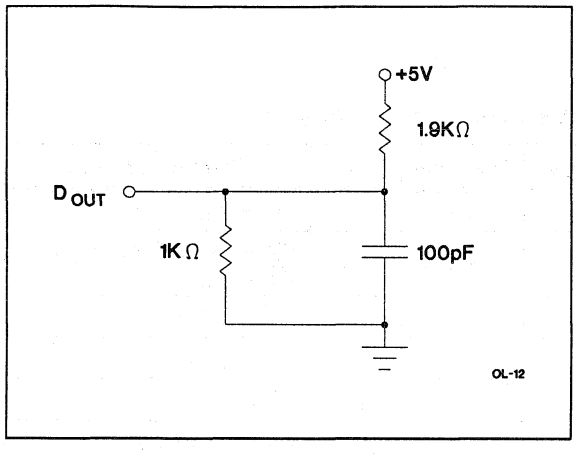


Figure 1. Output Load A

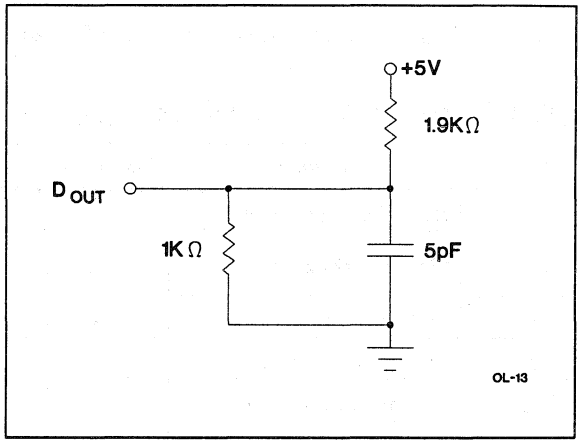
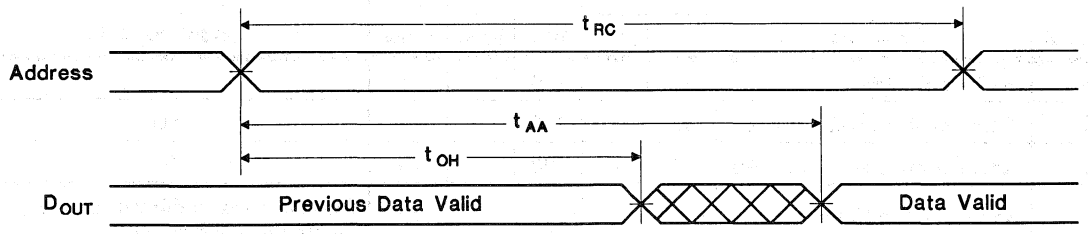


Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

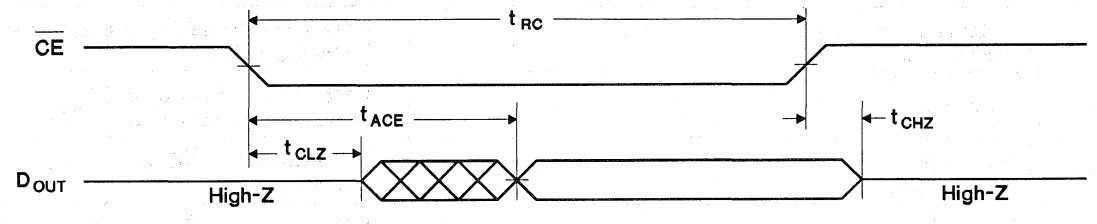
Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read cycle time	85	-	120	-	ns	
t_{AA}	Address access time	-	85	-	120	ns	Output load A
t_{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t_{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t_{OH}	Output hold from address change	10	-	10	-	ns	Output load A

Read Cycle No. 1 (Address Access) [1,2]



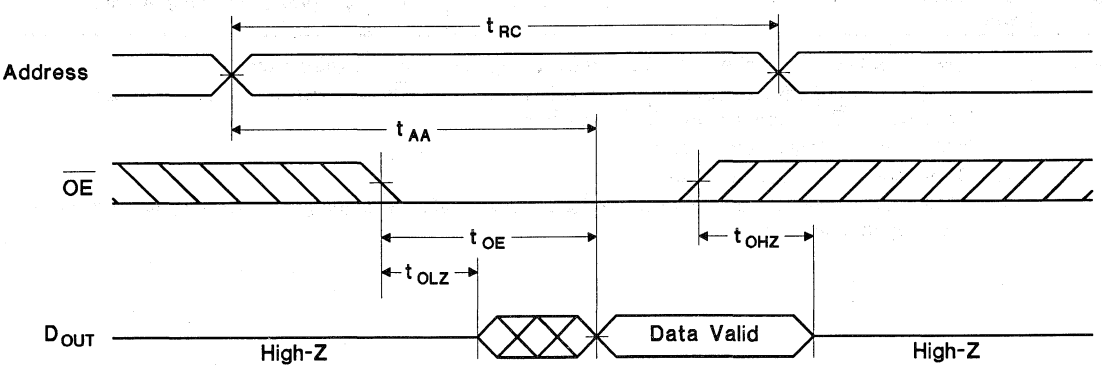
RC-1

Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



RC-2

Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



RC-3

Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

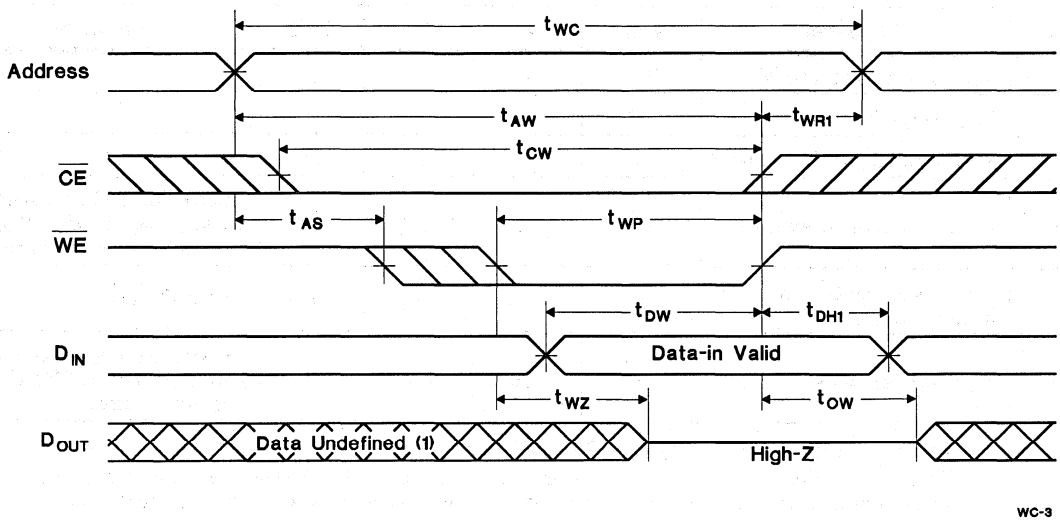
Write Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		-120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.		
t_{WC}	Write cycle time	85	-	120	-	ns	
t_{CW}	Chip enable to end of write	75	-	100	-	ns	(1)
t_{AW}	Address valid to end of write	75	-	100	-	ns	(1)
t_{AS}	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high-Z	0	30	0	40	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

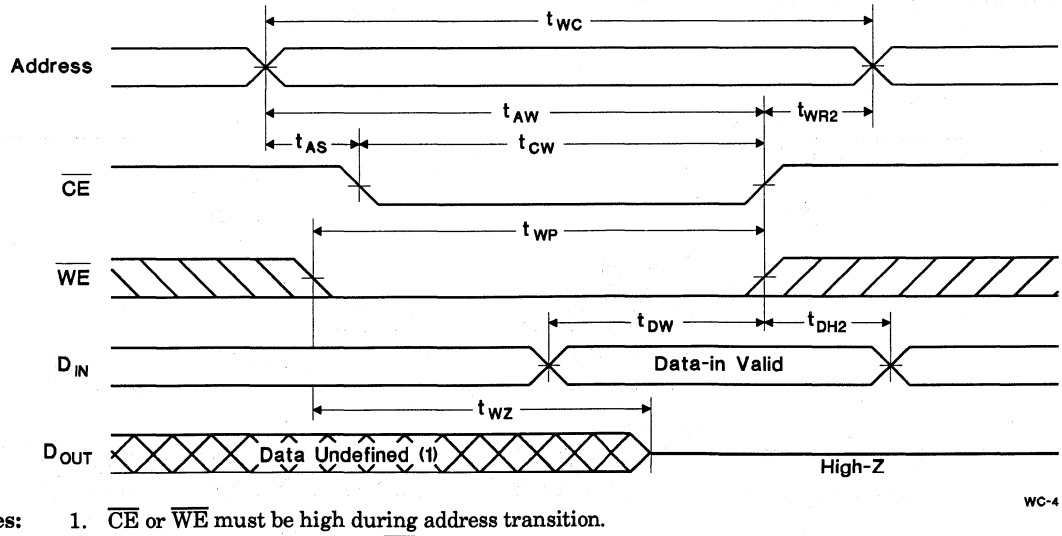
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

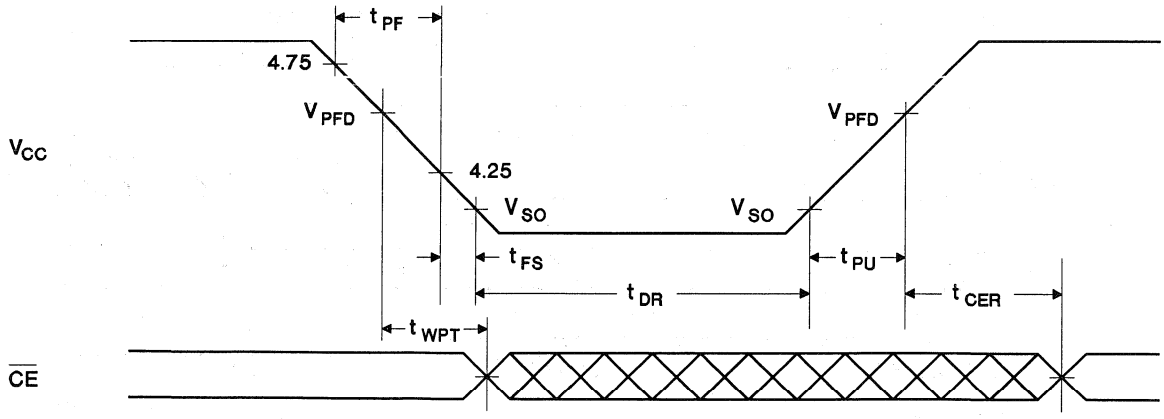
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-B

Data Sheet Revision History (Sept. 1992 Changes From Sept. 1990)

Clarification of Icc test conditions, page 5-63.

Ordering Information

bq4025 MA - _ _

- Temperature:
  blank = Commercial (0 to +70°C)
- Speed Options:
  85 = 85 ns
  120 = 120 ns
- Package Option:
  MA = A-type module
- Supply Tolerance:
  no mark = 5% negative supply tolerance
  Y = 10% negative supply tolerance
- Device:
  bq4025 256K x 16 NVSRAM

5

Notes

bq4115Y

512Kx8 NV Pseudo SRAM

Features

- Data retention in the absence of power
- Access time of 150 ns
- Automatic write-protection during power-up/power-down cycles
- Pseudo SRAM operation; unlimited read/write cycles
- Refresh handled internally
- No $\overline{CE}$ power-up cycles required
- BUSY pin indicates delayed start of read/write cycle
- Reset output for processor power-on reset
- Battery-fail warning

General Description

The CMOS bq4115Y is a nonvolatile pseudo static RAM organized as 512K words by 8 bits. The integral control circuitry and backup battery source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the PSRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the external energy source is switched on to sustain the memory until after V_{CC} returns valid. After V_{CC} returns valid, the 8 start-up cycles required by the PSRAM are handled internally during the write-protect time.

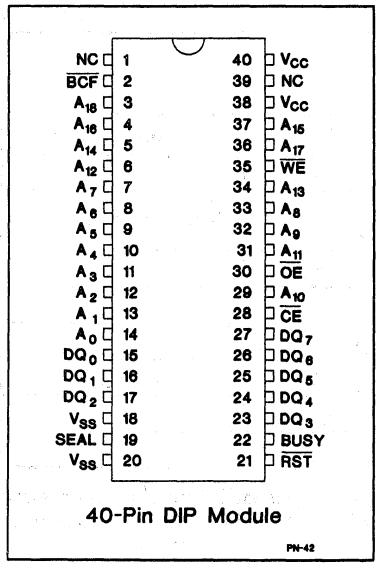
Because a $\overline{CE}$ access might be requested during an internal refresh interval, a BUSY pin is provided to indicate that the PSRAM is in a refresh cycle and the output data will be delayed.

The bq4115Y uses a low-standby-current PSRAM, coupled with two small batteries to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM and flash. The internal rechargeable lithium battery can maintain data for about 2 weeks. After that time, the internal backup is switched to a lithium nonrechargeable cell that can maintain data for 7 additional months. The rechargeable battery begins charging when V_{CC} becomes valid.

If the duration of the power loss is less than 2 weeks, the bq4115Y can operate as a nonvolatile memory for greater than 10 years.

5

Pin Connections



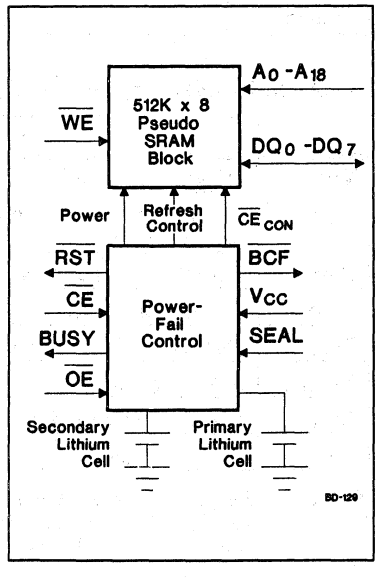
40-Pin DIP Module

PN-42

Pin Names

A_0-A_{18}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{BCF}$	Battery fail output
SEAL	Battery isolation signal input
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
$\overline{RST}$	Reset output
BUSY	Read/write cycle delay indicator open-drain output
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Functional Description

When power is valid, the bq4115Y operates as a standard CMOS PSRAM. During power-down and power-up cycles, the bq4115Y acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4115Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the bq4115Y automatically write-protects the data. All inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal rechargeable lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The bq4115Y provides a power-on reset that goes active at a time t_R after V_{CC} reaches V_{PFD} on power-down and remains active for t_{RR} after V_{CC} reaches V_{PFD} on power-up. It is recommended that the $\overline{RST}$ pin be used as the reset for the micro to avoid the possibility of bus contention during this time period.

As shipped from Benchmarq, the internal batteries are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs. The bq4115Y can be resealed by asserting the SEAL pin during valid V_{CC}. This causes the internal batteries to be disconnected from V_{OUT} after V_{CC} falls below V_{PFD}. Sealing a part is useful after testing, before the part is used.

Function Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0–A_{18}	DQ_0–DQ_7	Notes
Read	L	L	H	See note	Out	At $\overline{CE}$ falling edge, A_0–A_{18} are "in"; otherwise, A_0–A_{18} are "don't care."
Write	L	X	L	See note	In	At $\overline{CE}$ falling edge, A_0–A_{18} are "in"; otherwise, A_0–A_{18} are "don't care."
Standby	H	L	X	X	High Z	

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +55	°C	
T_{STG}	Storage temperature	0 to +55	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds
I_{OUT}	Short-circuit output current	300	mA	
P_D	Power dissipation	600	mW	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 10	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -15 mA
V_{OL}	Output low voltage	-	-	0.55	V	I_{OL} = 64 mA
I_{SB1}	Standby supply current	-	6	10	mA	$\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ 0V, $\overline{OE}$ = V_{IH}
I_{SB2}	Standby supply current	-	20	200	µA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN}, $\overline{OE}$ ≥ V_{CC} - 0.2
I_{CC}	Operating supply current	-	50	65	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
Output levels are for I/O pins.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

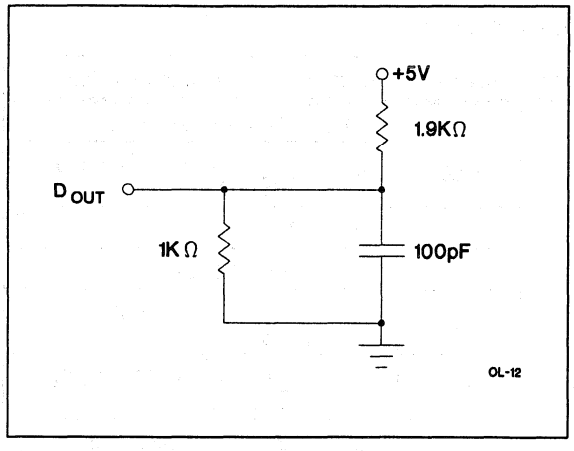


Figure 1. Output Load A

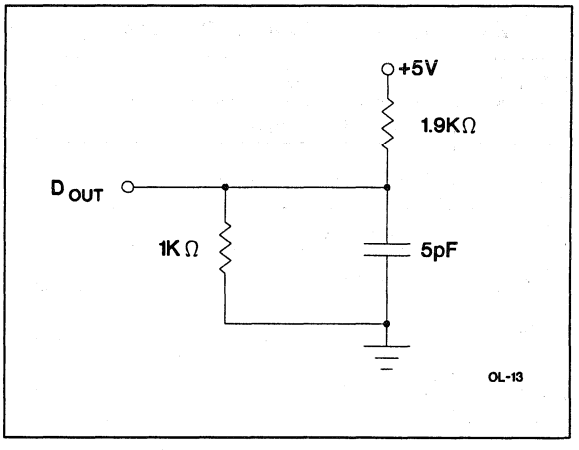


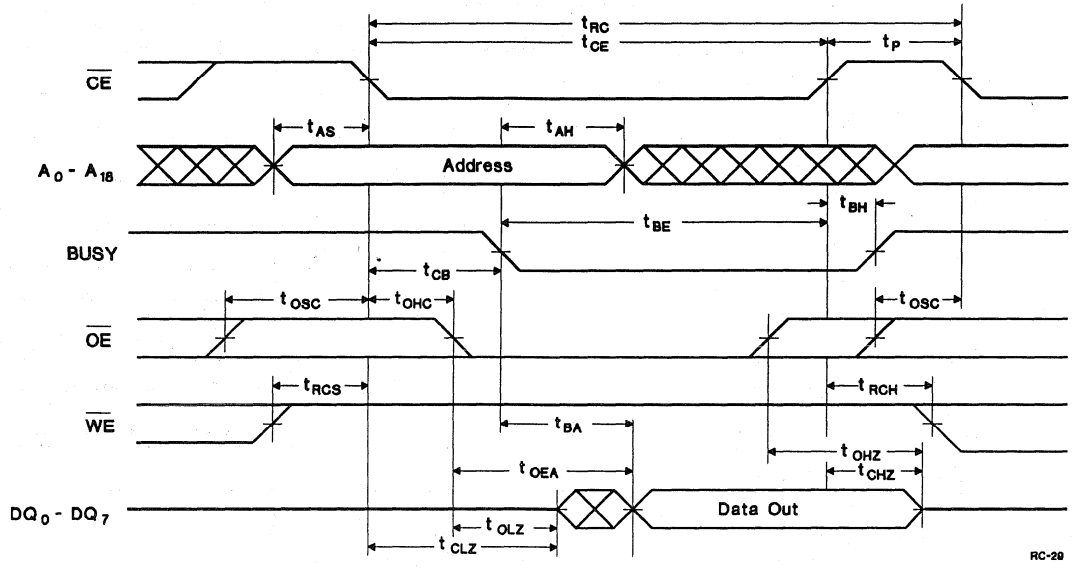
Figure 2. Output Load B

Read Cycle (T_A = 0 to 55°C, V_{CC} = 5V ±10%)

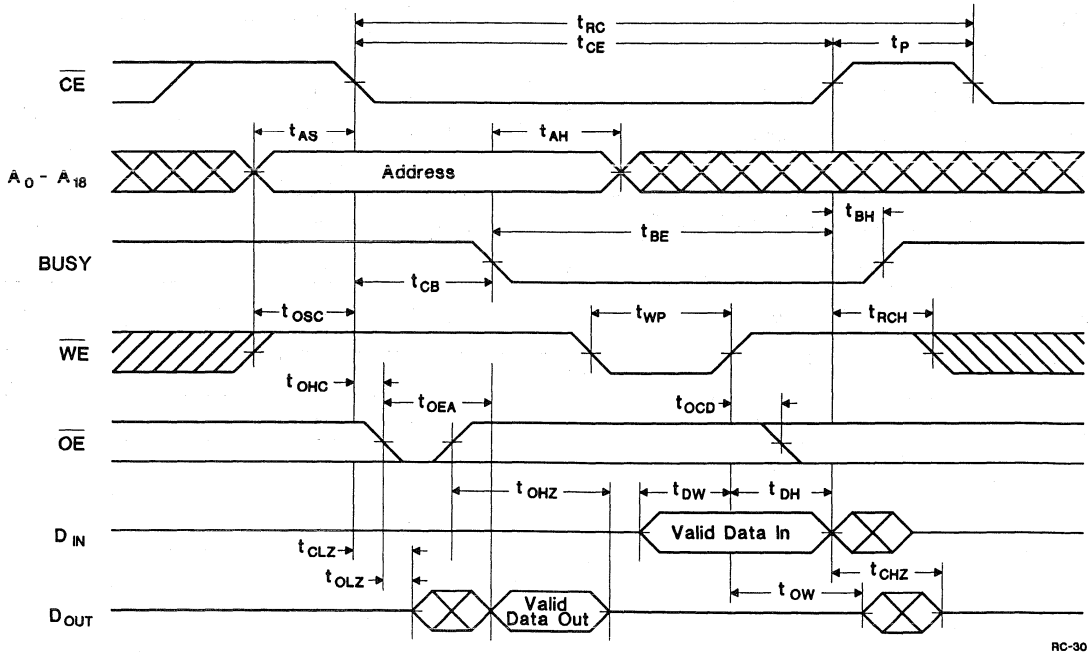
Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{RC}	Random read,write cycle time	230	-	-	ns	
t_{RMW}	Read modify write cycle time	290	-	-	ns	
t_{CE}	Chip enable pulse width	150	-	5,000	ns	
t_P	Chip enable precharge time	80	-	-	ns	
t_{CB}	$\overline{CE}$ low to BUSY low	-	7	10	ns	
	$\overline{CE}$ low to BUSY low during refresh	-	-	400	ns	t_{CB} has a <6% probability of being longer than 150ns due to an internal refresh cycle
t_{OEA}	Output enable access time	-	-	90	ns	When not in refresh mode
t_{CLZ}	Chip enable to output in low Z	30	-	-	ns	When not in refresh mode
t_{OLZ}	Output enable to output in low Z	10	-	-	ns	
t_{BE}	BUSY low to $\overline{CE}$ high	150	-	5,000	ns	
t_{BA}	Access time from BUSY	-	-	150	ns	
t_{CHZ}	Chip disable to output in high Z	-	-	45	ns	
t_{OHZ}	Output disable to output in high Z	-	-	45	ns	
t_{OSC}	$\overline{OE}$ setup time referenced to $\overline{CE}$	0	-	-	ns	
t_{OHC}	$\overline{OE}$ hold time referenced to $\overline{CE}$	0	-	-	ns	
t_{RCS}	Read command setup time	0	-	-	ns	
t_{RCH}	Read command hold time	10	-	-	ns	
t_{AS}	Address setup time, referenced to $\overline{CE}$	0	-	-	ns	
t_{AH}	Address hold time, referenced to BUSY	30	-	-	ns	
t_{BH}	BUSY hold time from $\overline{CE}$ high to BUSY high	-	-	10	ns	
t_{OW}	Output active from end of write	5	-	-	ns	
t_T	Transition time (rise and fall)	3	-	50	ns	

5

Read Cycle



Read Modify Write Cycle



Write Cycle (T_A = 0 to 55°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{RC}	Random read,write cycle time	230	-	-	ns	
t_{CE}	Chip enable pulse width	150	-	5,000	ns	
t_P	Chip enable precharge time	80	-	-	ns	
t_{CB}	$\overline{CE}$ low to BUSY	-	7	10	ns	
	$\overline{CE}$ low to BUSY low during refresh	-	-	400	ns	t_{CB} has a <6% probability of being longer than 150ns due to an internal refresh cycle
t_{CLZ}	Chip enable to output in low Z	30	-	-	ns	When not in refresh mode
t_{OLZ}	Output enable to output in low Z	10	-	-	ns	
t_{BE}	BUSY to $\overline{CE}$ high	150	-	5,000	ns	
t_{OHZ}	Output disable to output in high Z	-	-	45	ns	
t_{WHZ}	Write enable to output in high Z	-	-	30	ns	
t_{WP}	Write pulse width	35	-	-	ns	
t_{CW}	Chip enable to end of write	150	-	-	ns	
t_{DW}	Data setup time from end of write	30	-	-	ns	
t_{DWH}	Data hold time from end of write	0	-	-	ns	
t_{AS}	Address setup time, referenced to $\overline{CE}$	0	-	-	ns	
t_{AH}	Address hold time, referenced to BUSY	30	-	-	ns	
t_{BH}	BUSY hold time from $\overline{CE}$	0	-	10	ns	
t_{OCD}	Chip enable to output enable delay	0	-	-	ns	
t_{OW}	Output active from end of write	5	-	-	ns	
t_T	Transition time (rise and fall)	3	-	50	ns	

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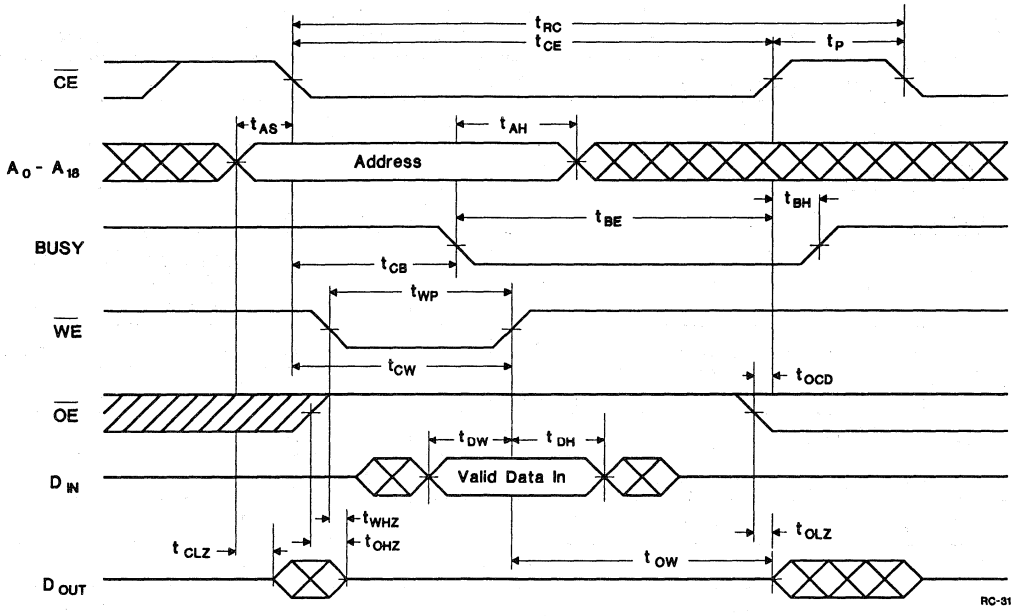
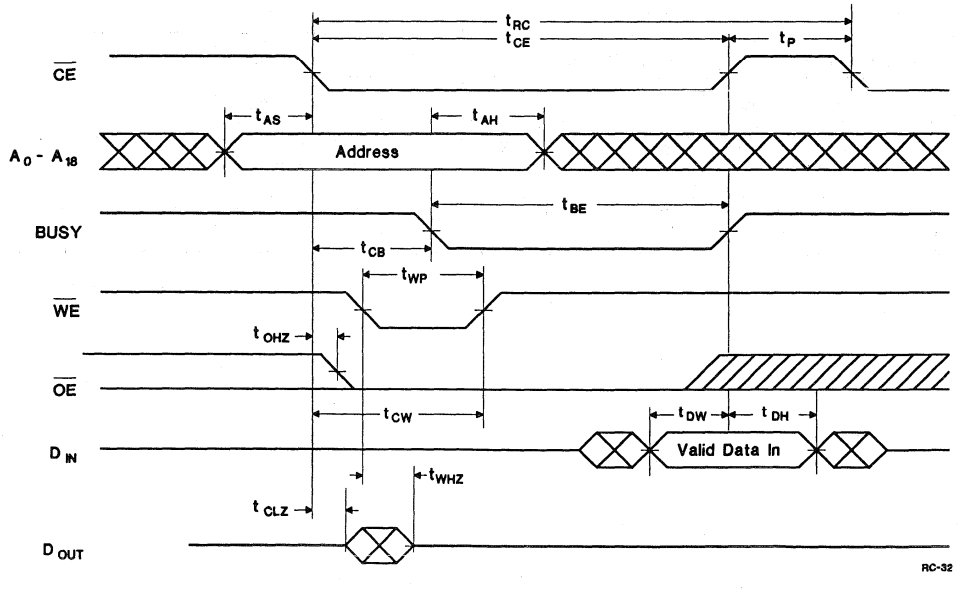
Write Cycle No. 1 ($\overline{OE}$ High)



Write Cycle No. 2 ($\overline{OE}$ Low)



Power-Down/Power-Up Cycle (T_A = 0 to 55°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	300	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	300	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which PSRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	7	-	-	months	For non-rechargeable; T_A = 25°C. (2)
		2	-	-	weeks	For rechargeable; T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	20	40	80	ms	

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

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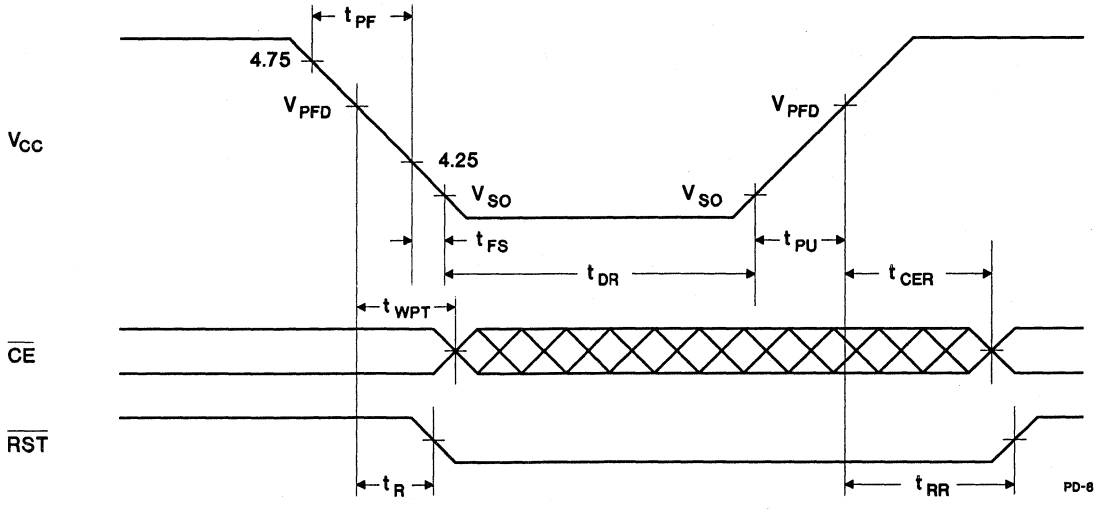
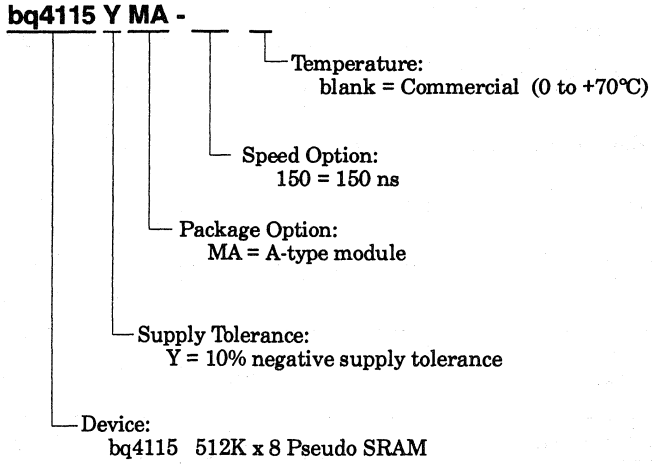
Power-Down/Power-Up Timing



Ordering Information



Package Drawings

Benchmarq's standard packages are described in the following tables.

Package Type	Description	No. Pins	Device
MA	DIP Module, A-Type	12	bq2502
		28	bq4010/bq4010Y bq4011Y/bq4011Y bq4830Y
		32	bq4013/bq4013Y bq4015/bq4015Y bq4832Y bq4842Y
		40	bq4024/bq4024Y bq4025/bq4025Y bq4115Y
MB	DIP Module, B-Type	32	bq4014/bq4014Y bq4015/bq4015Y
MT	DIP Module, T-Type	24	bq3287/bq3287A bq3287E/bq3287EA bq4287
P	Plastic DIP, 0.600"	24	bq3285 bq3285E bq3285L bq4285 bq4285E bq4285L
		28	bq4845/Y
PN	Plastic DIP, 0.300"	8	bq2002 bq2201 bq2053 bq2900
		14	bq2901
		16	bq2003 bq2004 bq2010 bq2011 bq2012 bq2014 bq2031 bq2040 bq2050 bq2054 bq2202 bq2203A bq2204A bq2212
		20	bq2005
		24	bq2001 bq2007

Package Type	Description	No. Pins	Device
Q	Quad PLCC	28	bq3285 bq3285E bq4285 bq4285E
S	SOIC, 0.300"	16	bq2003
		20	bq2005
		24	bq2001 bq2007 bq3285 bq3285E bq3285L bq4285 bq4285E bq4285L
		28	bq4845/Y
SN	SOIC Narrow, 0.150"	8	bq2002 bq2201 bq2053 bq2900
		14	bq2901
		16	bq2004 bq2010 bq2011 bq2012 bq2014 bq2031 bq2040 bq2050 bq2054 bq2202 bq2203A bq2204A bq2212
SS*	SSOP, 0.150"	24	bq2007 bq3285E bq3285L bq4285E bq4285L

* Contact factory for availability.

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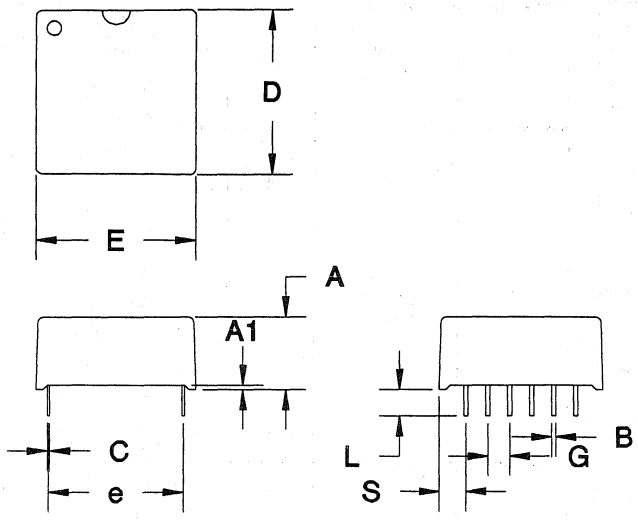
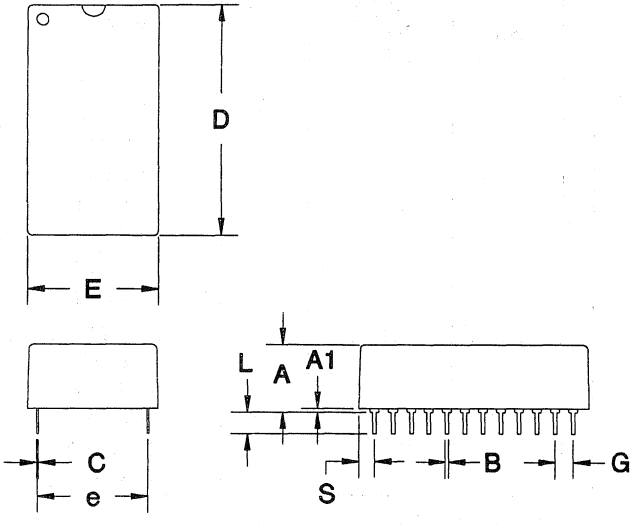
MA: 12-Pin A-Type Module



12-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	8.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	0.710	0.740	18.03	18.80
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.105	0.130	2.67	3.30

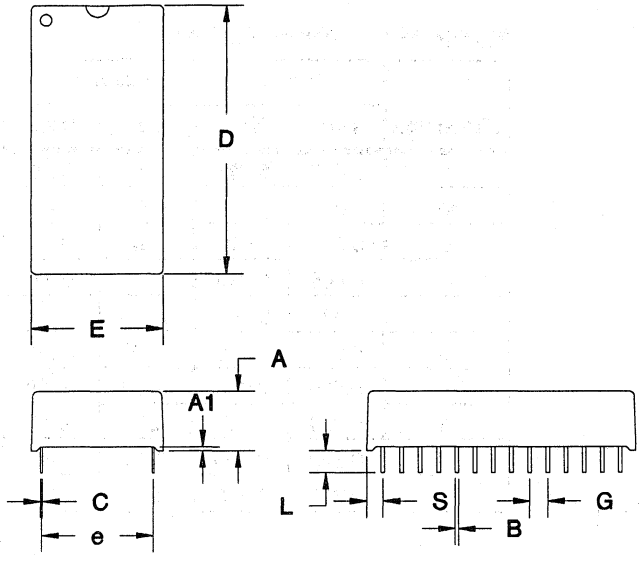
MT: 24-Pin T-Type Module



24-Pin MT (T-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.360	0.390	9.14	9.91
A1	0.015	-	0.38	-
B	0.015	0.022	0.38	0.56
C	0.008	0.013	0.20	0.33
D	1.320	1.335	33.53	33.91
E	0.710	0.740	18.03	18.80
e	0.590	0.620	14.99	15.75
G	0.090	0.110	2.29	2.79
L	0.110	0.130	2.79	3.30
S	0.100	0.120	2.54	3.05

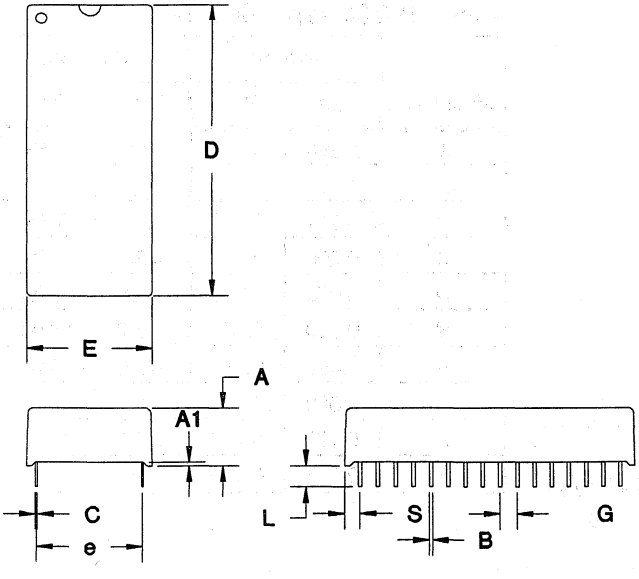
MA: 28-Pin A-Type Module



28-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.470	1.500	37.34	38.10
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

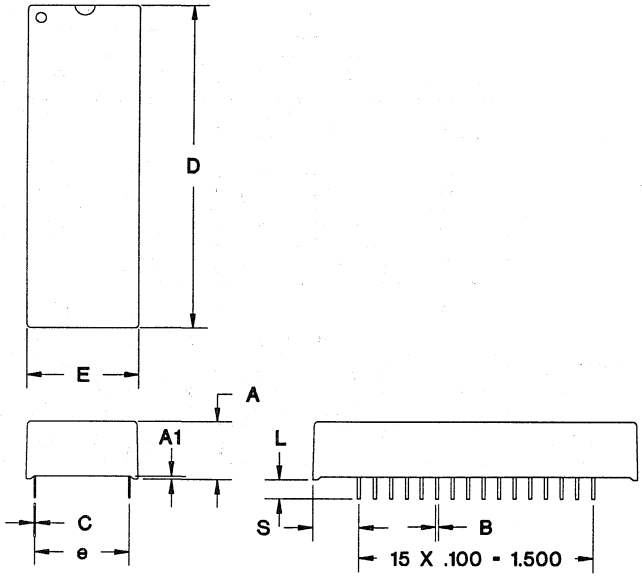
MA: 32-Pin A-Type Module



32-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.670	1.700	42.42	43.18
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

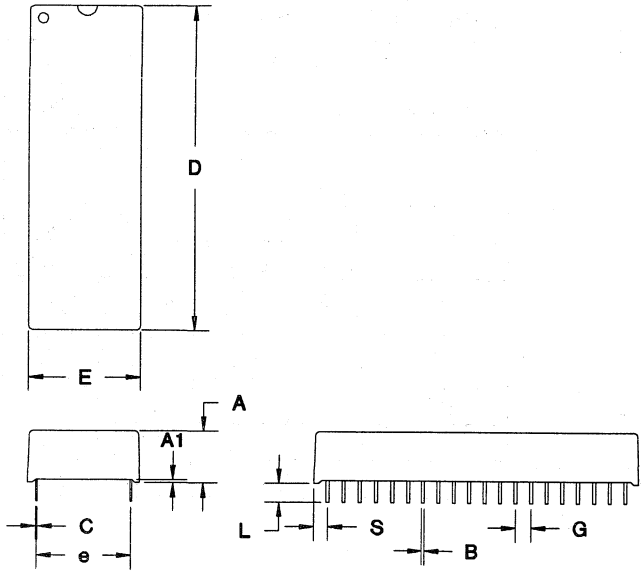
MB: 32-Pin B-Type Module



32-Pin MB (B-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.275	0.310	6.99	7.87

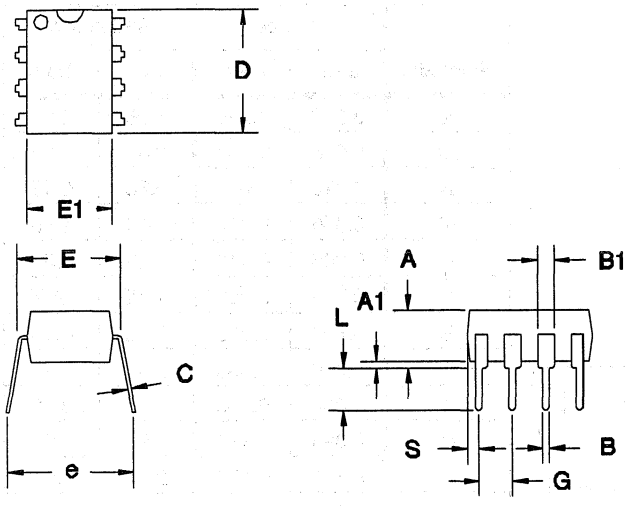
MA: 40-Pin A-Type Module



40-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

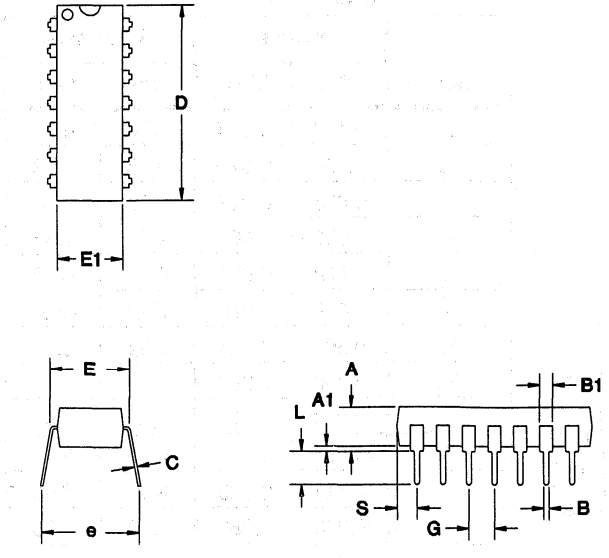
PN: 8-Pin DIP (0.300")



8-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.350	0.380	8.89	9.65
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

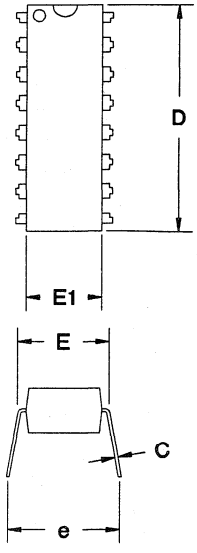
PN: 14-Pin DIP (0.300")

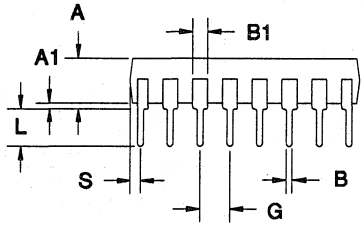


14-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

PN: 16-Pin DIP (0.300")

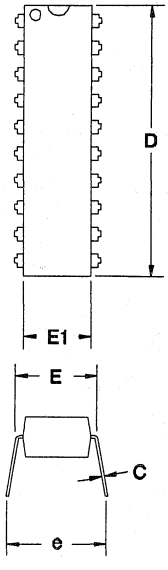


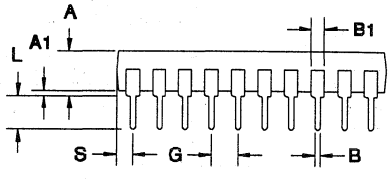


16-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

PN: 20-Pin DIP (0.300")

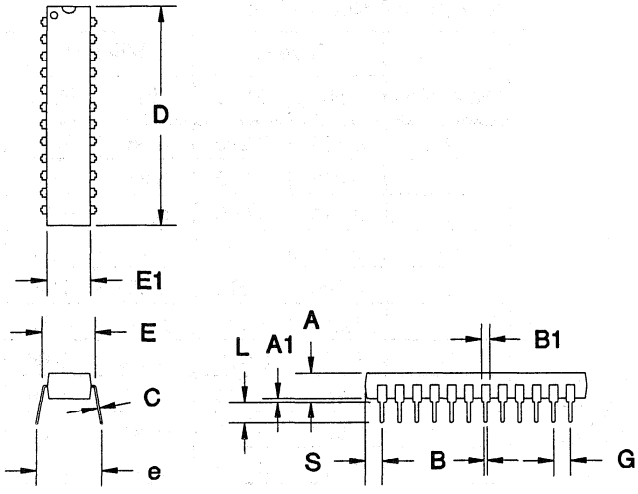




20-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	1.010	1.060	25.65	26.92
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.135	2.92	3.43
S	0.055	0.080	1.40	2.03

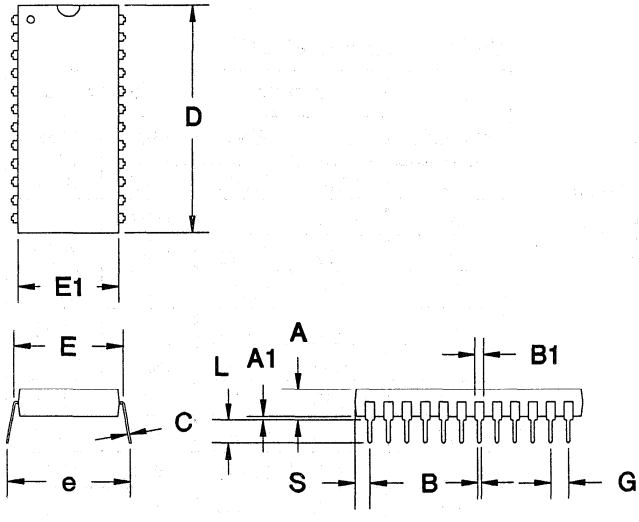
PN: 24-Pin DIP (0.300")



24-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.055	1.14	1.40
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.300	0.325	7.62	8.26
E1	0.250	0.300	6.35	7.62
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

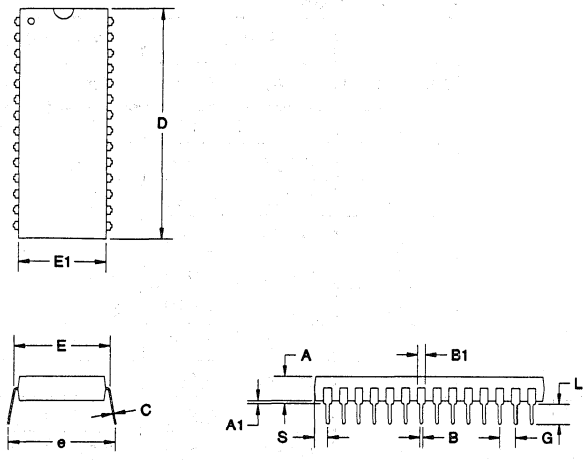
P: 24-Pin DIP (0.600")



24-Pin DIP (0.600" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.190	4.06	4.83
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.600	0.625	15.24	15.88
E1	0.530	0.570	13.46	14.48
e	0.600	0.670	15.24	17.02
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

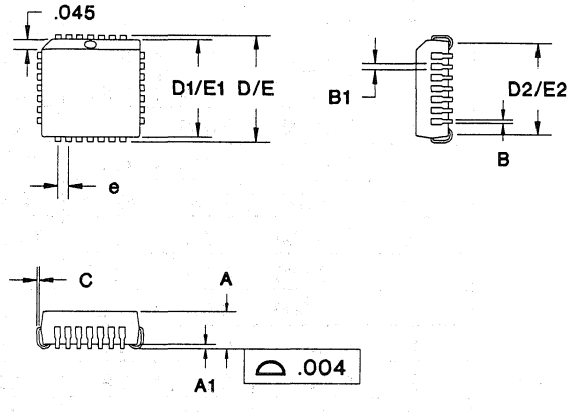
P: 28-Pin DIP (0.600")



28-Pin DIP (0.600" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.190	4.06	4.83
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.013	0.20	0.33
D	1.440	1.480	36.58	37.59
E	0.600	0.625	15.24	15.88
E1	0.530	0.570	13.46	14.48
e	0.600	0.670	15.24	17.02
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

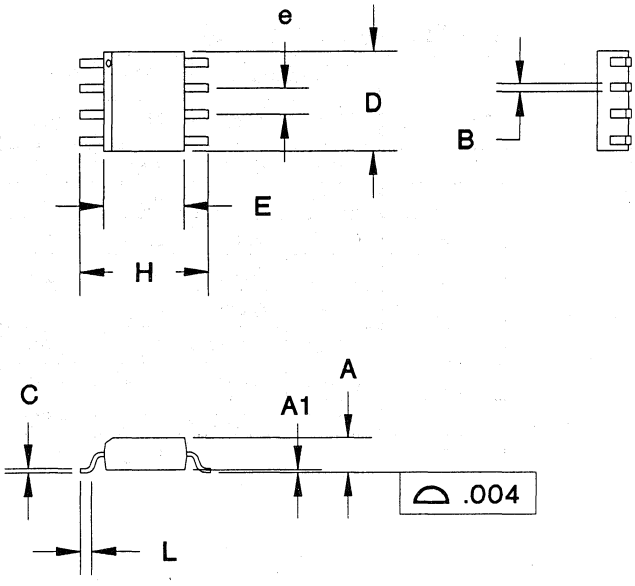
Q: 28-Pin Quad PLCC



28-Pin Q (Quad PLCC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.165	0.180	4.19	4.57
A1	0.020	-	0.51	-
B	0.012	0.021	0.30	0.53
B1	0.025	0.033	0.64	0.84
C	0.008	0.012	0.20	0.30
D	0.485	0.495	12.32	12.57
D1	0.445	0.455	11.30	11.56
D2	0.390	0.430	9.91	10.92
E	0.485	0.495	12.32	12.57
E1	0.445	0.455	11.30	11.56
E2	0.390	0.430	9.91	10.92
e	0.045	0.055	1.14	1.40

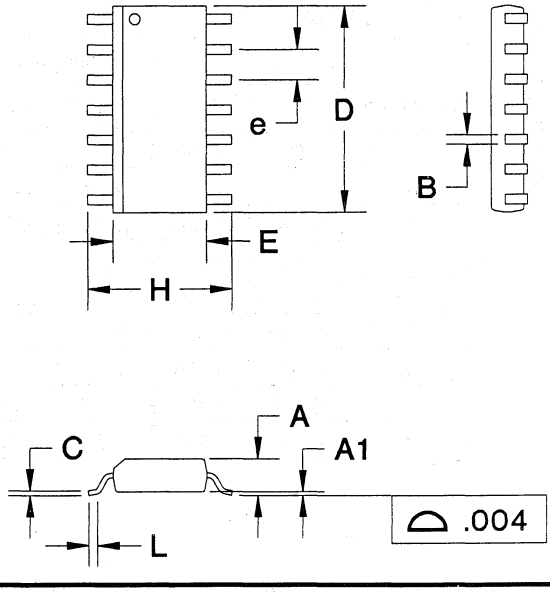
SN: 8-Pin SN (0.150" SOIC)



8-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.185	0.200	4.70	5.08
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

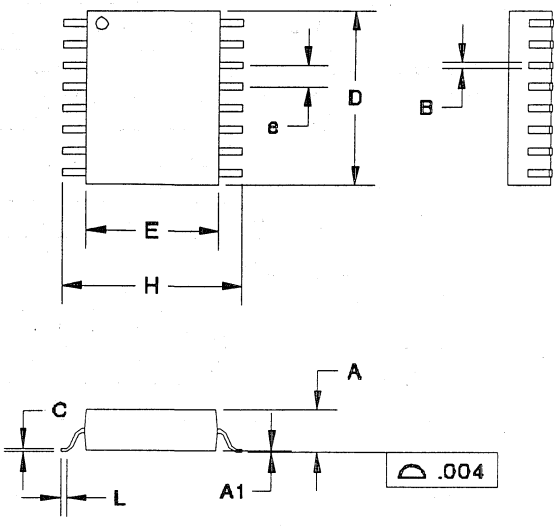
SN: 14-Pin SN (0.150" SOIC)



14-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.335	0.350	8.51	8.89
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

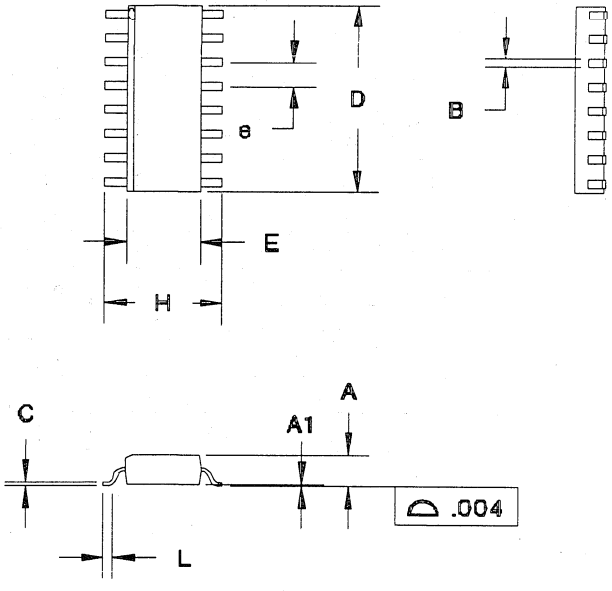
SN: 16-Pin SN (0.150" SOIC)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

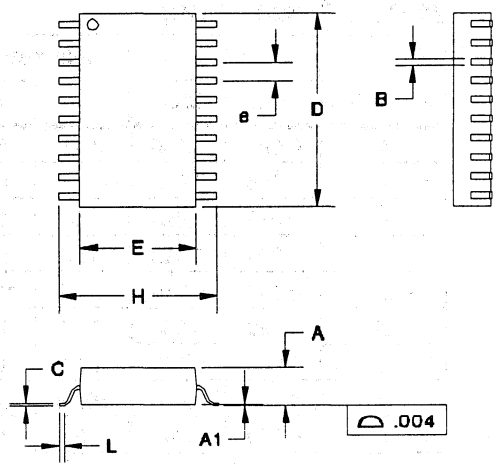
S: 16-Pin S (0.300" SOIC)



16-Pin S (0.300" SOIC)

Dimension	inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.400	0.415	10.16	10.54
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

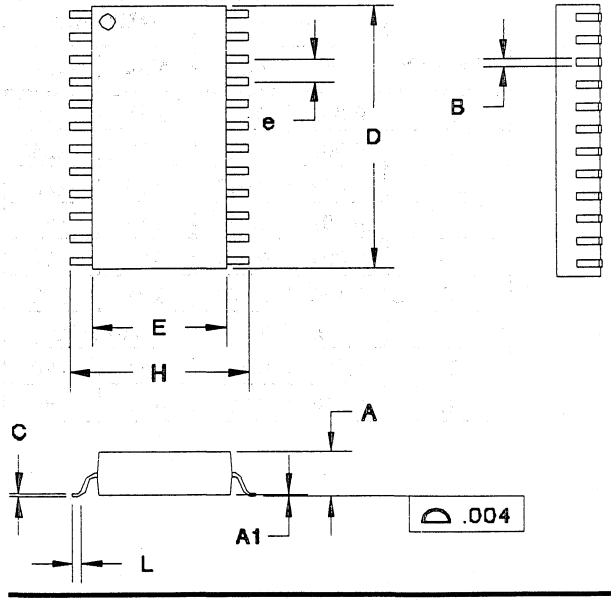
S: 20-Pin S (0.300" SOIC)



20-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.500	0.515	12.70	13.08
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

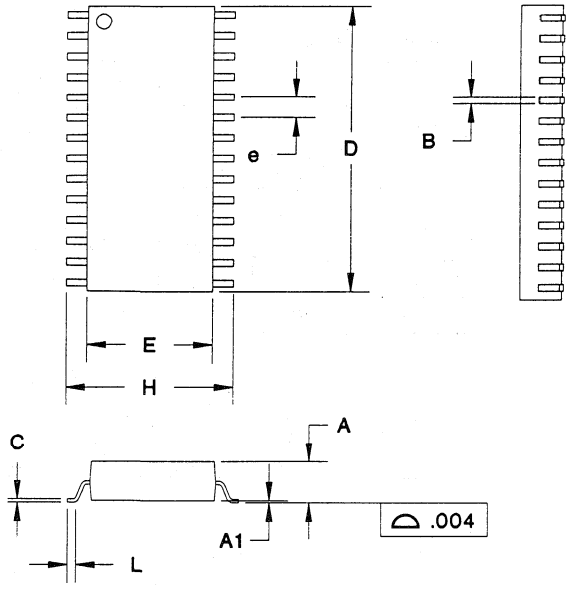
S: 24-Pin S (0.300" SOIC)



24-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.600	0.615	15.24	15.62
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

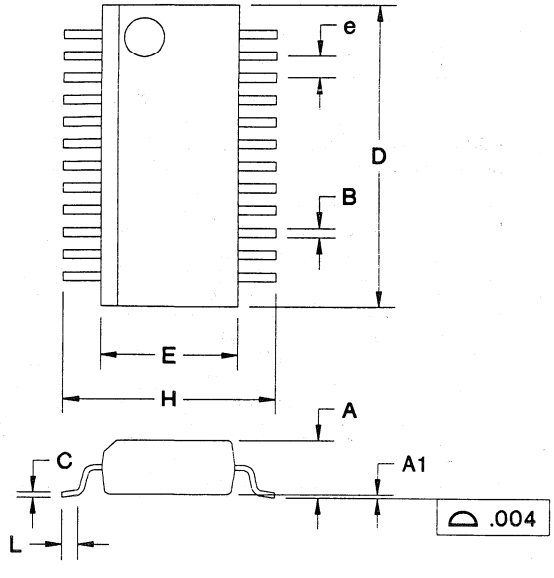
S: 28-Pin S (0.300" SOIC)



28-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.700	0.715	17.78	18.16
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

24-Pin SSOP (SS)



24-Pin SS (0.150" SSOP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.061	0.068	1.55	1.73
A1	0.004	0.010	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
L	0.016	0.035	0.41	0.89

The Benchmarq Quality Policy

It is the policy of Benchmarq to provide the highest-quality products in support of our customers' needs. We recognize that we are in the business of providing not only the physical product, but also documentation, technical support, sales and marketing support, and timely product delivery. Our commitment to our customers begins with product concept and must extend long after actual product purchase and receipt.

We are dedicated to establishing partnerships with our customers and know that to succeed we must help our customers succeed. We will do this by:

- Holding ourselves and our vendors accountable for establishing carefully considered methods and procedures for design, test, and production with clear and concise documentation,
- Responding professionally and expeditiously to customer or vendor problems that arise, bringing to bear the company's strongest resources,
- Developing an industry-leading "Quality Technology" to drive incremental improvements in all the products we provide, and to contribute to a continuous reduction in new product time to market, and
- Continuously providing products and services that meet or exceed the best expectations of our customers.

In pursuing this commitment to quality, we have performed extensive qualification testing on our devices to help ensure the highest levels of product reliability.

We feel confident that the reliability levels demonstrated by our qualification testing will allow us to provide a high-quality product that will meet or exceed our customers' needs. Benchmarq is continuously working toward improving product reliability.

An integral part of quality improvement is customer feedback. We encourage our customers to contact us with any questions or suggestions regarding their individual quality requirements or for information concerning up-to-date product enhancements.

Call us—we want to hear from you.

Underwriters Laboratory Recognition

Benchmarq's ICs and modules have been recognized by Underwriters Laboratory (U.L.®) under file E134016 (R). This helps to hasten U.L. approval of our customers' end equipment.

*For detailed *Quality and Reliability Reports*, contact the factory or your sales representative.

Quality Procedures

To help ensure that our final product is both consistent and reliable, the following quality tests and procedures have been implemented.

Test Probe

Each wafer is electrically tested at test probe to verify parametric integrity. Any wafer not meeting parametric specifications is rejected.

Wafer IQC

Wafer samples are periodically subjected to physical cross-sectional analysis to verify conformance to design and process specifications.

Final Visual

All lots are subjected to QC final visual inspection. The travelers are checked to make sure that the product was properly burned-in and tested. Additionally, lot numbers and counts are verified, and the devices are checked for mechanical integrity.

Board Level Products

All printed circuit board level products are manufactured to meet ANSI/IPC-A-610A and ANSI/IPC-A-600D Class 2 specifications.

Traceability

Full traceability is maintained on all products. The devices are traceable to front-end wafer lot and to assembly lot. Top brand includes the Benchmarq logo, part number, date code, and unique lot number (module products).

Electrostatic Discharge (ESD)

It is recognized that electronic components are susceptible to damage due to electrostatic discharge. To help minimize this risk, the following safeguards have been put into place:

- All personnel who handle devices wear grounded wrist and heel straps and have been trained to use proper device-handling procedures.
- All work surfaces used in the test and QC areas have been grounded. Antistatic flooring is used in the test, QC, and finished goods areas.
- All device testers and handlers have adequate grounding.
- Devices are placed into antistatic tubes and kept in conductive totes or boxes during the manufacturing process.
- Finished goods are stored in conductive boxes. Boxes and shipping containers are labeled with ESD warnings.

Packing and Shipping

Great care is taken to ensure that finished product reaches the customer in perfect condition. All devices are placed in antistatic tubes during the assembly and test operations. Before shipping, device tubes are placed in conductive boxes that are marked with ESD warning labels. The conductive boxes are then placed into non-conductive shipping containers for additional protection against rough handling. The shipping containers are also marked with ESD caution labels.

Process Monitoring

The materials, assembly process, and test process are constantly monitored for problems and inconsistencies. Operator traceability and accountability are maintained so that any problems can be identified earlier and corrections implemented quicker. The wafer foundry and assembly contractor are required to use Statistical Process Control (SPC) techniques to demonstrate that their manufacturing processes and hence, their final products, are in control and will not vary from lot to lot. This constant effort is provided to ensure the highest possible product quality.

Qualification Strategy

Benchmarq's goal is to provide the most reliable products possible. Hence, a combination of devices and packages representative of the front-end and back-end processes are selected for reliability testing. Three levels of qualification and reliability testing are performed on each product family. They are as follows:

Wafer Level

Wafer-level qualification is performed so that the reliability of the front-end process may be ascertained. Wafers from three front-end wafer lots are analyzed. Design rules such as critical dimensions, film thicknesses, step coverages, and oxide integrity are verified using a combination of electrical and visual analysis. Also, a series of tests designed to check the reliability of passivation, thin oxides, metal, and transistors are performed.

By analyzing the device in wafer form, any major process or design reliability problems are uncovered early in the product development phase where they can be more quickly corrected.

Package Level

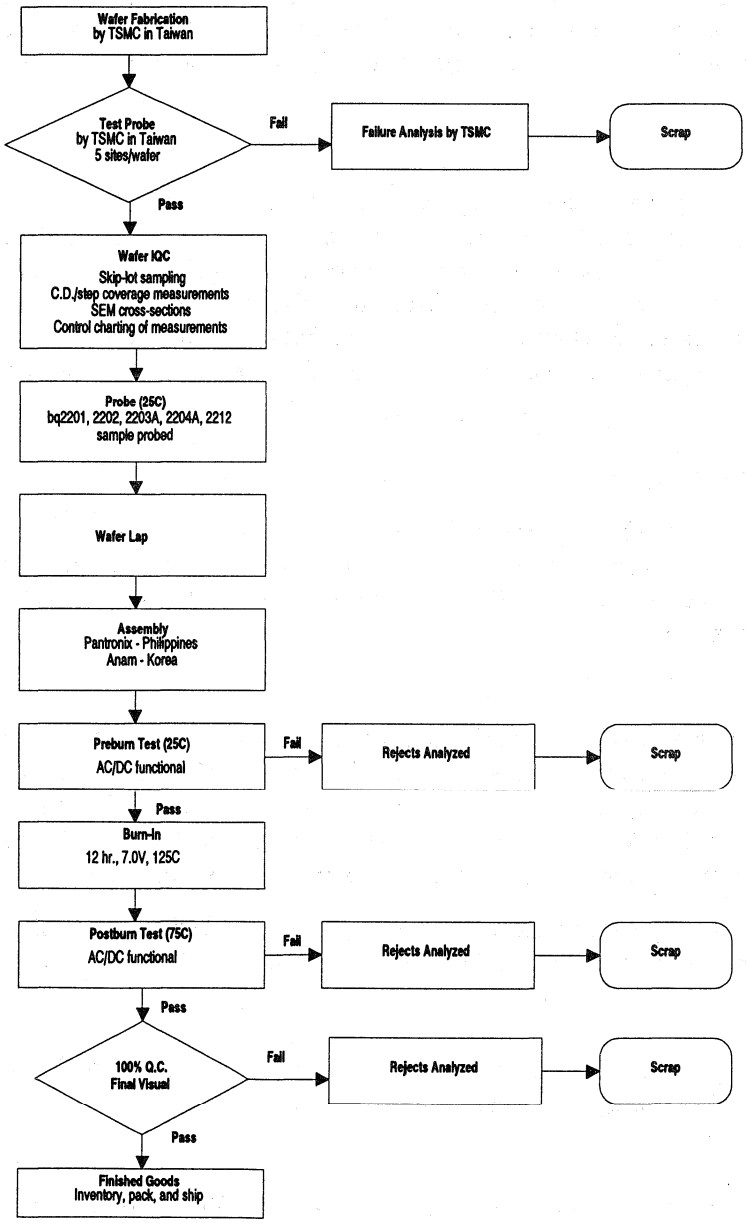
An assessment is performed on various package types to determine the reliability and manufacturability of the packaging process and materials.

System Level

Finally, a series of stringent environmental and operating life stresses are performed on packaged devices so that the short-term and long-term reliability of the product may be ensured. Infant life and long-term life predictions are then made based on this data.

NVSRAM Controllers

NVSRAM Controller Process Flow



Qualification Summary—NVSRAM Controllers

Product: NVSRAM Controllers (bq2201, bq2202, bq2204)

Qual Vehicle: bq2201SN 8-pin, 150-mil SOIC
(Lot: T044002AACPA Date Code: 9046)

High-Temperature Operating Life Test (5.5V, 150°C)

48 hrs	96 hrs	168 hrs
0/100	0/100	0/100

Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/298	0/298	0/298	1/298 [1]	0/297

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/89	0/89	0/89	1/89 [1]	0/88

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	0/50	0/50	0/50	0/50

Highly Accelerated Stress Test—HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	72 hrs
0/50	0/50	0/50

Temperature Cycling (-65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/97 [1]	0/97	0/97

Thermal Shock (-55°C to 125°C)

30 cyc
0/50

Moisture Resistance (unbiased, -10°C to 65°C, 90%RH)

10 cyc
0/50

Resistance to Soldering Heat (260°C, 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/24 leads fail
Lead Fatigue	0/16 leads fail
Lead Finish	0/24 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 1000V
Latch-up Immunity	>± 200mA

[1] Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

Predicted Failure Rates—NVSRAM Controllers

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (based on 85°C/85% RH THB failure)
- Temperature derated to 55°C (typical use condition)

$AF_{(55°C - 125°C)} = 77.8$

$AF_{(55°C - 150°C)} = 259.9$

Total device hours:

bq2201 2000 hours x 298 devices x 77.8 = 46,368,800 device hours
bq2201 168 hours x 100 devices x 259.9 = 4,366,320 device hours
bq1001 1000 hours x 100 devices x 77.8 = 7,780,000 device hours

Total device hours = 5.8515×10^7 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 1/5.815 \times 10^7 \text{ hours}$$

$$= 17.1 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 1
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f	=	number of failures
α	=	1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(4,\ 0.4)}}{2 \times (5.8515 \times 10^7)}$$

$$= 4.1175/(1.1703 \times 10^8)$$

$$= 3.52 \times 10^{-8}/\text{hours}$$

$$= 35.2 \text{ FITS}$$

Therefore, for the NVSRAM controllers built using the TSMC 1.2µ single-poly, double-level metal CMOS process, the mature life FIT rate is 36 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers a failure that occurs within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Derating for 150°C:

Infant life time	= AF x device stress hours
8760 hours	= 259.9 x device stress hours
Device stress hours	= 33.7 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life or in the first 33.7 hours of 150°C operating life is considered an infant life failure.

Total device hours:

bq2201 112.6 hours x 298 devices x 77.8 = 2,610,563 device hours
bq2201 33.7 hours x 100 devices x 259.9 = 875,863 device hours
bq1001 112.6 hours x 100 devices x 77.8 = 876,028 device hours

Total device hours = 4.3624×10^6 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 4.3624 \times 10^6 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f	=	number of failures
α	=	1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (4.3624 \times 10^6)}$$

$$= 1.8970 / (8.7249 \times 10^6)$$

$$= 2.174 \times 10^{-7} / \text{hours}$$

$$= 217.4 \text{ FITS}$$

Therefore, for the NVSRAM controllers built using the TSMC 1.2μ single-poly, double-level metal CMOS process, the infant life FIT rate is approximately 218 FITS.

NVSRAMs

NVSRAM Module Construction

Benchmarq's NVSRAM modules are designed and built by Benchmarq in Carrollton, Texas. Each module is constructed of one or more ICs mounted on a printed circuit board along with a lithium battery. This subassembly is then placed into a plastic housing and encapsulated with a specialized two-part epoxy. (The bq2502 Integrated Backup Unit is manufactured in the same manner.)

Quality Procedures

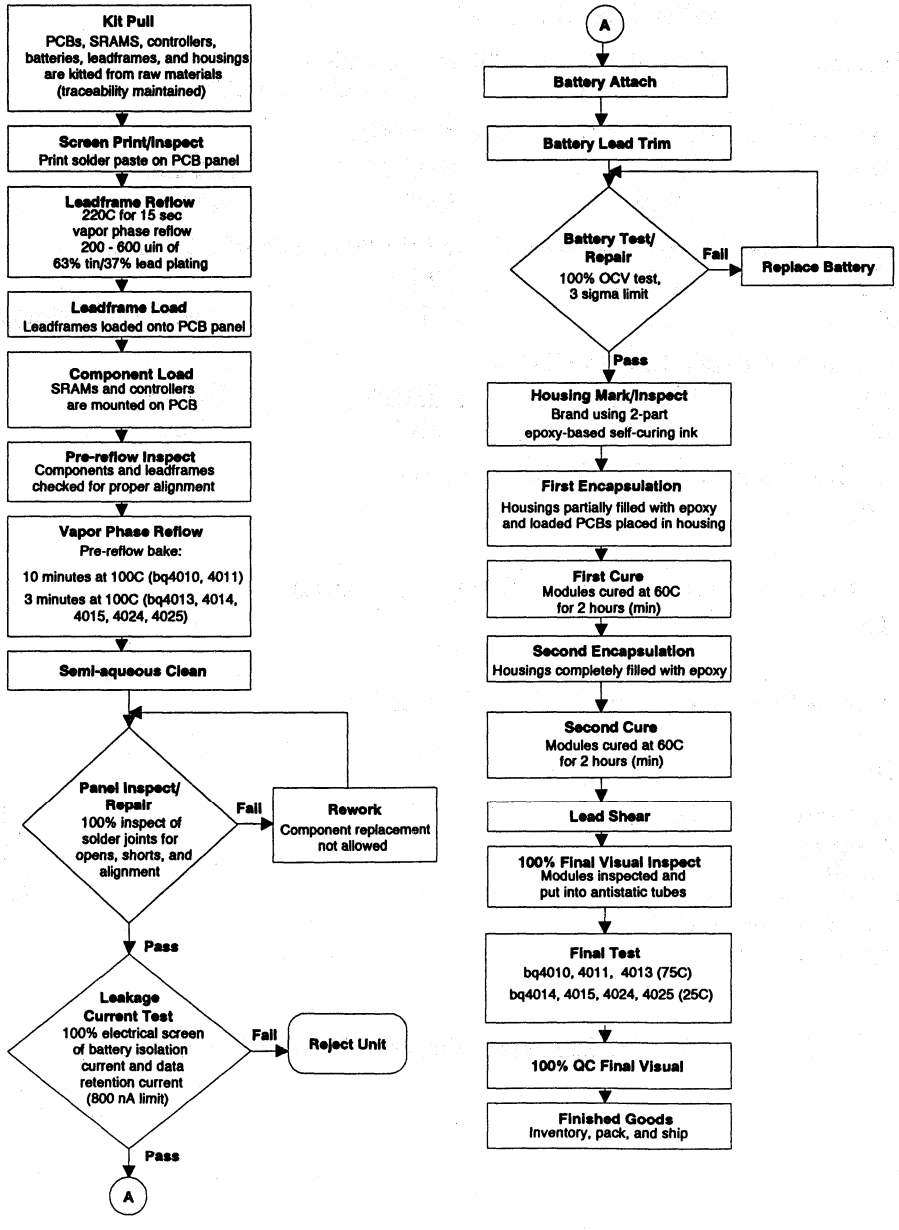
To help ensure that our final product is both consistent and reliable, the following quality inspections and tests are performed:

- **SRAMs**—Low-powered SRAMs are used in the manufacture of modules. At incoming inspection, data-retention current is measured on a representative sample from each lot. After the components are mounted on the circuit boards, the circuits are 100% tested for data-retention current.
- **Batteries**—Certificates of Compliance verifying the Open Circuit Voltage (OCV), Closed Circuit Voltage (CCV), and Internal Resistance (IR) are required from the manufacturer on each shipment. Historical statistical sampling indicates that a Lot Tolerant Percent Defective (LTPD) of less than 1% at a confidence level of 90% can be expected. After batteries are mounted on the circuit boards, they are 100% tested for OCV.
- **PCBs**—A sample from each lot of printed circuit boards is visually inspected for router damage, breakouts, opens, shorts, or misaligned solder masks.
- **Leads**—Certificates of Compliance verifying the plating thickness are required from the manufacturer. Periodic quality audits of the plating thickness are performed.

Traceability

Full traceability is maintained on both the integrated circuits and modules. The integrated circuits are traceable to front-end wafer lot and to assembly lot. The modules are traceable to housing, PCB, battery, controller, and SRAM lots.

NVSRAM Module Process Flow



Qualification Summary—NVSRAM Modules

Product NVSRAM Modules (bq4010, bq4011, bq4011H, bq4013, bq4014, bq4015, bq4024, bq4025, bq2502)

Qual Vehicle bq4010MA 28-pin, 600-mil Module
(Lot: QM04901 Date Code: 9049)

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/99	0/99	0/96 [1]	0/96	0/96

Highly Accelerated Stress Test*—HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	72 hrs	
0/80	0/80	4/79 [1]	*(without battery)

Temperature Cycling (-40°C to +85°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (-55°C to 125°C) without battery

30 cyc
0/105

Moisture Resistance (unbiased, -10°C to 65°C, 90%RH)

10 cyc
0/50

Resistance to Soldering Heat (260°C, 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/56 leads fail
Lead Fatigue	0/84 leads fail
Lead Finish	0/56 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 1000V
Latch-up Immunity	>± 200mA

[1] Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

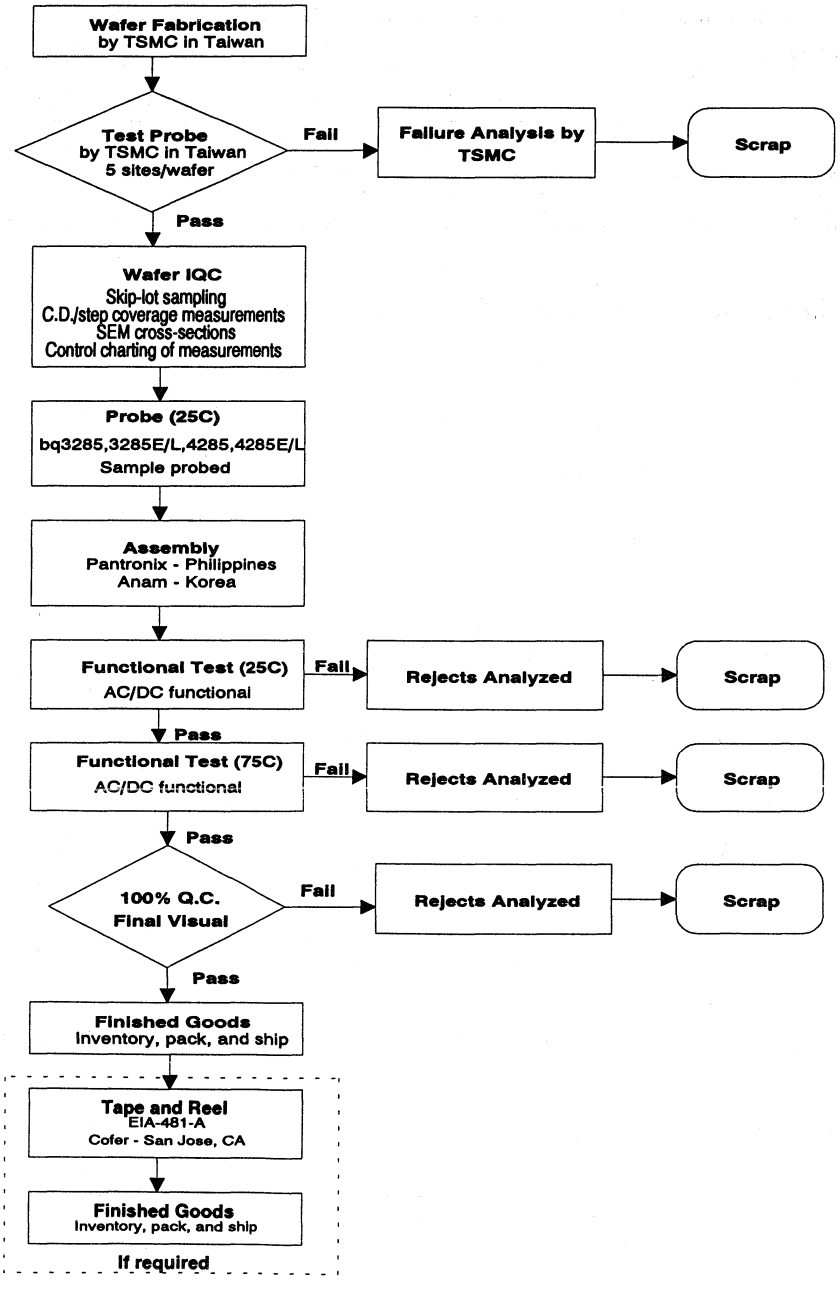
In the case of modules, an approximate FIT rate can be determined by adding together the FIT rates of the various components. The FIT rates used and their sources are listed below:

Component	FIT Rate	Source
Controller	36	Calculated in previous section
SRAM	35	SRAM manufacturer
Battery	<10	Panasonic (approximate)
Total	81 FITS	

Therefore, for our module products, the FIT rate is approximately 81 FITS.

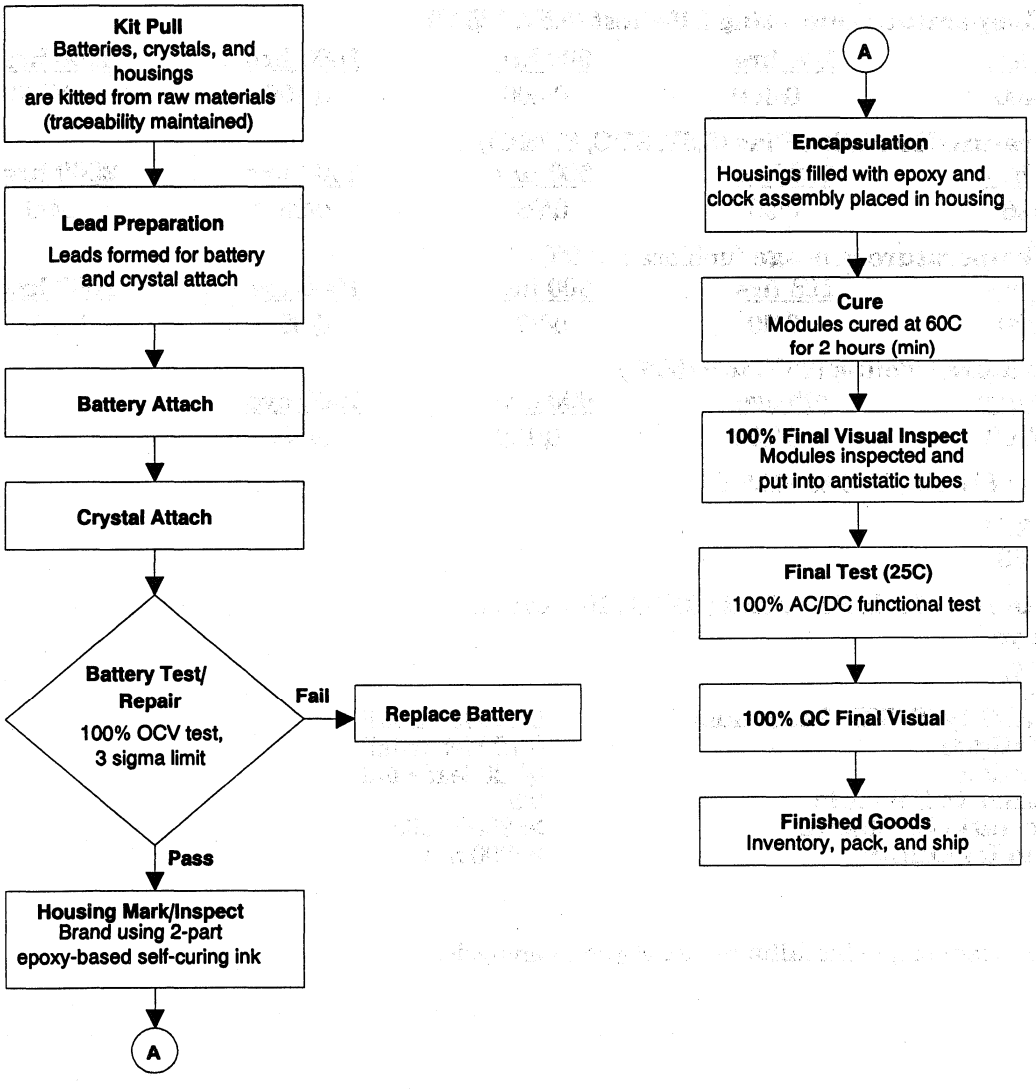
REAL-TIME CLOCKS (RTCs)

Real-Time Clock IC Process Flow



Real-Time Clock Module Process Flow

All modules are built by Benchmarq in Carrollton, Texas.



Qualification Summary-Real-Time Clock ICs

Product: RealTime Clocks (bq3285, bq3285E/L, bq4285, bq4285E/L)

Qual Vehicle: bq3285ES, 24pin 300mil SOIC

(Lot: 285AAEA, T346002, A61453.2 Date Code: 9332EP)

High-Temperature Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/400	0/400	0/400	0/400	0/400

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/96	0/96	0/96	0/96	0/96

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/30	0/30	0/30	0/30	* 1/30

Temperature Cycling (65°C to +150°C)

100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/120 leads fail
Lead Fatigue	0/120 leads fail
Lead Finish	0/120 leads fail
Resistance to Solvents	0/5
Electrostatic Discharge	>±2000 volts
Latchup Immunity	>±200 mA

* Intermittent single bit failure—destroyed in analysis.

Qualification SummaryRealTime Clock Modules

Product: RealTime Clock Modules (bq3287, bq3287A, bq3287E, bq3287L, bq3287EA, bq3287LA, bq4287E, bq4287L)

Qual Vehicle: bq3287MT, 24pin 600mil Module

(Lot: QM147001 Date Code: 9147)

(Lot: PM205004 Date Code: 9205)

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/100	0/100	0/100	0/100	0/100

Highly Accelerated Stress Test HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	144 hrs
0/75	0/75	0/75

Temperature Cycling (65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/95

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/24 leads fail
Lead Fatigue	0/72 leads fail
Lead Finish	0/72 leads fail
Resistance to Solvents	0/4
Physical Dimension	0/4

Predicted Failure RatesRealTime Clock I.C.s

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)
- $AF_{(55°C - 125°C)} = 77.8$
- Voltage derated to 5.5V (typical use condition)
- $AF_{(5.5V - 7.0V)} = 5.0$ (conservative estimate)

Total device hours:

bq3285 2000 hours x 400 devices x 77.8 x 5.0 = 311,200,000 device hours

Total device hours = 3.1120×10^8 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 3.1120 \times 10^8 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0

Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures

α= 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (1.2448 \times 10^8)}$$

$$= 1.8970/(6.224 \times 10^8)$$

$$= 3.05 \times 10^{-9}/\text{hours}$$

$$= 3.05 \text{ FITS}$$

Therefore, for the real-time clock integrated circuit built using the TSMC 0.8µ CMOS single-poly, double-level metal process, the mature life FIT rate is approximately 3 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total device hours:

bq3285 112.6 hours x 400 devices x 77.8 x 5.0 = 17,520,560 device hours

Total device hours = 1.7520×10^7 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 1.7520 \times 10^7 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

Number of failures: 0

Confidence level: 60%

where:

f = number of failures

α= 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times \left(7.0082 \times 10^6\right)}$$

$$= 1.8970 / (3.5041 \times 10^7)$$

$$= 5.4136 \times 10^{-8} / \text{hours}$$

$$= 54.1 \text{ FITS}$$

Therefore, for the real-time clock integrated circuit built using the TSMC 0.8 single-poly, double-level metal CMOS process, the infant life FIT rate is approximately 54 FITS.

Predicted Failure Rates RealTime Clock Modules

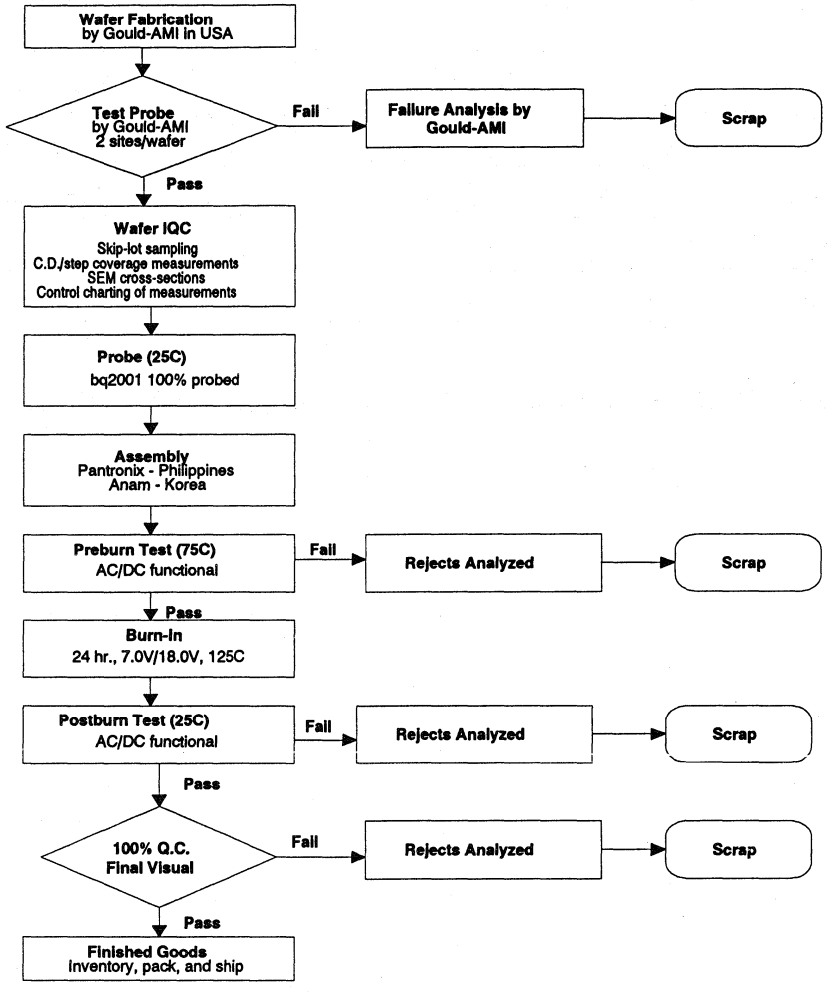
In the case of modules, an approximate FIT rate can be determined by adding together the FIT rates of the various components. The FIT rates used and their sources are listed below:

Component	FIT Rate	Source
Real-Time Clock IC	3	Calculated in previous section
Crystal	<5	Daiwa (approximate)
Battery	<2	Panasonic (approximate)
Total	10 FITS	

Therefore, for our RTC module products, the FIT rate is approximately 10 FITS.

Energy Management Units (EMUs)

Energy Management Unit Process Flow



Qualification Summary-Energy Management Units

Product: Energy Management Unit (bq2001)

Qual Vehicle: bq2001, 24-pin 300-mil SOIC
(Lot: A129001ABCK, A135001ADQK, A135001AEEK, A135001AJCA, A137002AACA, A206003ABCA)
(Date Code: 9130, 9135, 9136, 9141, 9141, 9208)

High-Temperature Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/300	0/300	0/300	0/300	0/300

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/84	0/84	0/84	0/84	0/84

Temperature/Humidity/Bias (7.0V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/100	0/100	0/100	0/100	0/100

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	0/50	0/50	0/50	0/50

Highly Accelerated Stress Test - HAST (5.5V, 130°C, 85%RH, 1.7 atm)

48 hrs	96 hrs	168 hrs
0/99	0/99	0/99

Temperature Cycling (-65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	1/100[1]	0/99	0/99	1/99[1]

Thermal Shock (-55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/168 leads fail
Lead Fatigue	0/72 leads fail
Lead Finish	0/72 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 2000 volts
Latch-up Immunity	>± 200 mA

[1] Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

Predicted Failure Rates—Energy Management Units

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)

  $AF_{(55°C - 125°C)} = 77.8$
- Voltage derated to 5.5V (typical use condition)

  $AF_{(5.5V - 7.0V)} = 5.0$ (conservative estimate)

Total device hours:

bq2001 2000 hours x 300 devices x 77.8 = 46,680,000 device hours
bq2001 2000 hours x 84 devices x 77.8 x 5.0 = 65,352,000 device hours

Total device hours = 1.1203×10^8 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 1.1203 \times 10^{8} \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2f + 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
α = 1 – confidence level

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times \left(1.1203 \times 10^{8} \right)}$$

$$= 1.8970 / (2.2406 \times 10^{8})$$

$$= 8.4663 \times 10^{-9} / \text{hours}$$

$$= 8.5 \text{ FITS}$$

Therefore, for the EMUs built using the Gould-AMI 1.5µ BiCMOS process, the mature life FIT rate is approximately 9 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total device hours:

bq2001 112.6 hours x 300 devices x 77.8 = 2,628,084 device hours
bq2001 112.6 hours x 84 devices x 77.8 x 5.0 = 3,679,320 device hours

Total device hours = 6.3074×10^6 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 6.3074 \times 10^6 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f	=	number of failures
α	=	1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (6.3074 \times 10^6)}$$

$$= 1.8970/(1.2615 \times 10^7)$$

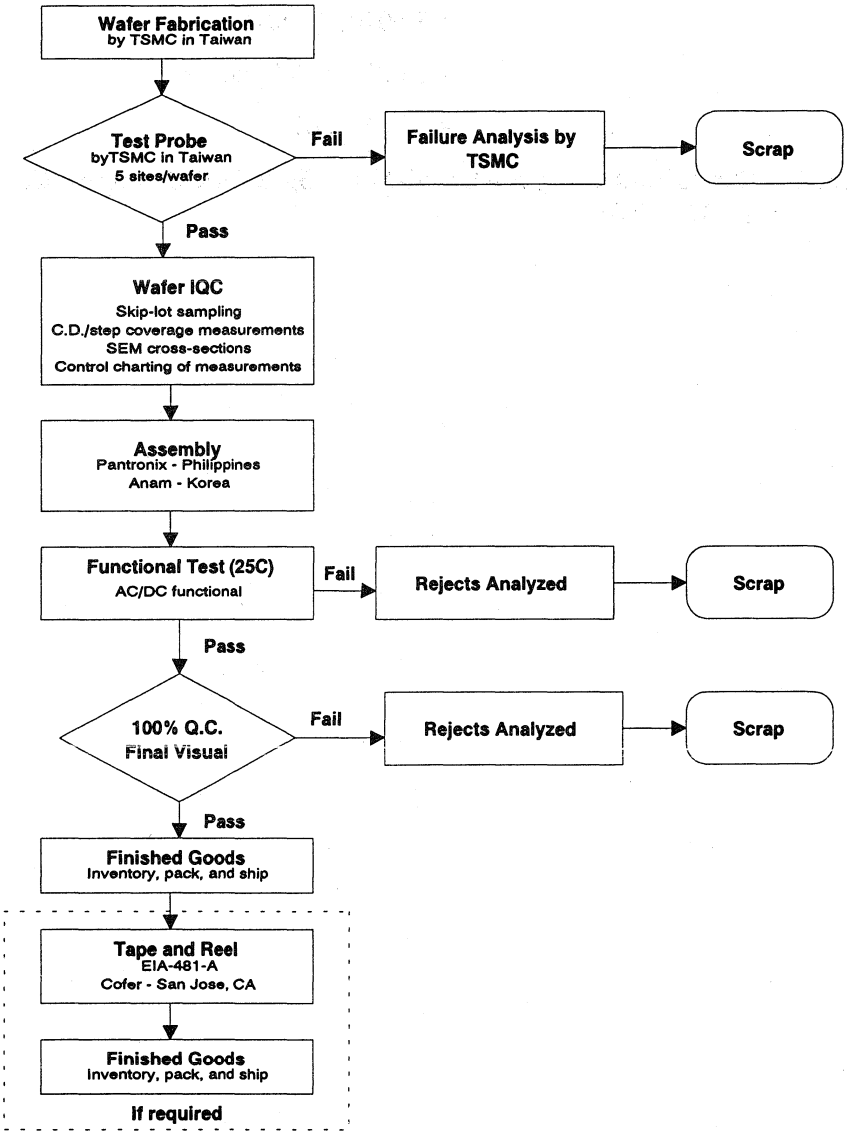
$$= 1.5038 \times 10^{-7}/\text{hours}$$

$$= 150.4 \text{ FITS}$$

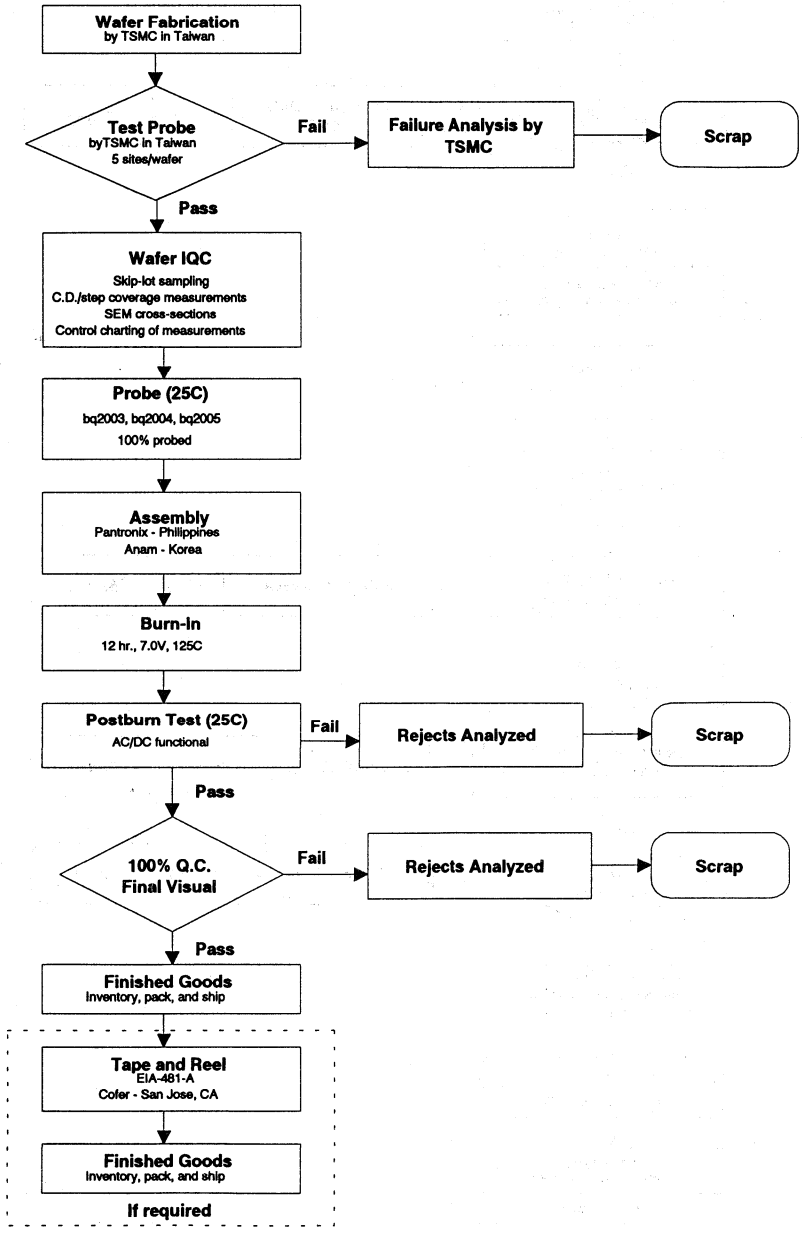
Therefore, for the EMUs built using the Gould-AMI 1.5μ BiCMOS process, the infant life FIT rate is approximately 151 FITS.

Battery Management ICs

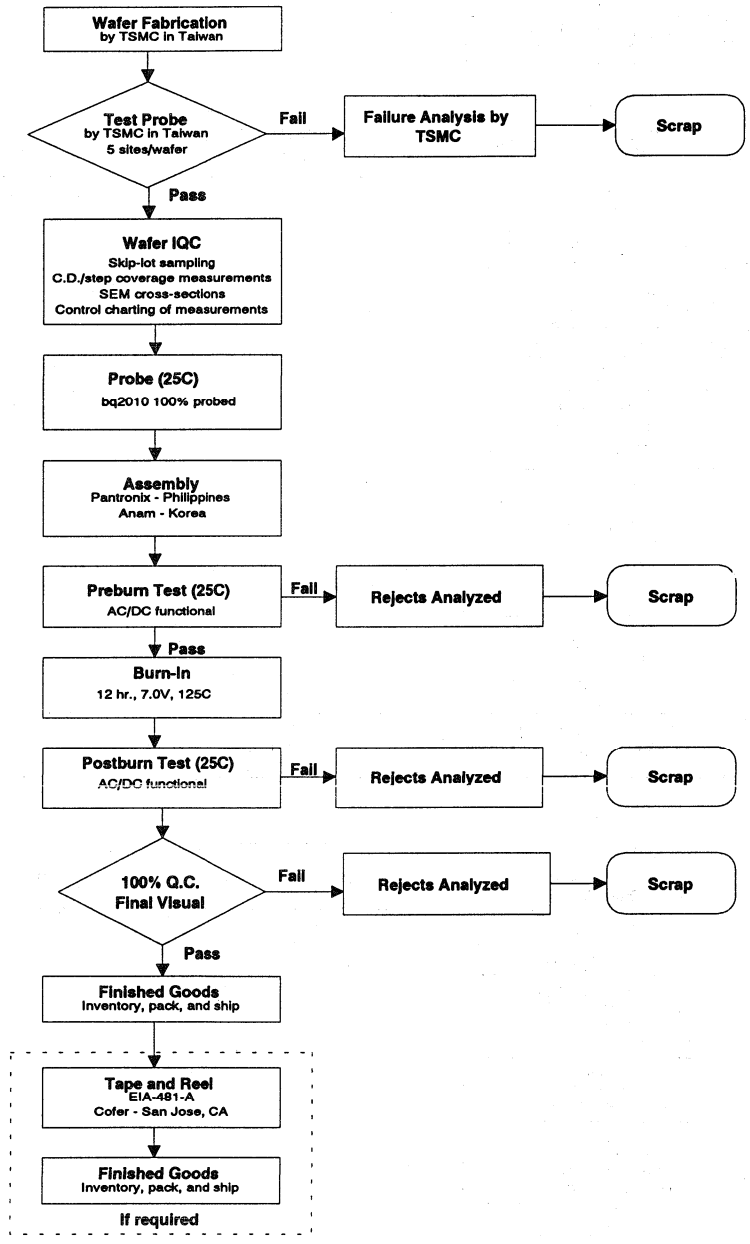
bq2002 Fast Charge IC Process Flow



bq2003, 2004, 2005 Fast Charge IC Process Flow



bq2010 Gas Gauge IC Process Flow



Qualification Summary—Fast Charge IC

Product: bq2003 Fast Charge IC

Qual Vehicle: 20-pin 300-mil PDIP

(Lots: T221001, T237001, T244012)

(Lot: 211ABCP Date Code: 9226-EP)

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/399	0/399	0/399	0/399	0/399

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/120	0/120	0/120	0/120	0/120

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	0/50	0/50	0/50	0/50

Temperature Cycling (65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/96 leads fail
Lead Fatigue	0/80 leads fail
Lead Finish	0/80 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 2000 volts
Latchup Immunity	>± 200 mA

Qualification Summary—Dual-Battery Fast Charge IC

Product: bq2005 Dual-Battery Fast Charge IC

Qual Vehicle: 20-pin 300-mil SOIC

(Lot: 232AACA Date Code: 9329)

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs
0/144	0/144	0/144	0/144

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs
0/99	0/99	0/99	0/99

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs
0/50	0/50	0/50	0/50

Temperature Cycling (65°C to +150°C)

100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/100 leads fail
Lead Fatigue	0/100 leads fail
Lead Finish	0/100 leads fail
Resistance to Solvents	0/5 devices fail
Electrostatic Discharge	>± 2000 volts
Latchup Immunity	>± 200 mA

Predicted Failure Rates—Fast Charge ICs

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)
- $AF_{(55°C - 125°C)} = 77.8$
- Voltage derated to 5.5V (typical use condition)
- $AF_{(5.5V - 7.0V)} = 5.0$ (conservative estimate)

Total equivalent device hours:

bq2003 2000 hours x 399 devices x 77.8 x 5.0 = 310,422,000 device hours
bq2005 1000 hours x 144 devices x 77.8 x 5.0 = 56,016,000 device hours

Total equivalent device hours: 366,438,000 device hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 3.66438 \times 10^{8} \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0

Confidence level: 60%

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2f + 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures

α = 1 – confidence level

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (3.10422 \times 10^{8})}$$

$$= 1.8970 / (7.32876 \times 10^{8})$$

$$= 2.59 \times 10^{-9} / \text{hours}$$

$$= 2.6 \text{ FITS}$$

Therefore, for the Battery Management ICs built using the TSMC 1.2µ double-level poly, double-level metal CMOS process, the mature life FIT rate is approximately 3 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total equivalent device hours:

bq2003 112.6 hours x 399 devices x 77.8 x 5.0 = 17,476,759 device hours
bq2005 112.6 hours x 144 devices x 77.8 x 5.0 = 6,307,402 device hours

Total equivalent device hours: 23,784,161 device hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 2.3784 \times 10^{7} \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0

Confidence level: 60%

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures

α = 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (1.7477 \times 10^7)}$$

$$= 1.8970 / (4.7568 \times 10^7)$$

$$= 3.9880 \times 10^{-8} / \text{hours}$$

$$= 39.9 \text{ FITS}$$

Therefore, for the Battery Management ICs built using the TSMC 1.2µ double-level poly, double-level metal CMOS process, the infant life FIT rate is approximately 40 FITS.

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